Microchip Technology - ATXMEGA32D4-AU Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega32d4-au

Ordering Code	Flash (Bytes)	EEPROM (Bytes)	SRAM (Bytes)	Speed (MHz)	Power Supply	Package[1][2][3]	Temp
ATxmega128D4-AN	128K + 8K	2K	8K	32	1.6 - 3.6V	44A	-40°C - 105°C
ATxmega128D4-ANR[4]	128K + 8K	2K	8K				
ATxmega64D4-AN	64K + 4K	2K	4K				
ATxmega64D4-ANR[4]	64K + 4K	2K	4K				
ATxmega32D4-AN	32K + 4K	1K	4K				
ATxmega32D4-ANR[4]	32K + 4K	1K	4K				
ATxmega16D4-AN	16K + 4K	1K	2K				
ATxmega16D4-ANR[4]	16K + 4K	1K	2K				
ATxmega128D4-M7	128K + 8K	2K	8K			44M1	
ATxmega128D4-M7R[4]	128K + 8K	2K	8K				
ATxmega64D4-M7	64K + 4K	2K	4K				
ATxmega64D4-M7R[4]	64K + 4K	2K	4K				
ATxmega32D4-M7	32K + 4K	1K	4K				
ATxmega32D4-M7R[4]	32K + 4K	1K	4K				
ATxmega16D4-M7	16K + 4K	1K	2K				
ATxmega16D4-M7R[4]	16K + 4K	1K	2K				

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For packaging information see "Packaging information" on page 64.
4. Tape and Reel.

Package type	
44A	44-lead, 10*10mm body size, 1.0mm body thickness, 0.8mm lead pitch, thin profile plastic quad flat package (TQFP)
44M1	44-Pad, 7*7*1mm body, lead pitch 0.50mm, 5.20mm exposed pad, thermally enhanced plastic very thin quad no lead package (VQFN)
49C2	49-ball (7 * 7 Array), 0.65mm pitch, 5.0*5.0*1.0mm, very thin, fine-pitch ball grid array package (VFBGA)

Typical Applications

Industrial control	Climate control	Low power battery applications
Factory automation	RF and ZigBee®	Power tools
Building control	USB connectivity	HVAC
Board control	Sensor control	Utility metering
White goods	Optical	Medical applications

7.8 Data Memory and Bus Arbitration

Since the data memory is organized as four separate sets of memories, the bus masters (CPU, etc.) can access different memory sections at the same time.

7.9 Memory Timing

Read and write access to the I/O memory takes one CPU clock cycle. A write to SRAM takes one cycle, and a read from SRAM takes two cycles. EEPROM page load (write) takes one cycle, and three cycles are required for read. For burst read, new data are available every second cycle. Refer to the instruction summary for more details on instructions and instruction timing.

7.10 Device ID and Revision

Each device has a three-byte device ID. This ID identifies Atmel as the manufacturer of the device and the device type. A separate register contains the revision number of the device.

7.11 I/O Memory Protection

Some features in the device are regarded as critical for safety in some applications. Due to this, it is possible to lock the I/O register related to the clock system, the event system, and the advanced waveform extensions. As long as the lock is enabled, all related I/O registers are locked and they can not be written from the application software. The lock registers themselves are protected by the configuration change protection mechanism.

7.12 Flash and EEPROM Page Size

The flash program memory and EEPROM data memory are organized in pages. The pages are word accessible for the flash and byte accessible for the EEPROM.

Table 7-2 on page 16 shows the Flash Program Memory organization and Program Counter (PC) size. Flash write and erase operations are performed on one page at a time, while reading the Flash is done one byte at a time. For Flash access the Z-pointer (Z[m:n]) is used for addressing. The most significant bits in the address (FPAGE) give the page number and the least significant address bits (FWORD) give the word in the page.

Table 7-2. Number of Words and Pages in the Flash

Devices	PC size	Flash size	Page Size	FWORD	FPAGE	Application		Boot	
	bits	bytes	words			Size	No of pages	Size	No of pages
ATxmega16D4	14	16K + 4K	128	Z[7:1]	Z[13:8]	16K	64	4K	16
ATxmega32D4	15	32K + 4K	128	Z[7:1]	Z[14:8]	32K	128	4K	16
ATxmega64D4	16	64K + 4K	128	Z[7:1]	Z[15:8]	64K	256	4K	16
ATxmega128D4	17	128K + 8K	128	Z[9:1]	Z[16:8]	128K	512	8K	32

Table 7-3 on page 17 shows EEPROM memory organization for the Atmel AVR XMEGA D4 devices. EEEPROM write and erase operations can be performed one page or one byte at a time, while reading the EEPROM is done one byte at a time. For EEPROM access the NVM address register (ADDR[m:n]) is used for addressing. The most significant bits in the address (E2PAGE) give the page number and the least significant address bits (E2BYTE) give the byte in the page.

32.1.13.7 External 16MHz Crystal Oscillator and XOSC Characteristics

Table 32-25. External 16MHz Crystal Oscillator and XOSC Characteristics

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Cycle to cycle jitter	XOSCPWR=0	FRQRANGE=0		0		ns
			FRQRANGE=1, 2, or 3		0		
		XOSCPWR=1			0		
	Long term jitter	XOSCPWR=0	FRQRANGE=0		0		
			FRQRANGE=1, 2, or 3		0		
		XOSCPWR=1			0		
	Frequency error	XOSCPWR=0	FRQRANGE=0		0.03		%
			FRQRANGE=1		0.03		
			FRQRANGE=2 or 3		0.03		
		XOSCPWR=1			0.003		
	Duty cycle	XOSCPWR=0	FRQRANGE=0		50		
			FRQRANGE=1		50		
			FRQRANGE=2 or 3		50		
		XOSCPWR=1			50		
R_Q	Negative impedance	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF		44k		Ω
			1MHz crystal, CL=20pF		67k		
			2MHz crystal, CL=20pF		67k		
		XOSCPWR=0, FRQRANGE=1, CL=20pF	2MHz crystal		82k		
			8MHz crystal		1500		
			9MHz crystal		1500		
		XOSCPWR=0, FRQRANGE=2, CL=20pF	8MHz crystal		2700		
			9MHz crystal		2700		
			12MHz crystal		1000		
		XOSCPWR=0, FRQRANGE=3, CL=20pF	9MHz crystal		3600		
			12MHz crystal		1300		
			16MHz crystal		590		
		XOSCPWR=1, FRQRANGE=0, CL=20pF	9MHz crystal		390		
			12MHz crystal		50		
			16MHz crystal		10		

32.2.8 Bandgap and Internal 1.0V Reference Characteristics

Table 32-41. Bandgap and Internal 1.0V Reference Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Startup time	As reference for ADC		1 Clk_{PER} + 2.5µs		µs
		As input voltage to ADC and AC		1.5		
	Bandgap voltage			1.1		V
INT1V	Internal 1.00V reference	T= 85°C, after calibration	0.98	1	1.02	
	Variation over voltage and temperature	Calibrated at T= 85°C, V_{CC} = 3.0V		±1.0		%

32.2.9 Brownout Detection Characteristics

Table 32-42. Brownout Detection Characteristics(1)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{BOT}	BOD level 0 falling V_{CC}		1.50	1.62	1.75	V
	BOD level 1 falling V_{CC}			1.8		
	BOD level 2 falling V_{CC}			2.0		
	BOD level 3 falling V_{CC}			2.2		
	BOD level 4 falling V_{CC}			2.4		
	BOD level 5 falling V_{CC}			2.6		
	BOD level 6 falling V_{CC}			2.8		
	BOD level 7 falling V_{CC}			3.0		
t_{BOD}	Detection time	Continuous mode		0.4		µs
		Sampled mode		1000		
V_{HYST}	Hysteresis			1.2		%

Note: 1. BOD is calibrated at 85°C within BOD level 0 values, and BOD level 0 is the default level.

32.2.10 External Reset Characteristics

Table 32-43. External Reset Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{EXT}	Minimum reset pulse width		1000	90		ns
V_{RST}	Reset threshold voltage (V_{IH})	V_{CC} = 2.7 - 3.6V	0.6*V_{CC}			V
		V_{CC} = 1.6 - 2.7V	0.6*V_{CC}			
	Reset threshold voltage (V_{IL})	V_{CC} = 2.7 - 3.6V			0.5*V_{CC}	
		V_{CC} = 1.6 - 2.7V			0.4*V_{CC}	
R_{RST}	Reset pin pull-up resistor			25		kΩ

32.3 ATxmega64D4

32.3.1 Absolute Maximum Ratings

Stresses beyond those listed in Table 32-57 under may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 32-57. Absolute Maximum Ratings

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		-0.3		4	V
I_{VCC}	Current into a V_{CC} pin				200	mA
I_{GND}	Current out of a Gnd pin				200	
V_{PIN}	Pin voltage with respect to Gnd and V_{CC}		-0.5		V_{CC}+0.5	V
I_{PIN}	I/O pin sink/source current		-25		25	mA
T_A	Storage temperature		-65		150	°C
T_j	Junction temperature				150	

32.3.2 General Operating Ratings

The device must operate within the ratings listed in Table 32-58 in order for all other electrical characteristics and typical characteristics of the device to be valid.

Table 32-58. General Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		1.60		3.6	V
AV_{CC}	Analog supply voltage		1.60		3.6	
T_A	Temperature range		-40		85	°C
T_j	Junction temperature		-40		105	

Table 32-59. Operating Voltage and Frequency

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{CPU}	CPU clock frequency	V_{CC} = 1.6V	0		12	MHz
		V_{CC} = 1.8V	0		12	
		V_{CC} = 2.7V	0		32	
		V_{CC} = 3.6V	0		32	

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
C_{XTAL1}	Parasitic capacitance XTAL1 pin			5.9		pF
C_{XTAL2}	Parasitic capacitance XTAL2 pin			8.3		
C_{LOAD}	Parasitic capacitance load			3.5		

Note: 1. Numbers for negative impedance are not tested in production but guaranteed from design and characterization.

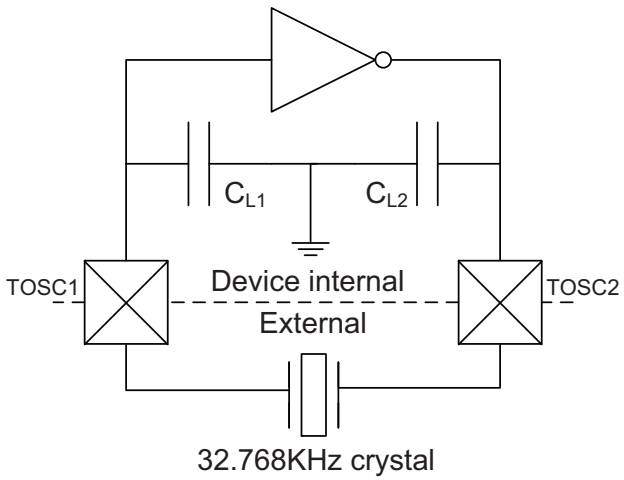
32.3.13.8 External 32.768kHz Crystal Oscillator and TOSC Characteristics

Table 32-83. External 32.768kHz Crystal Oscillator and TOSC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ESR/R1	Recommended crystal equivalent series resistance (ESR)	Crystal load capacitance 6.5pF			60	kΩ
		Crystal load capacitance 9.0pF			35	
C_{TOSC}	Parasitic capacitance	Normal mode		4.7		pF
		Low power mode		5.2		
	Recommended safety factor	Capacitance load matched to crystal specification	3			

Note: 1. See Figure 32-18 on page 118 for definition.

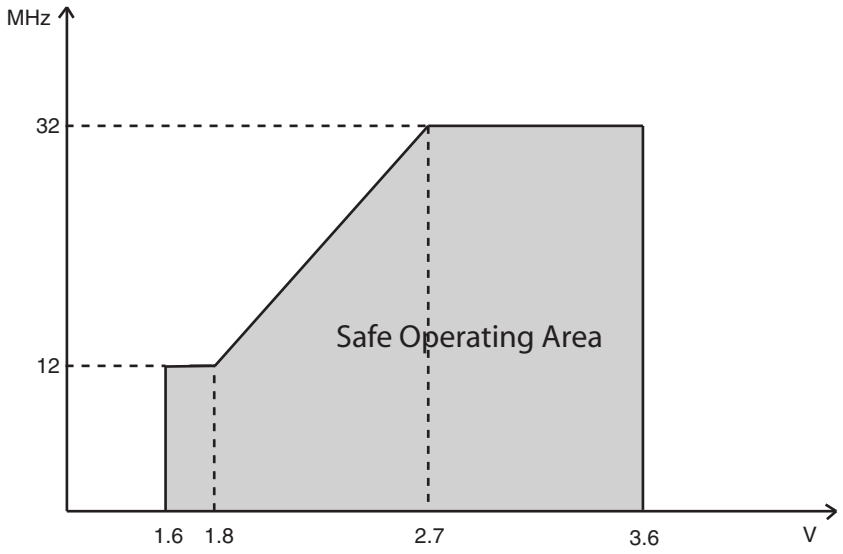
Figure 32-18.TOSC Input Capacitance



The parasitic capacitance between the TOSC pins is C_{L1} + C_{L2} in series as seen from the crystal when oscillating without external capacitors.

The maximum CPU clock frequency depends on V_{CC}. As shown in Figure 32-22 the Frequency vs. V_{CC} curve is linear between 1.8V < V_{CC} < 2.7V.

Figure 32-22.Maximum Frequency vs. V_{CC}



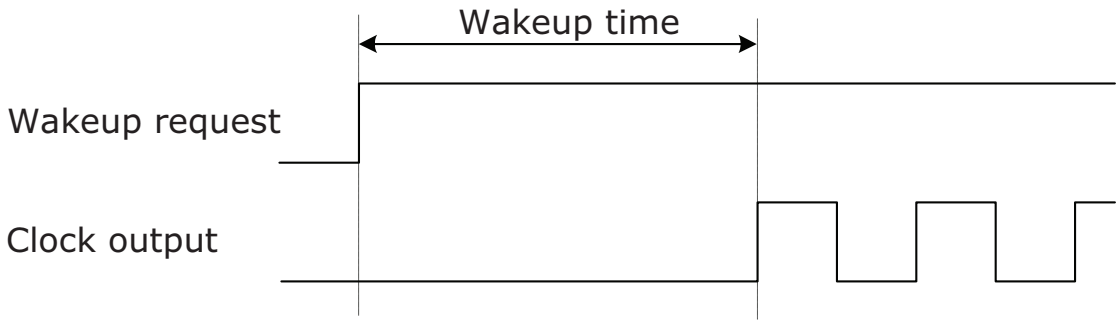
32.4.4 Wake-up Time from Sleep Modes

Table 32-91. Device Wake-up Time from Sleep Modes with Various System Clock Sources

Symbol	Parameter	Condition	Min.	Typ.(1)	Max.	Units
t_{wakeup}	Wake-up time from Idle, Standby, and Extended Standby mode	External 2MHz clock		2.0		µs
		32.768kHz internal oscillator		120		
		2MHz internal oscillator		2.0		
		32MHz internal oscillator		0.2		
	Wake-up time from Power-save and Power-down mode	External 2MHz clock		4.5		
		32.768kHz internal oscillator		320		
		2MHz internal oscillator		9.0		
		32MHz internal oscillator		5.0		

Note: 1. The wake-up time is the time from the wake-up request is given until the peripheral clock is available on pin, see Figure 32-23. All peripherals and modules start execution from the first clock cycle, expect the CPU that is halted for four clock cycles before program execution starts.

Figure 32-23.Wake-up Time Definition



Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
R_Q	Negative impedance[1]	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF	2.4k			Ω
			1MHz crystal, CL=20pF	8.7k			
			2MHz crystal, CL=20pF	2.1k			
		XOSCPWR=0, FRQRANGE=1, CL=20pF	2MHz crystal	4.2k			
			8MHz crystal	250			
			9MHz crystal	195			
		XOSCPWR=0, FRQRANGE=2, CL=20pF	8MHz crystal	360			
			9MHz crystal	285			
			12MHz crystal	155			
		XOSCPWR=0, FRQRANGE=3, CL=20pF	9MHz crystal	365			
			12MHz crystal	200			
			16MHz crystal	105			
		XOSCPWR=1, FRQRANGE=0, CL=20pF	9MHz crystal	435			
			12MHz crystal	235			
			16MHz crystal	125			
		XOSCPWR=1, FRQRANGE=1, CL=20pF	9MHz crystal	495			
			12MHz crystal	270			
			16MHz crystal	145			
		XOSCPWR=1, FRQRANGE=2, CL=20pF	12MHz crystal	305			
			16MHz crystal	160			
		XOSCPWR=1, FRQRANGE=3, CL=20pF	12MHz crystal	380			
			16MHz crystal	205			
	ESR	SF = safety factor				$min(R_Q)/SF$	kΩ
	Start-up time	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF		1.0		ms
		XOSCPWR=0, FRQRANGE=1	2MHz crystal, CL=20pF		2.6		
		XOSCPWR=0, FRQRANGE=2	8MHz crystal, CL=20pF		0.8		
		XOSCPWR=0, FRQRANGE=3	12MHz crystal, CL=20pF		1.0		
		XOSCPWR=1, FRQRANGE=3	16MHz crystal, CL=20pF		1.4		

32.4.15 Two-Wire Interface Characteristics

Table 32-114 describes the requirements for devices connected to the Two-Wire Interface Bus. The Atmel AVR XMEGA Two-Wire Interface meets or exceeds these requirements under the noted conditions. Timing symbols refer to Figure 32-28.

Figure 32-28.Two-wire Interface Bus Timing

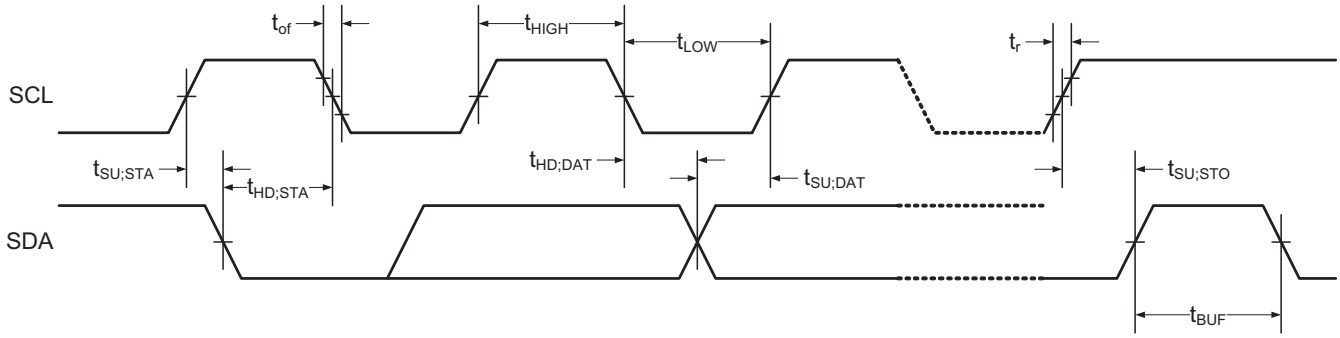


Table 32-114. Two-wire Interface Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input high voltage		$0.7*V_{CC}$		$V_{CC}+0.5$	V
V_{IL}	Input low voltage		-0.5		$0.3*V_{CC}$	
V_{hys}	Hysteresis of Schmitt Trigger Inputs		$0.05*V_{CC}$ (1)			
V_{OL}	Output low voltage	3mA, sink current	0		0.4	
t_r	Rise time for both SDA and SCL		$20+0.1C_b$ (1)(2)		300	ns
t_{of}	Output fall time from V_{IHmin} to V_{ILmax}	$10pF < C_b < 400pF$ (2)	$20+0.1C_b$ (1)(2)		250	
t_{SP}	Spikes suppressed by input filter		0		50	
I_I	Input current for each I/O pin	$0.1V_{CC} < V_I < 0.9V_{CC}$	-10		10	µA
C_I	Capacitance for each I/O pin				10	pF
f_{SCL}	SCL clock frequency	f_{PER} (3)>max($10f_{SCL}$, 250kHz)	0		400	kHz
R_P	Value of pull-up resistor	$f_{SCL} \leq 100kHz$	$\frac{V_{CC}-0.4V}{3mA}$		$\frac{100ns}{C_b}$	Ω
		$f_{SCL} > 100kHz$			$\frac{300ns}{C_b}$	

Figure 33-37. INL Error vs. Sample Rate

T = 25°C, V_{CC} = 3.6V, V_{REF} = 3.0V external

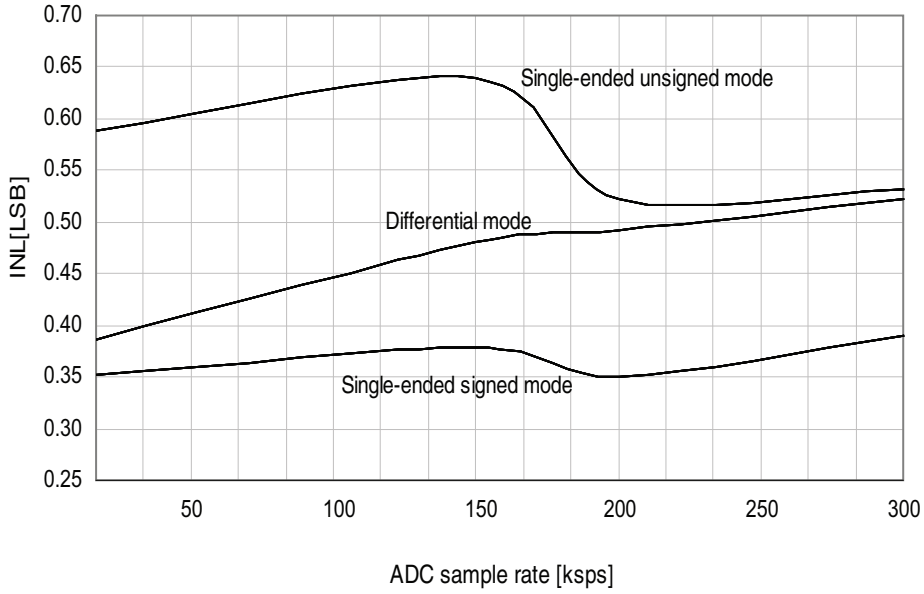


Figure 33-38. INL Error vs. Input Code

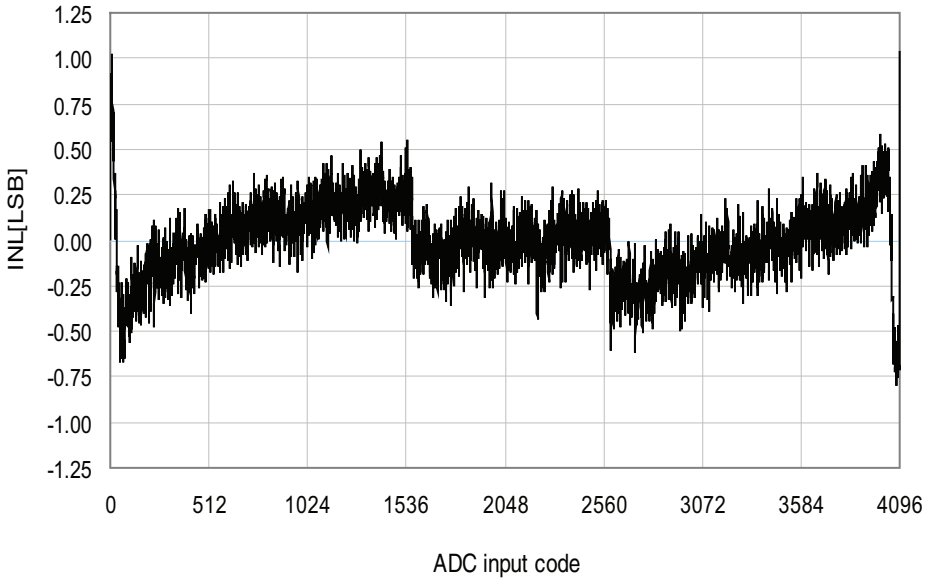


Figure 33-45. Gain Error vs. Temperature

V_{CC} = 3.0V, V_{REF} = external 2.0V

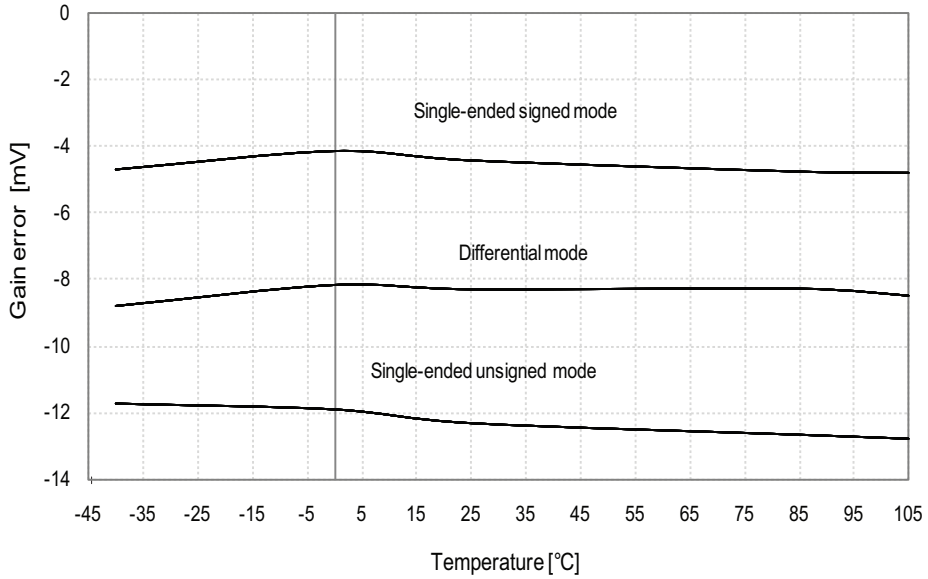


Figure 33-46. Offset Error vs. V_{CC}

T = 25°C, V_{REF} = external 1.0V, ADC sample rate = 200ksps

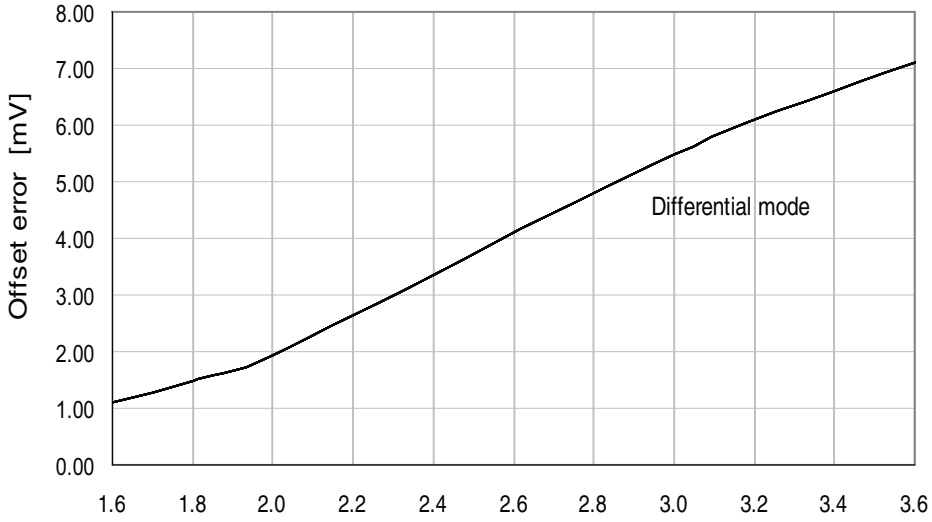


Figure 33-124. Offset Error vs. V_{REF}

T = 25°C, V_{CC} = 3.6V, ADC sample rate = 200ksps

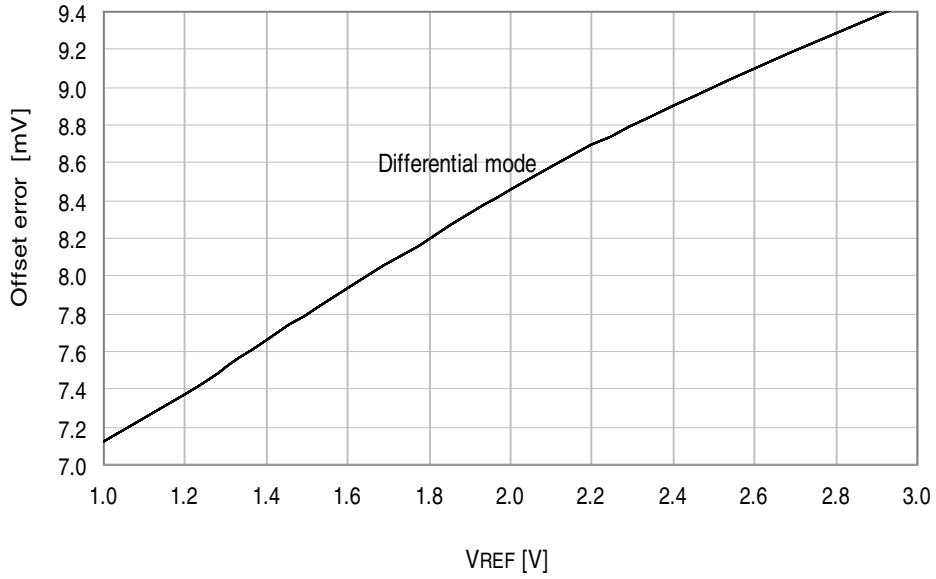


Figure 33-125. Offset Error vs. V_{CC}

T = 25°C, V_{REF} = external 1.0V, ADC sample rate = 200ksps

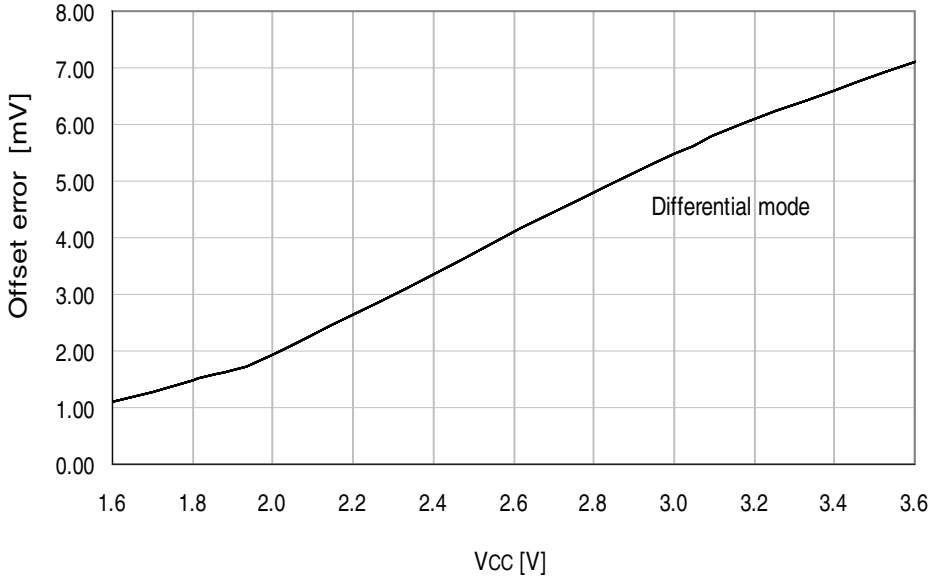
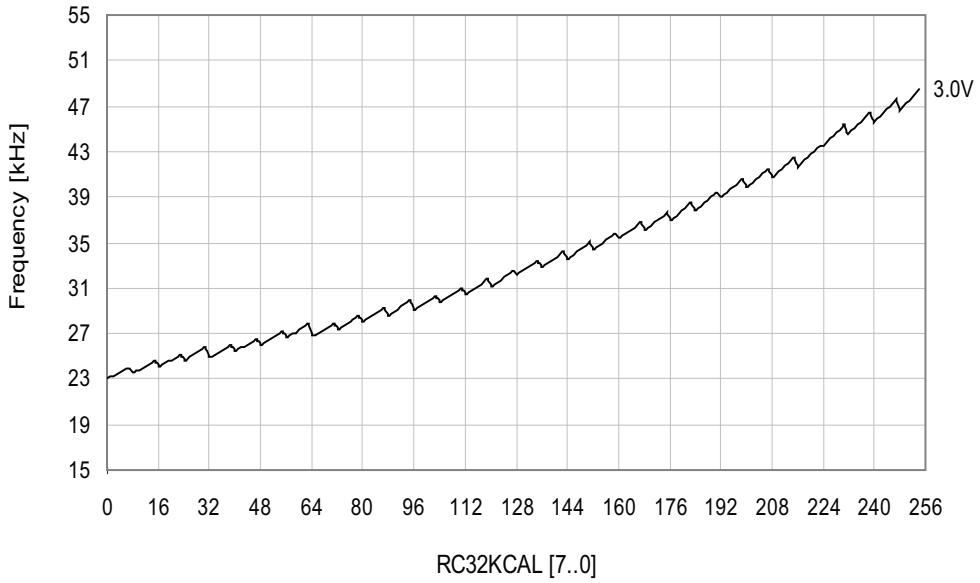


Figure 33-146. 32.768kHz Internal Oscillator Frequency vs. Calibration Value

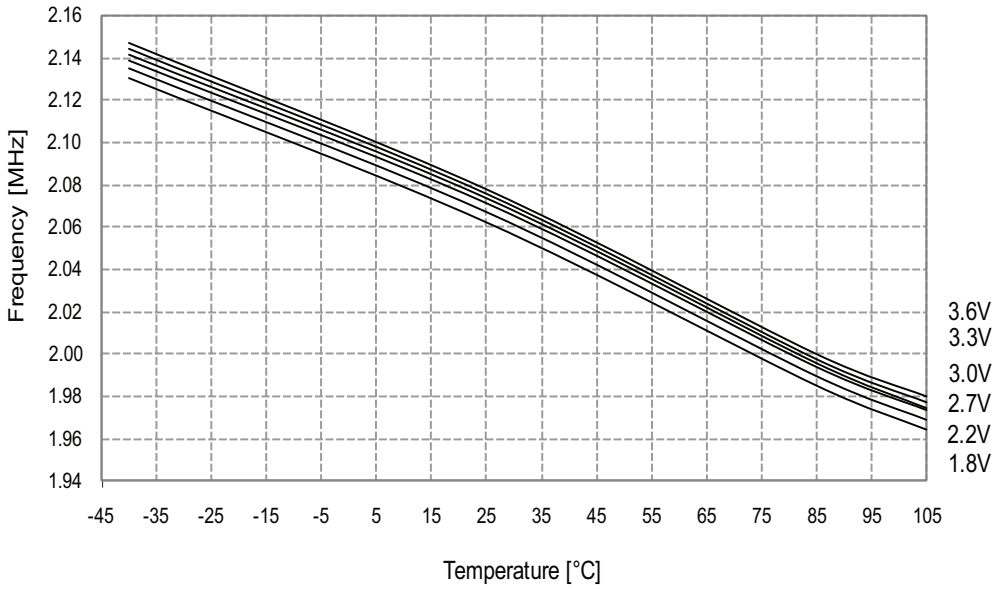
V_{CC} = 3.0V, T = 25°C



33.2.9.3 2MHz Internal Oscillator

Figure 33-147. 2MHz Internal Oscillator Frequency vs. Temperature

DFLL disabled



33.4 ATxmega128D4

33.4.1 Current Consumption

33.4.1.1 Active Mode Supply Current

Figure 33-243. Active Supply Current vs. Frequency

f_{SYS} = 0 - 1MHz external clock, T = 25°C

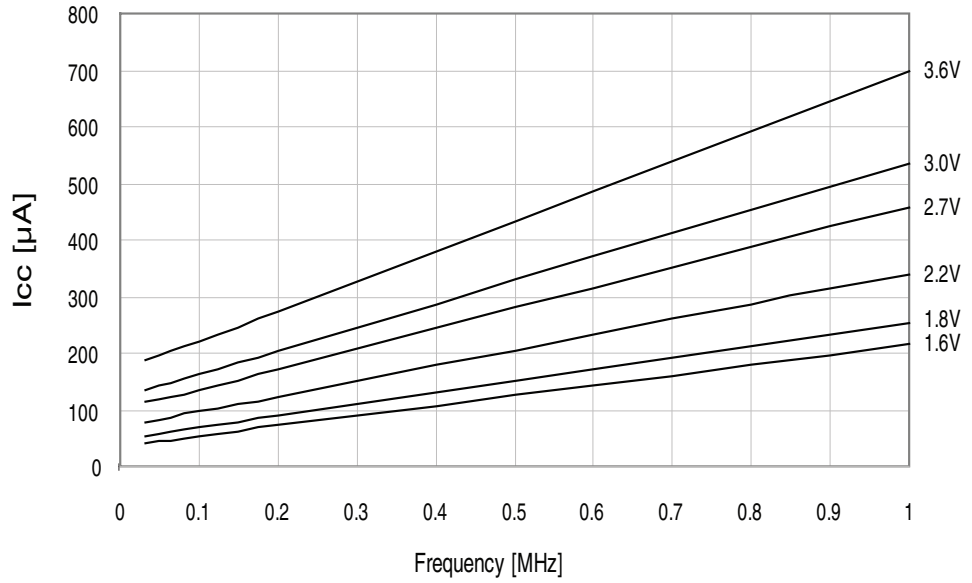
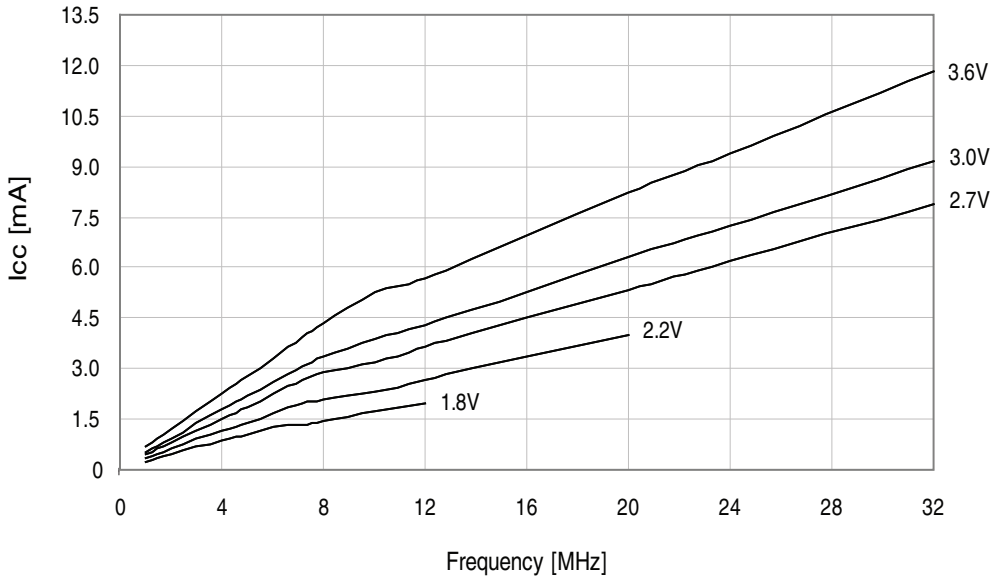


Figure 33-244. Active Supply Current vs. Frequency

f_{SYS} = 1 - 32MHz external clock, T = 25°C



33.4.2 I/O Pin Characteristics

33.4.2.1 Pull-up

Figure 33-263. I/O Pin Pull-up Resistor Current vs. Input Voltage

V_{CC} = *1.8V*

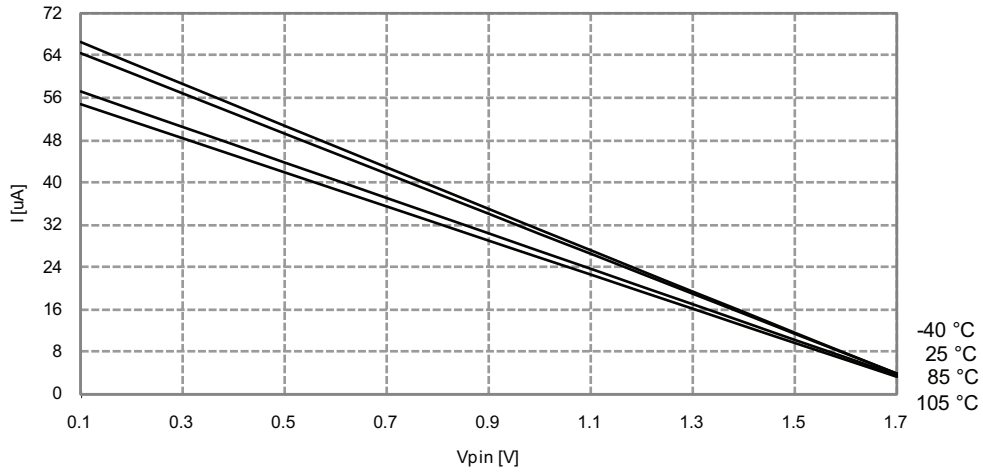


Figure 33-264. I/O Pin Pull-up Resistor Current vs. Input Voltage

V_{CC} = *3.0V*

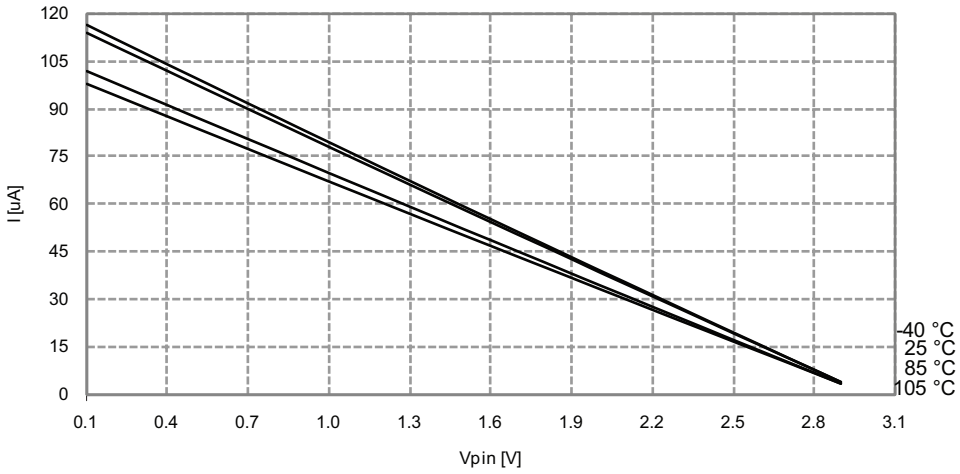


Figure 33-267. I/O Pin Output Voltage vs. Source Current

V_{CC} = 3.0V

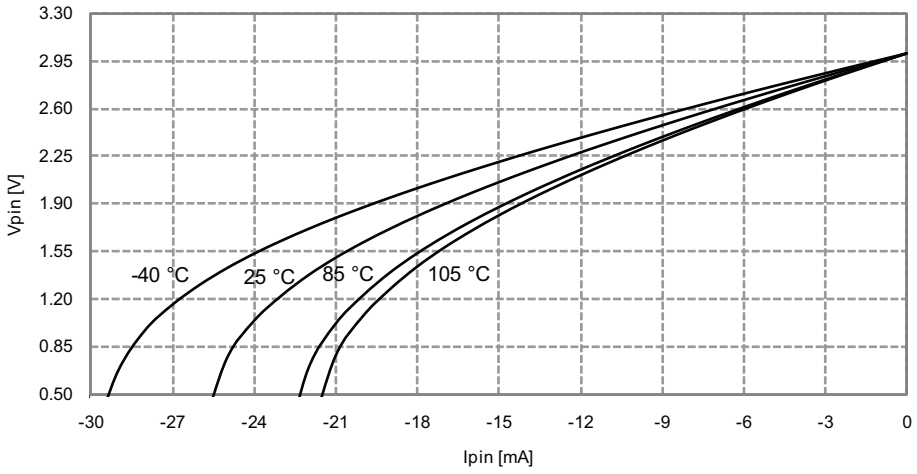


Figure 33-268. I/O Pin Output Voltage vs. Source Current

V_{CC} = 3.3V

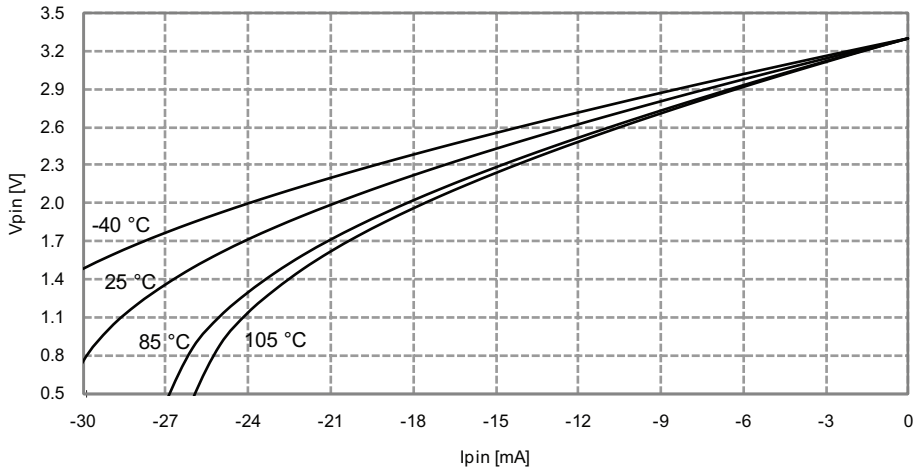


Figure 33-279. INL Error vs. Sample rate

T = 25°C, V_{CC} = 3.6V, V_{REF} = 3.0V external

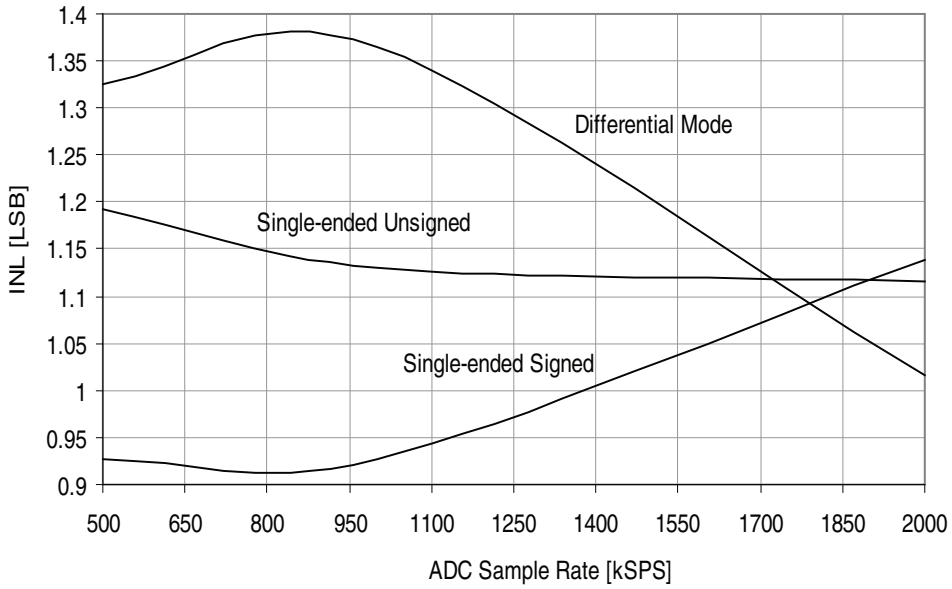
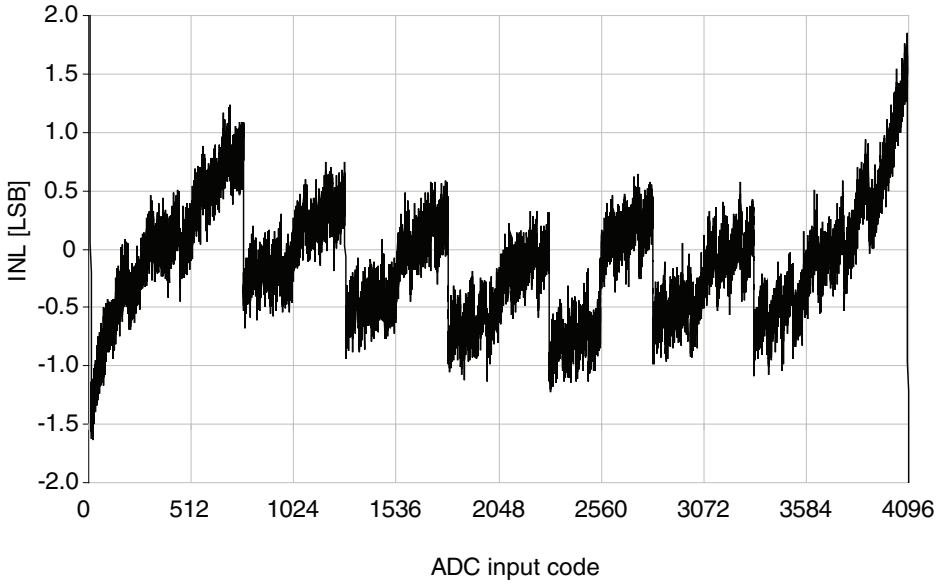


Figure 33-280. INL Error vs. Input code



33.4.4 DAC Characteristics

Figure 33-291. DAC INL Error vs. V_{REF}

V_{CC} = 3.6V

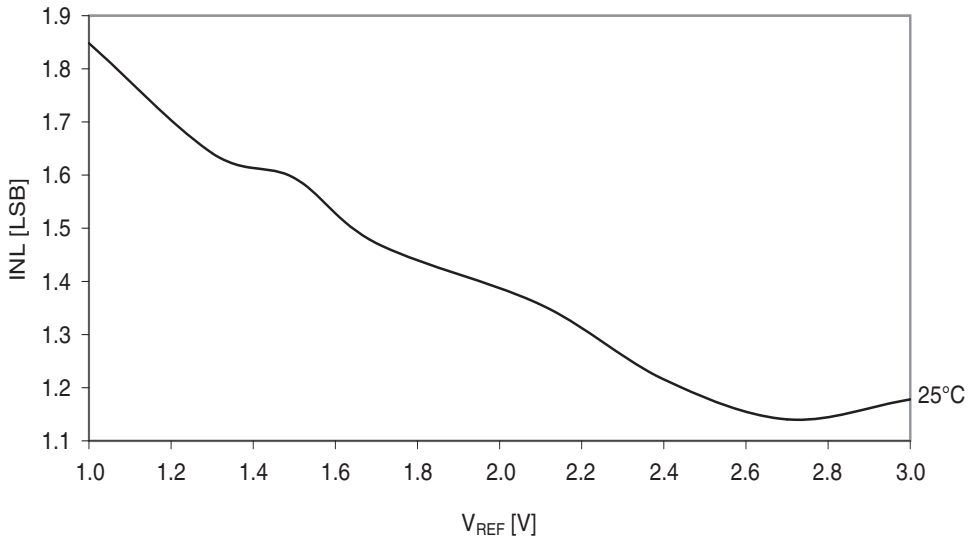
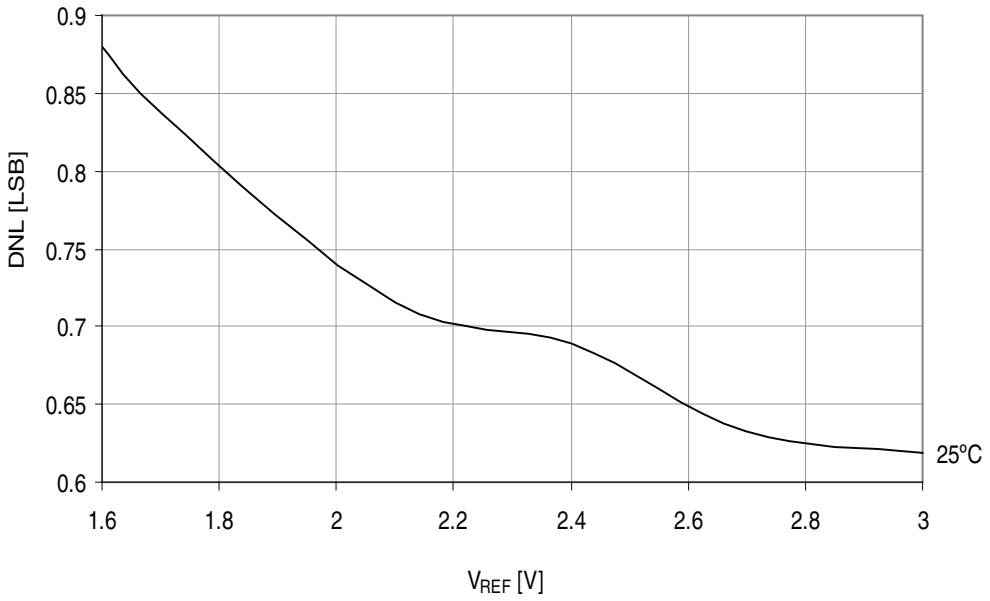


Figure 33-292. DNL Error vs. V_{REF}

T = 25°C, V_{CC} = 3.6V



Problem fix/Workaround

Configure the analog comparator setup to give an inverted result, or use an external inverter to change polarity of Analog Comparator Output.

27. Non available functions and options

The below function and options are not available. Writing to any registers or fuse to try and enable or configure these functions or options will have no effect, and will be as writing to a reserved address location.

- TWIE, the TWI module on PORTE.
- TWI SDAHOLD option in the TWI CTRL register is one bit.
- CRC generator module.
- ADC 1/2x gain option, and this configuration option in the GAIN bits in the ADC Channel CTRL register.
- ADC V_{CC}/2 reference option and this configuration option in the REFSEL bits on the ADC REFCTRL register.
- ADC option to use internal Gnd as negative input in differential measurements and this configuration option in the MUXNEG bits in the ADC Channel MUXCTRL register.
- ADC channel scan and the ADC SCAN register
- ADC current limitation option, and the CURRLIMIT bits in the ADC CTRLB register
- ADC impedance mode selection for the gain stage, and the IMPMODE bit in the ADC CTRLB register.
- Timer/Counter 2 and the SPLITMODE configuration option in the BYTEM bits in the Timer/Counter 0 CTRLE register.
- Analog Comparator (AC) current output option, and the AC CURRCTRL and CURRCALIB registers.
- PORT remap functions with alternate pin locations for Timer/Counter output compare channels, USART0 and SPI, and the PORT REMAP register.
- PORT RTC clock output option and the RTCOUT bit in the PORT CLKEVOUT register.
- PORT remap functions with alternate pin locations for the clock and event output, and the CLKEVPIN bit in the PORT CLKEVOUT register.
- TOSC alternate pin locations, and TOSCSEL bit in FUSEBYTE2
- Real Time Counter clock source options of external clock from TOSC1, and 32.768kHz from TOSC, and 32.768kHz from the 32.768kHz internal oscillator, and these configuration options in the RTCSRC bits in the Clock RTCTRL register.
- PLL divide by two option, and the PLLDIV bit in the Clock PLLCTRL register.
- PLL lock detection failure function and the PLLDIF and PLLFDEN bits in the Clock XOSCFAIL register.
- The high drive option for external crystal and the XOSCPWR bit on the Oscillator XOSCCTRL register.
- The option to enable sequential startup of the analog modules and the ANAINIT register in MCU Control memory.

Problem fix/Workaround

None.

28. Temperature sensor not calibrated

Temperature sensor factory calibration not implemented.

Problem fix/Workaround

None.

29. Disabling of USART transmitter does not automatically set the TxD pin direction to input

If the USART transmitter is idle with no frames to transmit, setting TXEN to zero will not automatically set the TxD pin direction to input.

Problem fix/Workaround

The TxD pin direction can be set to input using the Port DIR register. Be advised that setting the Port DIR register to input will be immediate. Ongoing transmissions will be truncated.