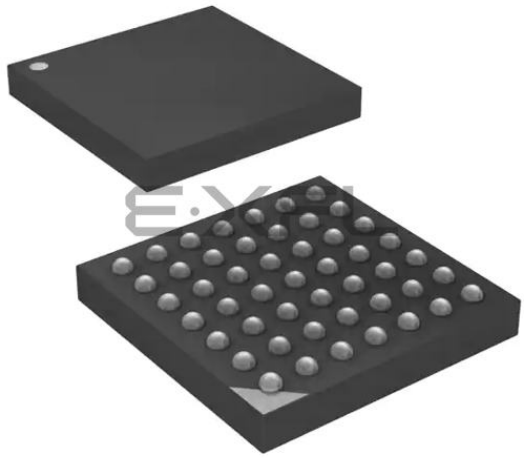

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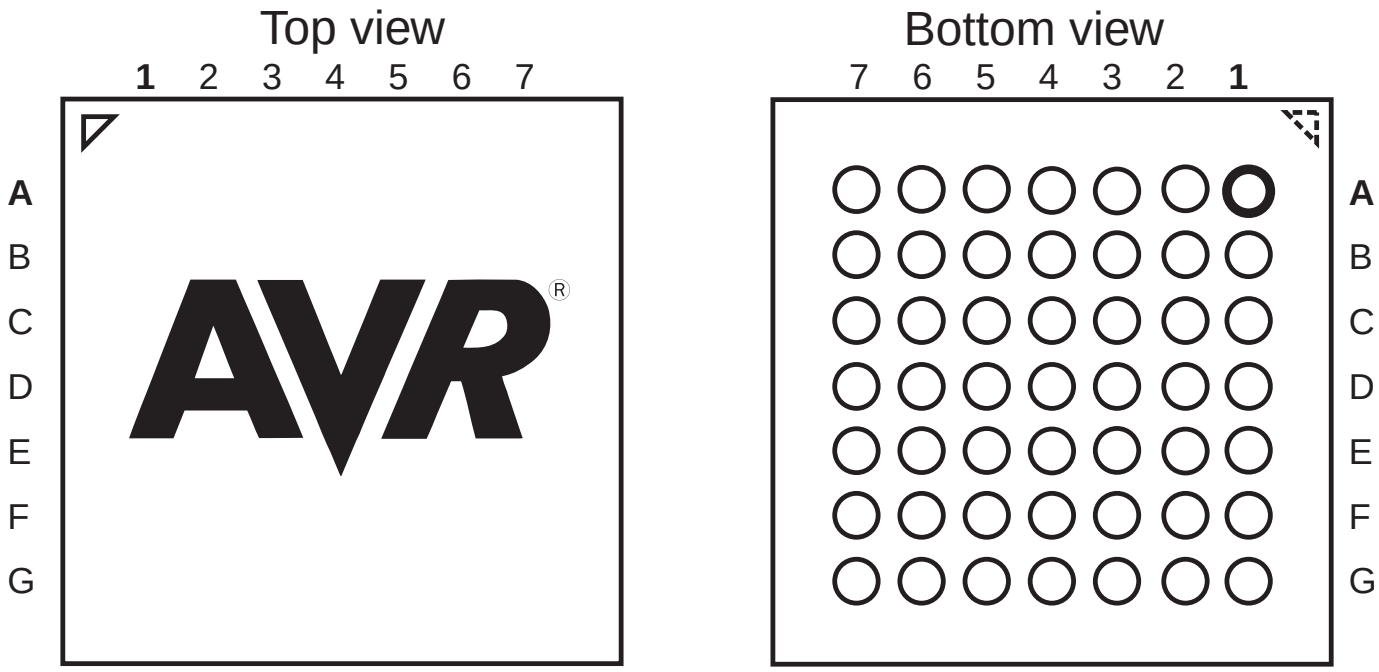
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	49-VFBGA
Supplier Device Package	49-VFBGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega32d4-cu

Figure 2-2. VFBGA Pinout



	1	2	3	4	5	6	7
A	PA3	AVCC	GND	PR1	PR0	PDI	PE3
B	PA4	PA1	PA0	GND	$\overline{\text{RESET}}$/PDI_CLK	PE2	VCC
C	PA5	PA2	PA6	PA7	GND	PE1	GND
D	PB1	PB2	PB3	PB0	GND	PD7	PE0
E	GND	GND	PC3	GND	PD4	PD5	PD6
F	VCC	PC0	PC4	PC6	PD0	PD1	PD3
G	PC1	PC2	PC5	PC7	GND	VCC	PD2

18. Hi-Res – High Resolution Extension

18.1 Features

- Increases waveform generator resolution up to 8x (three bits)
- Supports frequency, single-slope PWM, and dual-slope PWM generation
- Supports the AWeX when this is used for the same timer/counter

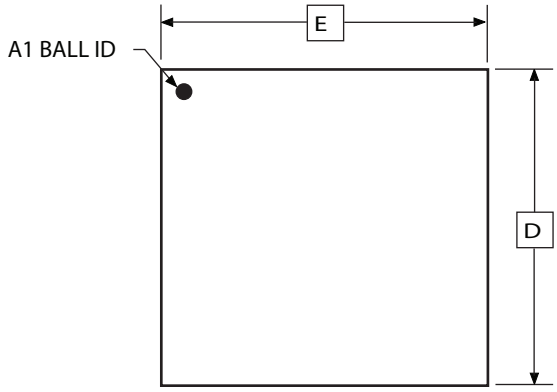
18.2 Overview

The high-resolution (hi-res) extension can be used to increase the resolution of the waveform generation output from a timer/counter by four or eight. It can be used for a timer/counter doing frequency, single-slope PWM, or dual-slope PWM generation. It can also be used with the AWeX if this is used for the same timer/counter.

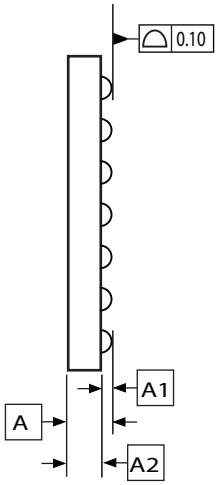
The hi-res extension uses the peripheral 4x clock (Clk_{PER4}). The system clock prescalers must be configured so the peripheral 4x clock frequency is four times higher than the peripheral and CPU clock frequency when the hi-res extension is enabled.

There is one hi-res extension that can be enabled for each timer/counter on PORTC. The notation of this is HIRESC.

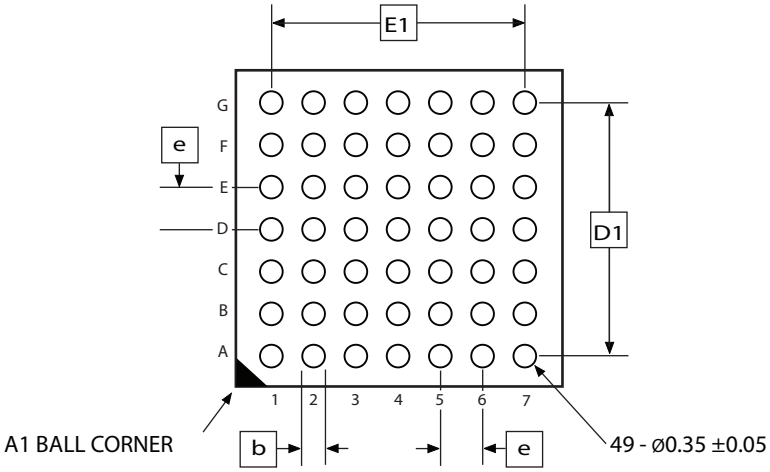
31.3 49C2



TOP VIEW



SIDE VIEW



BOTTOM VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.00	
A1	0.20	–	–	
A2	0.65	–	–	
D	4.90	5.00	5.10	
D1		3.90 BSC		
E4.90	5.00	5.10		
E1		3.90 BSC		
b	0.30	0.35	0.40	
e		0.65 BSC		

3/14/08

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE 49C2, 49-ball (7 x 7 array), 0.65mm pitch, 5.0 x 5.0 x 1.0mm, very thin, fine-pitch ball grid array package (VFBGA)	GPC CBD	DRAWING NO. 49C2	REV. A

32.1.13.7 External 16MHz Crystal Oscillator and XOSC Characteristics

Table 32-25. External 16MHz Crystal Oscillator and XOSC Characteristics

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Cycle to cycle jitter	XOSCPWR=0	FRQRANGE=0		0		ns
			FRQRANGE=1, 2, or 3		0		
		XOSCPWR=1			0		
	Long term jitter	XOSCPWR=0	FRQRANGE=0		0		
			FRQRANGE=1, 2, or 3		0		
		XOSCPWR=1			0		
	Frequency error	XOSCPWR=0	FRQRANGE=0		0.03		%
			FRQRANGE=1		0.03		
			FRQRANGE=2 or 3		0.03		
		XOSCPWR=1			0.003		
	Duty cycle	XOSCPWR=0	FRQRANGE=0		50		
			FRQRANGE=1		50		
			FRQRANGE=2 or 3		50		
		XOSCPWR=1			50		
R_Q	Negative impedance	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF		44k		Ω
			1MHz crystal, CL=20pF		67k		
			2MHz crystal, CL=20pF		67k		
		XOSCPWR=0, FRQRANGE=1, CL=20pF	2MHz crystal		82k		
			8MHz crystal		1500		
			9MHz crystal		1500		
		XOSCPWR=0, FRQRANGE=2, CL=20pF	8MHz crystal		2700		
			9MHz crystal		2700		
			12MHz crystal		1000		
		XOSCPWR=0, FRQRANGE=3, CL=20pF	9MHz crystal		3600		
			12MHz crystal		1300		
			16MHz crystal		590		
		XOSCPWR=1, FRQRANGE=0, CL=20pF	9MHz crystal		390		
			12MHz crystal		50		
			16MHz crystal		10		

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
R_Q	Negative impedance	XOSCPWR=1, FRQRANGE=1, CL=20pF	9MHz crystal		1500		Ω
			12MHz crystal		650		
			16MHz crystal		270		
		XOSCPWR=1, FRQRANGE=2, CL=20pF	12MHz crystal		1000		
			16MHz crystal		440		
		XOSCPWR=1, FRQRANGE=3, CL=20pF	12MHz crystal		1300		
			16MHz crystal		590		
	ESR	SF = safety factor				min(R_Q)/SF	kΩ
	Start-up time	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF		1.0		ms
		XOSCPWR=0, FRQRANGE=1	2MHz crystal, CL=20pF		2.6		
		XOSCPWR=0, FRQRANGE=2	8MHz crystal, CL=20pF		0.8		
		XOSCPWR=0, FRQRANGE=3	12MHz crystal, CL=20pF		1.0		
		XOSCPWR=1, FRQRANGE=3	16MHz crystal, CL=20pF		1.4		
C_{XTAL1}	Parasitic capacitance XTAL1 pin				5.9		pF
C_{XTAL2}	Parasitic capacitance XTAL2 pin				8.3		
C_{LOAD}	Parasitic capacitance load				3.5		

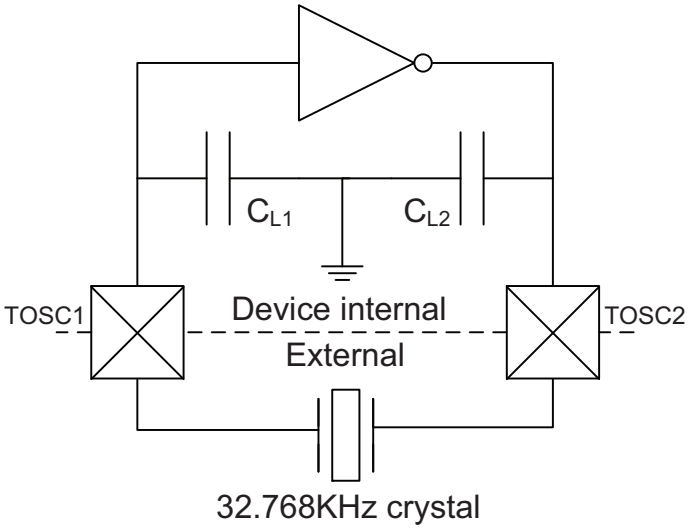
32.1.13.8 External 32.768kHz Crystal Oscillator and TOSC Characteristics

Table 32-26. External 32.768kHz Crystal Oscillator and TOSC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ESR/R1	Recommended crystal equivalent series resistance (ESR)	Crystal load capacitance 6.5pF			60	kΩ
		Crystal load capacitance 9.0pF			35	
		Crystal load capacitance 12pF			28	
C_{TOSC1}	Parasitic capacitance TOSC1 pin			3.5		pF
C_{TOSC2}	Parasitic capacitance TOSC2 pin			3.5		
	Recommended safety factor	capacitance load matched to crystal specification	3			

Note: See Figure 32-4 for definition.

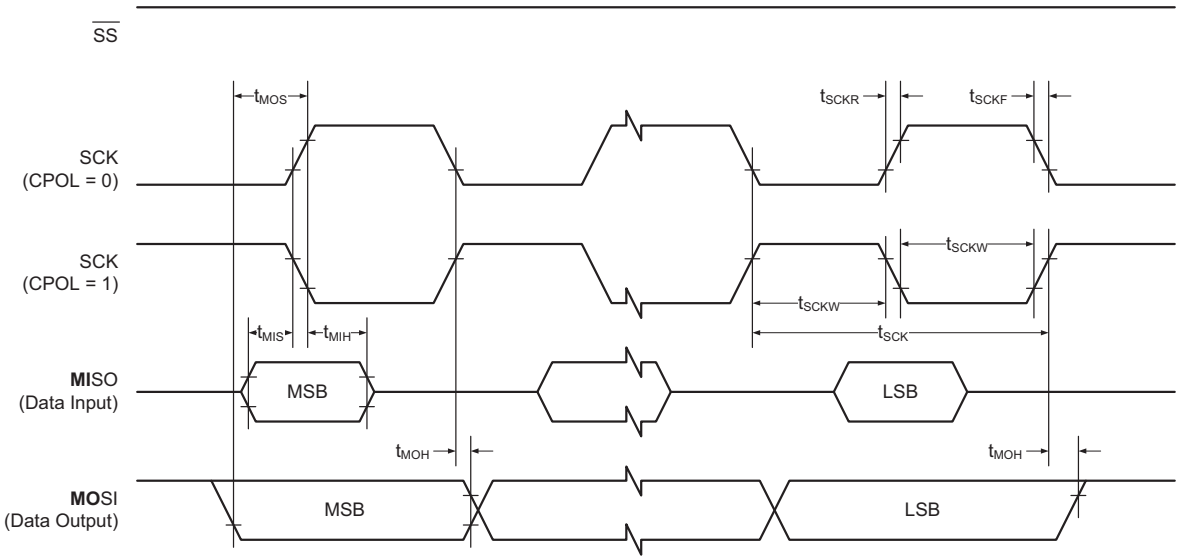
Figure 32-4. TOSC Input Capacitance



The parasitic capacitance between the TOSC pins is C_{L1} + C_{L2} in series as seen from the crystal when oscillating without external capacitors.

32.1.14 SPI Characteristics

Figure 32-5. SPI Timing Requirements in Master Mode



32.4.3 Current Consumption

Table 32-89. Current Consumption for Active Mode and Sleep Modes

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{CC}	Active power consumption[1]	32kHz, Ext. Clk	V_{CC} = 1.8V		55		µA
			V_{CC} = 3.0V		135		
		1MHz, Ext. Clk	V_{CC} = 1.8V		255		
			V_{CC} = 3.0V		535		
		2MHz, Ext. Clk	V_{CC} = 1.8V		460	600	
			V_{CC} = 3.0V		1.0	1.4	mA
		32MHz, Ext. Clk			9.5	12	
	Idle power consumption[1]	32kHz, Ext. Clk	V_{CC} = 1.8V		2.9		µA
			V_{CC} = 3.0V		3.9		
		1MHz, Ext. Clk	V_{CC} = 1.8V		62		
			V_{CC} = 3.0V		118		
		2MHz, Ext. Clk	V_{CC} = 1.8V		125	225	
			V_{CC} = 3.0V		240	350	
		32MHz, Ext. Clk			3.8	5.5	mA
	Power-down power consumption	T = 25°C	V_{CC} = 3.0V		0.1	1.0	µA
		T = 85°C			1.5	4.5	
		T = 105°C			0.1	8.6	
		WDT and sampled BOD enabled, T = 25°C	V_{CC} = 3.0V		1.4	3.0	
		WDT and sampled BOD enabled, T = 85°C			2.8	6.0	
		WDT and sampled BOD enabled, T = 105°C			1.4	8.8	
	Power-save power consumption[2]	RTC from ULP clock, WDT and sampled BOD enabled, T = 25°C	V_{CC} = 1.8V		1.2		
			V_{CC} = 3.0V		1.5		
		RTC from 1.024kHz low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.6	2.0	
			V_{CC} = 3.0V		0.7	2.0	
		RTC from low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.8	3.0	
			V_{CC} = 3.0V		1.0	3.0	
	Reset power consumption	Current through $\overline{\text{RESET}}$ pin substracted	V_{CC} = 3.0V		300		

Notes:
1. All Power Reduction Registers set.
2. Maximum limits are based on characterization, and not tested in production.

32.4.6 ADC Characteristics

Table 32-93. Power Supply, Reference and Input Range

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
AV_{CC}	Analog supply voltage		V_{CC}- 0.3		V_{CC}+ 0.3	V
V_{REF}	Reference voltage		1.0		AV_{CC}- 0.6	
R_{in}	Input resistance	Switched		4.0		kΩ
C_{sample}	Input capacitance	Switched		4.4		pF
R_{AREF}	Reference input resistance	(leakage only)		>10		MΩ
C_{AREF}	Reference input capacitance	Static load		7.0		pF
V_{IN}	Input range		-0.1		AV_{CC}+0.1	V
	Conversion range	Differential mode, Vinp - Vinn	$-V_{REF}$		V_{REF}	
	Conversion range	Single ended unsigned mode, Vinp	-ΔV		V_{REF}-ΔV	
ΔV	Fixed offset voltage			190		lsb

Table 32-94. Clock and Timing

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{ADC}	ADC clock frequency	Maximum is 1/4 of Peripheral clock frequency	100		1400	kHz
		Measuring internal signals	100		125	
f_{ADC}	Sample rate	Current limitation (CURRLIMIT) off	14		200	ksps
		CURRLIMIT = LOW	14		150	
		CURRLIMIT = MEDIUM	14		100	
		CURRLIMIT = HIGH			50	
	Sampling time	1/2 Clk_{ADC} cycle	0.25		5	µs
	Conversion time (latency)	(RES+2)/2+GAIN RES = 8 or 12, GAIN = 0, 1, 2 or 3	5	7	10	Clk_{ADC} cycles
	Start-up time	ADC clock cycles		12	24	Clk_{ADC} cycles
	ADC settling time	After changing reference or input mode		7	7	
		After ADC flush		1	1	

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
t_{delay}	Propagation delay	V_{CC} = 3.0V, T= 85°C	mode = HS		30	90	ns
					30		
	64-Level voltage scaler	Integral non-linearity (INL)			0.3	0.5	lsb

32.4.8 Bandgap and Internal 1.0V Reference Characteristics

Table 32-98. Bandgap and Internal 1.0V Reference Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Startup time	As reference for ADC		1 Clk_{PER} + 2.5µs		µs
		As input voltage to ADC and AC		1.5		
	Bandgap voltage			1.1		V
INT1V	Internal 1.00V reference	T= 85°C, after calibration	0.99	1.0	1.01	
	Variation over voltage and temperature	Relative to T= 85°C, V_{CC} = 3.0V		±1.5		%

32.4.9 Brownout Detection Characteristics

Table 32-99. Brownout Detection Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{BOT}	BOD level 0 falling V_{CC}		1.60	1.62	1.72	V
	BOD level 1 falling V_{CC}			1.8		
	BOD level 2 falling V_{CC}			2.0		
	BOD level 3 falling V_{CC}			2.2		
	BOD level 4 falling V_{CC}			2.4		
	BOD level 5 falling V_{CC}			2.6		
	BOD level 6 falling V_{CC}			2.8		
	BOD level 7 falling V_{CC}			3.0		
t_{BOD}	Detection time	Continuous mode		0.4		µs
		Sampled mode		1000		
V_{HYST}	Hysteresis			1.2		%

33.2 ATxmega32D4

33.2.1 Current Consumption

33.2.1.1 Active Mode Supply Current

Figure 33-80. Active Supply Current vs. Frequency

f_{SYS} = 0 - 1MHz external clock, T = 25°C

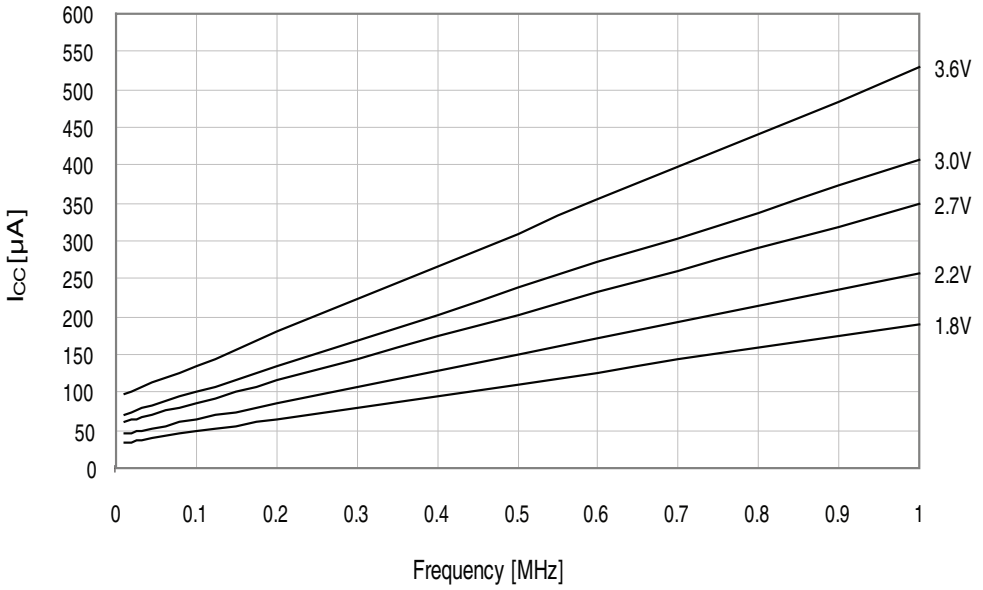


Figure 33-81. Active Supply Current vs. Frequency

f_{SYS} = 1 - 32MHz external clock, T = 25°C

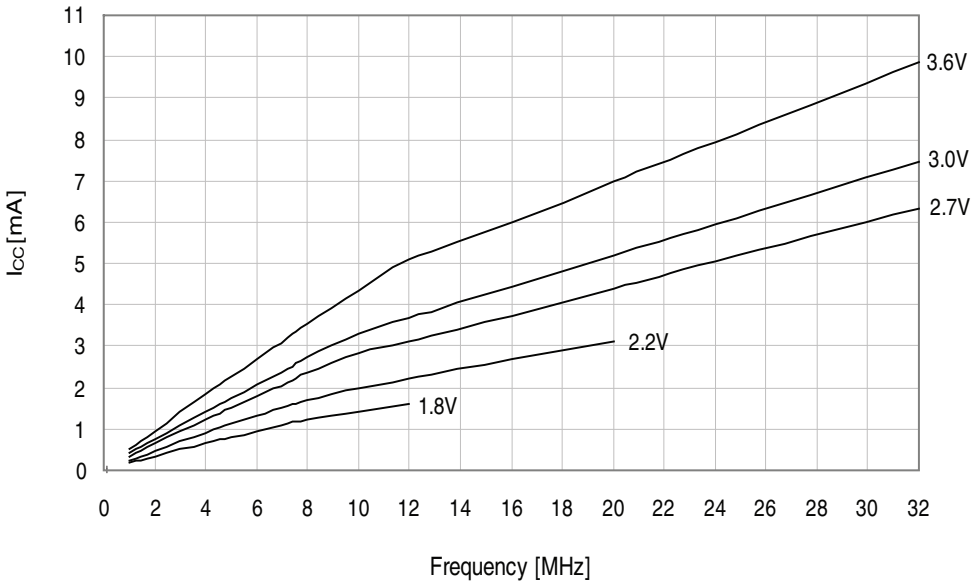


Figure 33-104. I/O Pin Output Voltage vs. Source Current

V_{CC} = 3.0V

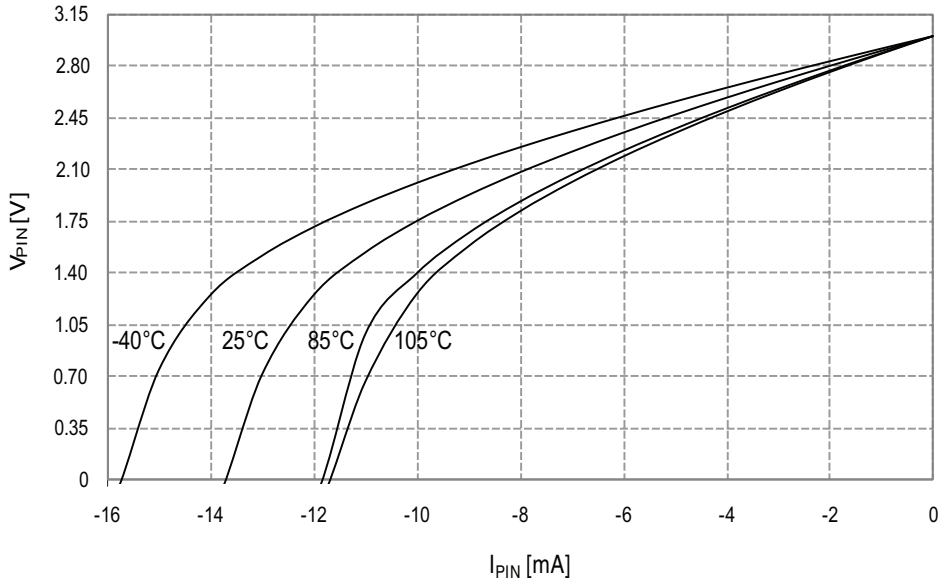


Figure 33-105. I/O Pin Output Voltage vs. Source Current

V_{CC} = 3.3V

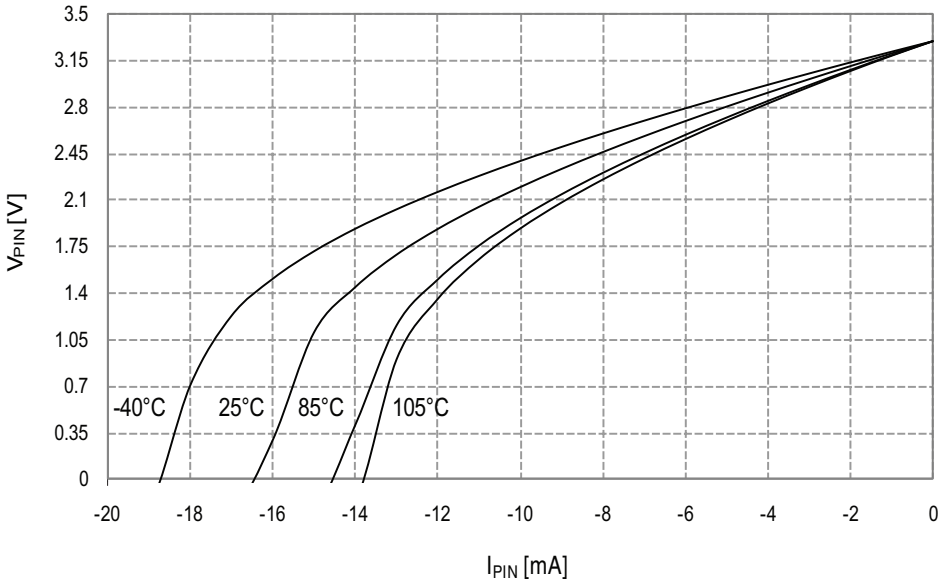


Figure 33-120. DNL Error vs. Input code

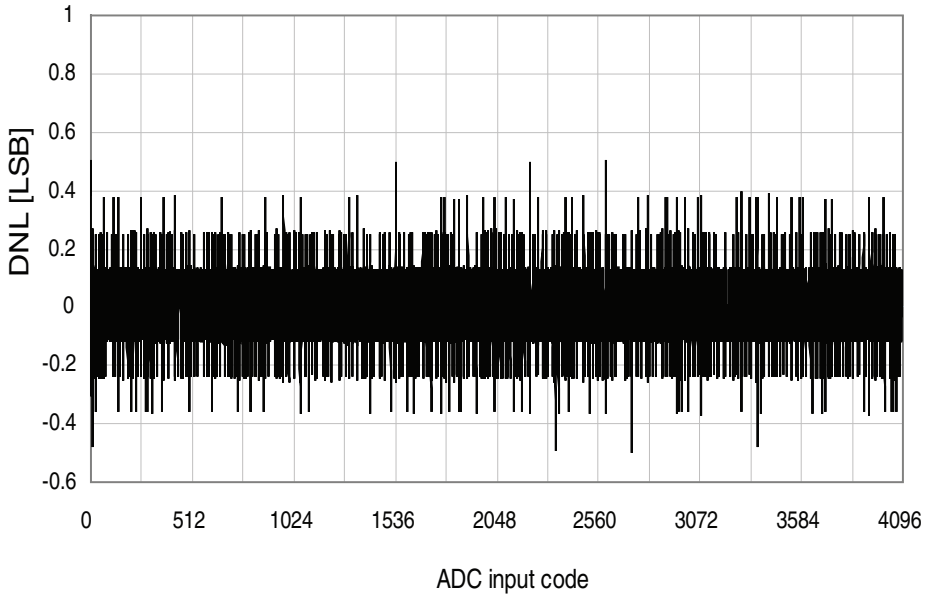
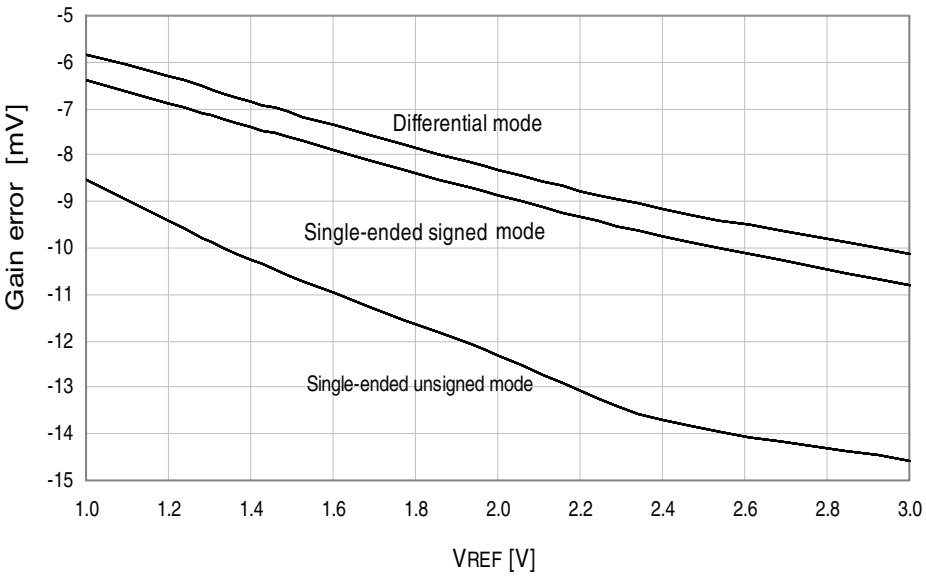


Figure 33-121. Gain Error vs. V_{REF}

T = 25°C, V_{CC} = 3.6V, ADC sample rate = 200ksps



33.2.9.4 32MHz Internal Oscillator

Figure 33-150. 32MHz Internal Oscillator Frequency vs. Temperature

DFLL disabled

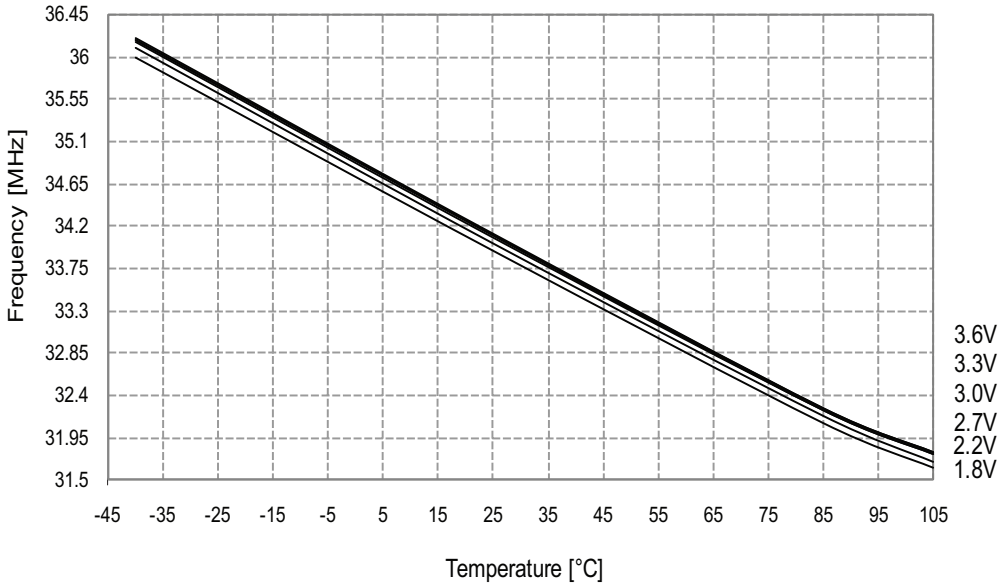


Figure 33-151. 32MHz Internal Oscillator Frequency vs. Temperature

DFLL enabled, from the 32.768kHz internal oscillator

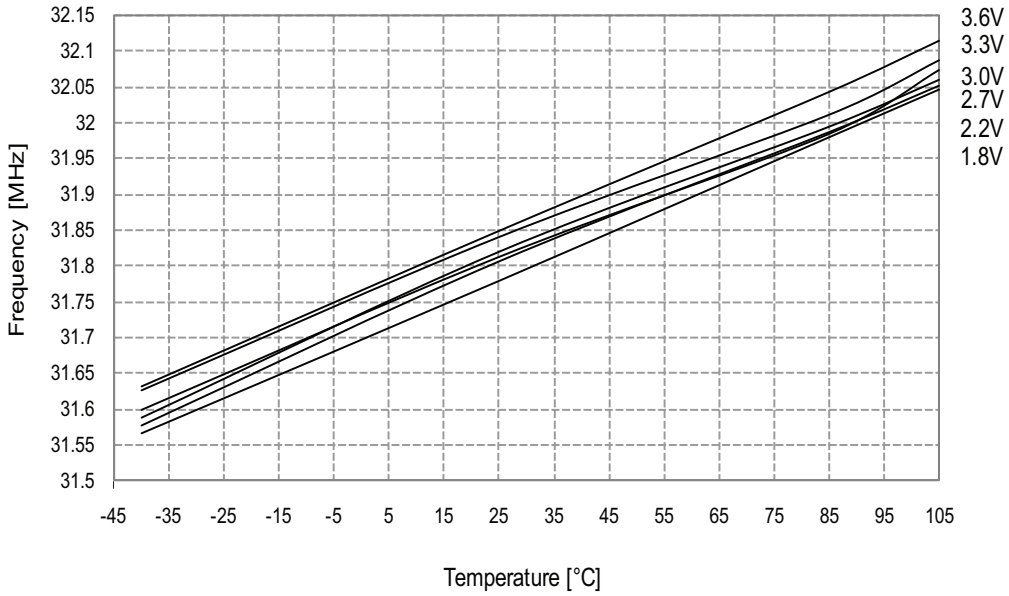
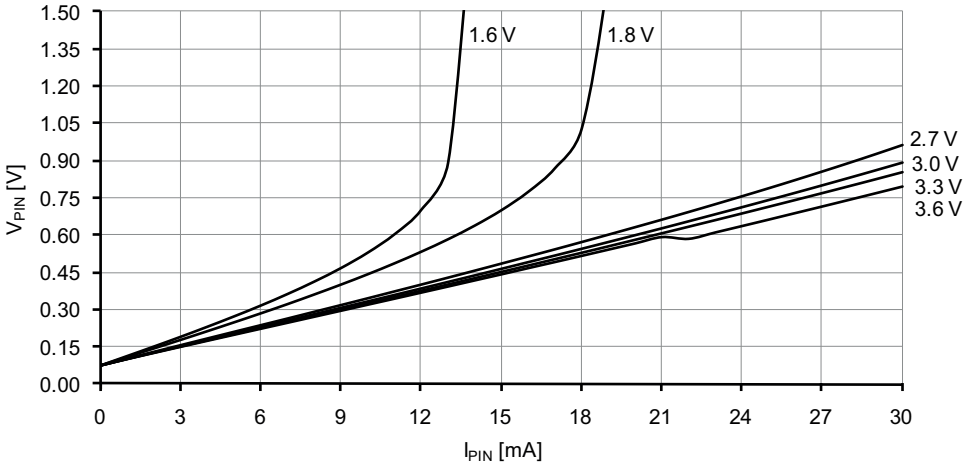


Figure 33-189. I/O Pin Output Voltage vs. Sink Current



33.3.2.3 Thresholds and Hysteresis

Figure 33-190. I/O Pin Input Threshold Voltage vs. V_{CC}

T = 25°C

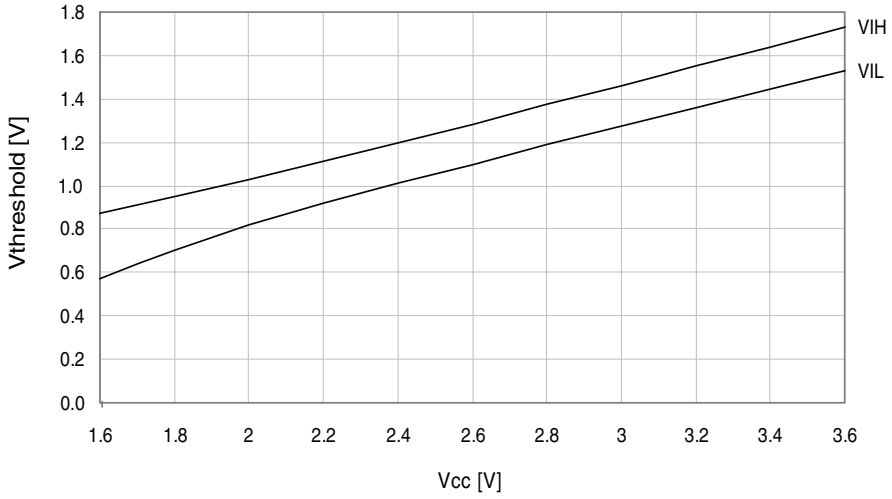


Figure 33-289. Noise vs. V_{REF}

T = 25°C, V_{CC} = 3.6V, ADC sampling speed = 500ksps

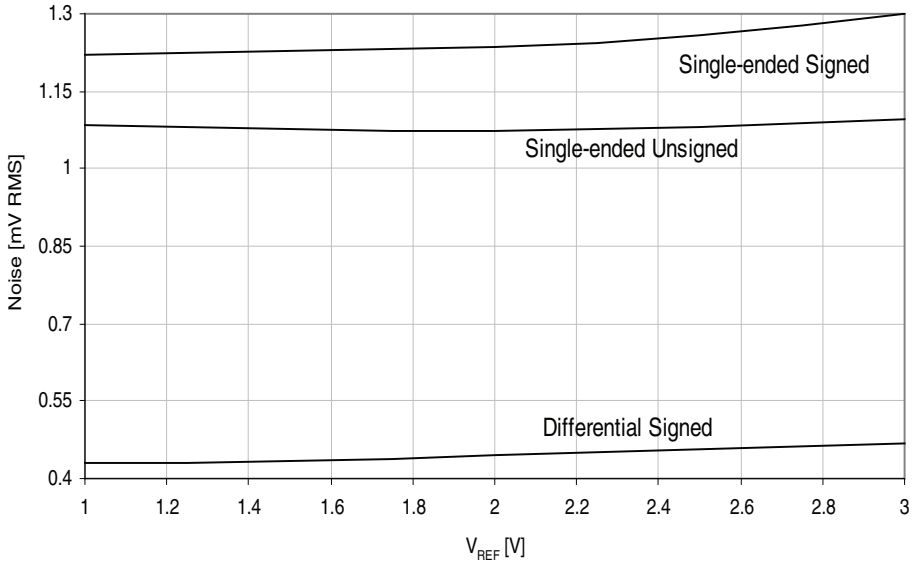
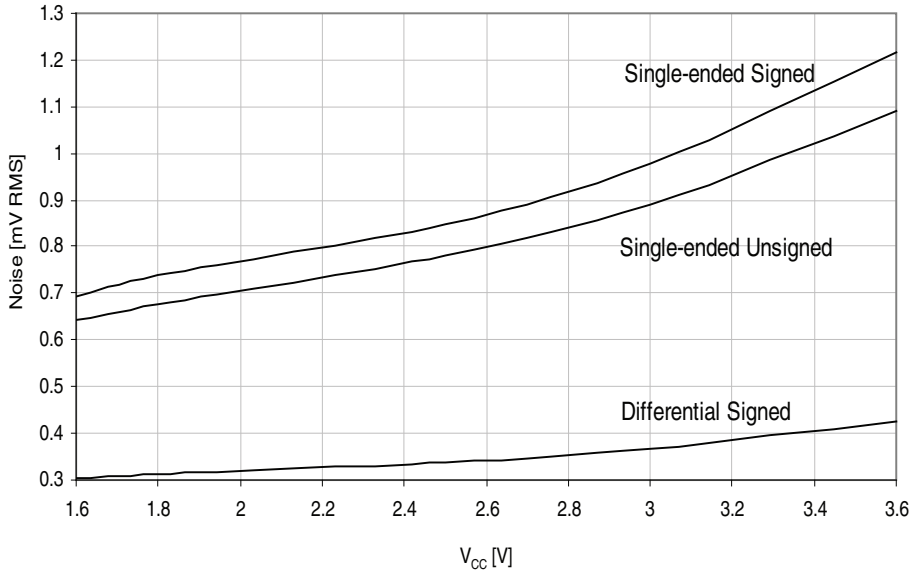


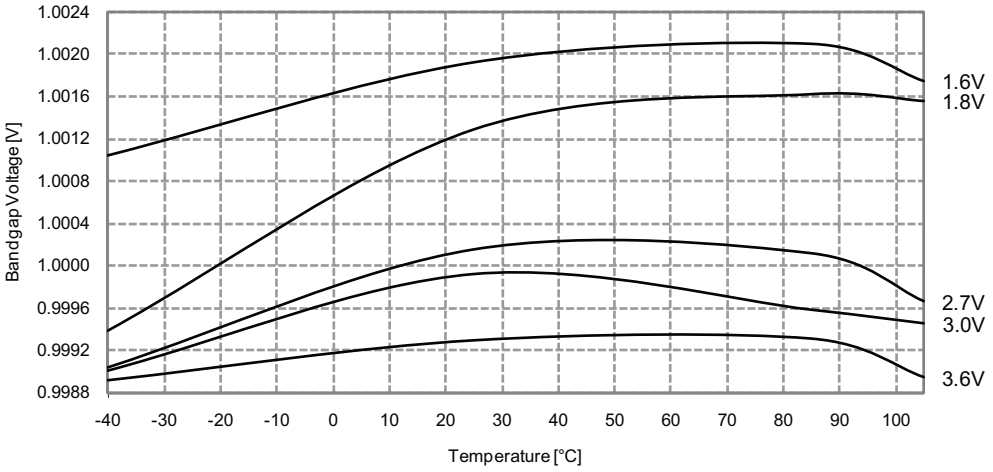
Figure 33-290. Noise vs. V_{CC}

T = 25°C, V_{REF} = external 1.0V, ADC sampling speed = 500ksps



33.4.6 Internal 1.0V Reference Characteristics

Figure 33-301. ADC/DAC Internal 1.0V Reference vs. Temperature



33.4.7 BOD Characteristics

Figure 33-302. BOD Thresholds vs. Temperature

BOD level = 1.6V

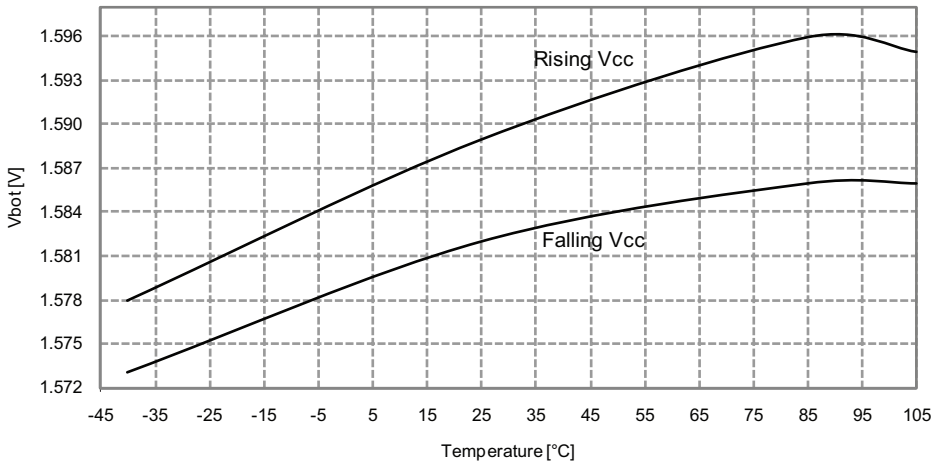
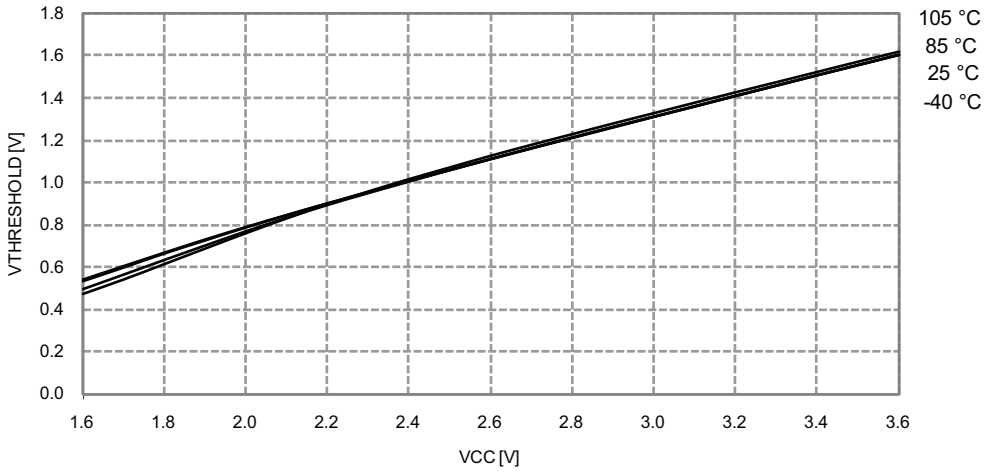


Figure 33-309. Reset Pin Input Threshold Voltage vs. V_{CC}

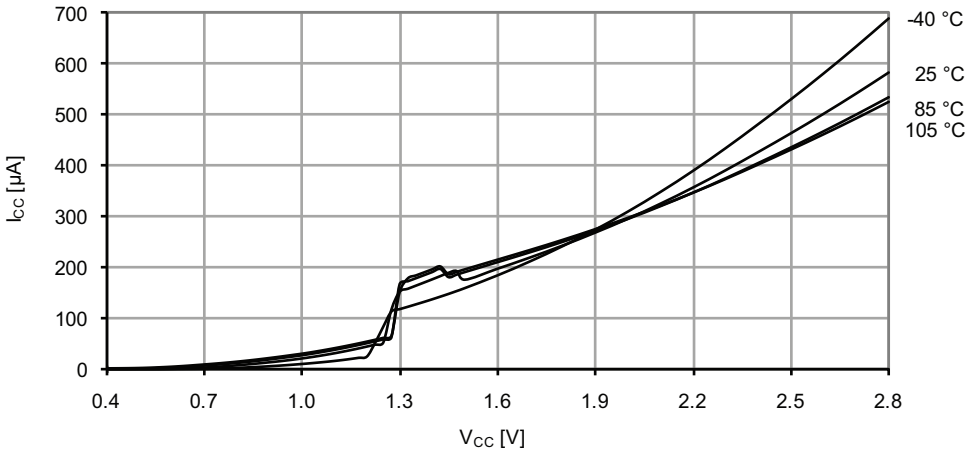
V_{IL} - Reset pin read as "0"



33.4.9 Power-on Reset Characteristics

Figure 33-310. Power-on Reset Current Consumption vs. V_{CC}

BOD level = 3.0V, enabled in continuous mode



34. Errata

34.1 ATxmega16D4 / ATxmega32D4

34.1.1 Rev. I

- Temperature sensor not calibrated

1. Temperature sensor not calibrated

Temperature sensor factory calibration not implemented.

Problem fix/Workaround

None.

34.1.2 Rev. F/G/H

Not sampled.

34.1.3 Rev. E

- ADC propagation delay is not correct when gain is used
- CRC fails for Range CRC when end address is the last word address of a flash section
- AWeX fault protection restore is not done correct in Pattern Generation Mode
- Erroneous interrupt when using Timer/Counter with QDEC
- AC system status flags are only valid if AC-system is enabled
- Temperature sensor not calibrated

1. ADC propagation delay is not correct when gain is used

The propagation delay will increase by only one ADC clock cycle for all gain setting.

Problem fix/Workaround

None.

2. CRC fails for Range CRC when end address is the last word address of a flash section

If boot read lock is enabled, the range CRC cannot end on the last address of the application section. If application table read lock is enabled, the range CRC cannot end on the last address before the application table.

Problem fix/Workaround

Ensure that the end address used in Range CRC does not end at the last address before a section with read lock enabled. Instead, use the dedicated CRC commands for complete applications sections.

3. AWeX fault protection restore is not done correct in Pattern Generation Mode

When a fault is detected the OUTOVEN register is cleared, and when fault condition is cleared, OUTOVEN is restored according to the corresponding enabled DTI channels. For Common Waveform Channel Mode (CWCM), this has no effect as the OUTOVEN is correct after restoring from fault. For Pattern Generation Mode (PGM), OUTOVEN should instead have been restored according to the DTILSBUF register.

35.9 8135K – 06/2012

1. ATxmega64D4-CU is added in “Ordering Information” on page 2

35.10 8135J – 12/10

1. Datasheet status changed to complete: Preliminary removed from the front page.
2. Updated all tables in the “Electrical Characteristics” on page 64.
3. Replaced Table 31-11 on page 64.
4. Replaced Table 31-17 on page 65 and added the figure ”TOSC input capacitance” on page 66.
5. Updated ERRATA ADC (ADC has increased INL for some operating conditions).
6. Updated ERRATA ”rev. A/B” on page 90 with TWIE (TWIE is not available).
7. Updated the last page with Atmel new Brand Style Guide.

35.11 8135I – 10/10

1. Updated Table 31-1 on page 58.

35.12 8135H – 09/10

1. Updated ”Errata” on page 90.

35.13 8135G – 08/10

1. Updated the Footnote 3 of ”Ordering Information” on page 2.
2. All references to CRC removed. Updated Figure 3-1 on page 7.
3. Updated ”Features” on page 26. Event Channel 0 output on port pin 7.
4. Updated ”DC Characteristics” on page 58 by adding Icc for Flash/EEPROM Programming.
5. Added AVCC in ”ADC Characteristics” on page 62.
6. Updated Start up time in ”ADC Characteristics” on page 62.
7. Updated and fixed typo in “Errata” section.

35.14 8135F – 02/10

1. Added ”PDI Speed” on page 89.

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