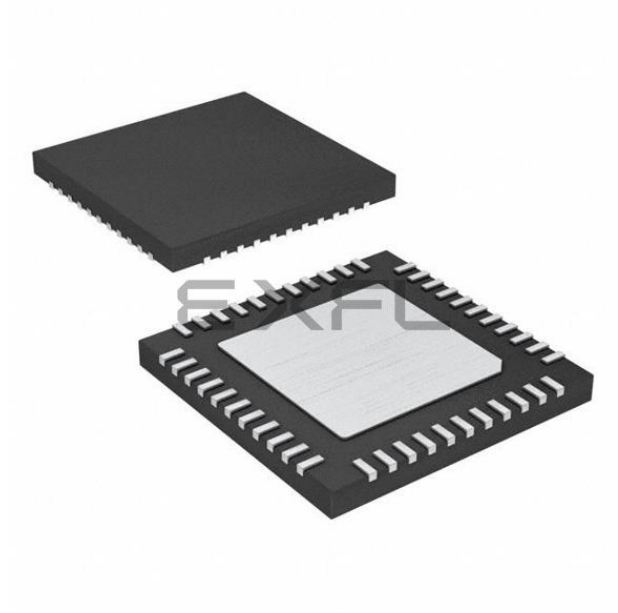

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFQFN Exposed Pad
Supplier Device Package	44-VQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega32d4-mh

9. System Clock and Clock Options

9.1 Features

- Fast start-up time
- Safe run-time clock switching
- Internal oscillators:
  - 32MHz run-time calibrated and tuneable oscillator
  - 2MHz run-time calibrated oscillator
  - 32.768kHz calibrated oscillator
  - 32kHz ultra low power (ULP) oscillator with 1kHz output
- External clock options
  - 0.4MHz - 16MHz crystal oscillator
  - 32.768kHz crystal oscillator
  - External clock
- PLL with 20MHz - 128MHz output frequency
  - Internal and external clock options and 1x to 31x multiplication
  - Lock detector
- Clock prescalers with 1x to 2048x division
- Fast peripheral clocks running at two and four times the CPU clock
- Automatic run-time calibration of internal oscillators
- External oscillator and PLL lock failure detection with optional non-maskable interrupt

9.2 Overview

Atmel AVR XMEGA D4 devices have a flexible clock system supporting a large number of clock sources. It incorporates both accurate internal oscillators and external crystal oscillator and resonator support. A high-frequency phase locked loop (PLL) and clock prescalers can be used to generate a wide range of clock frequencies. A calibration feature (DFLL) is available, and can be used for automatic run-time calibration of the internal oscillators to remove frequency drift over voltage and temperature. An oscillator failure monitor can be enabled to issue a non-maskable interrupt and switch to the internal oscillator if the external oscillator or PLL fails.

When a reset occurs, all clock sources except the 32kHz ultra low power oscillator are disabled. After reset, the device will always start up running from the 2MHz internal oscillator. During normal operation, the system clock source and prescalers can be changed from software at any time.

Figure 9-1 on page 20 presents the principal clock system in the XMEGA D4 family of devices. Not all of the clocks need to be active at a given time. The clocks for the CPU and peripherals can be stopped using sleep modes and power reduction registers, as described in “Power Management and Sleep Modes” on page 22.

19. RTC – 16-bit Real-Time Counter

19.1 Features

- 16-bit resolution
- Selectable clock source
  - 32.768kHz external crystal
  - External clock
  - 32.768kHz internal oscillator
  - 32kHz internal ULP oscillator
- Programmable 10-bit clock prescaling
- One compare register
- One period register
- Clear counter on period overflow
- Optional interrupt/event on overflow and compare match

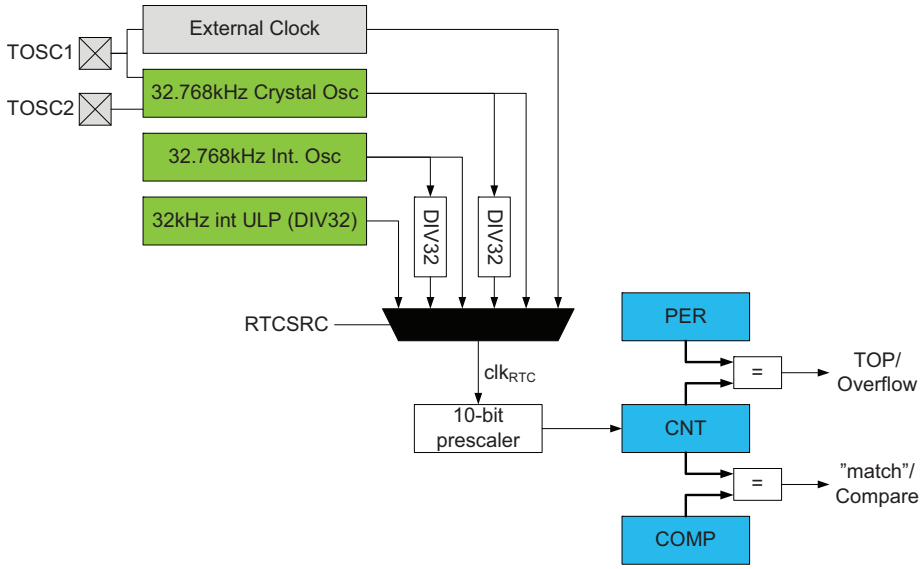
19.2 Overview

The 16-bit real-time counter (RTC) is a counter that typically runs continuously, including in low-power sleep modes, to keep track of time. It can wake up the device from sleep modes and/or interrupt the device at regular intervals.

The reference clock is typically the 1.024kHz output from a high-accuracy crystal of 32.768kHz, and this is the configuration most optimized for low power consumption. The faster 32.768kHz output can be selected if the RTC needs a resolution higher than 1ms. The RTC can also be clocked from an external clock signal, the 32.768kHz internal oscillator or the 32kHz internal ULP oscillator.

The RTC includes a 10-bit programmable prescaler that can scale down the reference clock before it reaches the counter. A wide range of resolutions and time-out periods can be configured. With a 32.768kHz clock source, the maximum resolution is 30.5µs, and time-out periods can range up to 2000 seconds. With a resolution of 1s, the maximum timeout period is more than18 hours (65536 seconds). The RTC can give a compare interrupt and/or event when the counter equals the compare register value, and an overflow interrupt and/or event when it equals the period register value.

Figure 19-1. Real-time Counter Overview



32.1.5 I/O Pin Characteristics

The I/O pins complies with the JEDEC LVTTL and LVCMOS specification and the high- and low level input and output voltage limits reflect or exceed this specification.

Table 32-7. I/O Pin Characteristics

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{OH} (1)/ I_{OL} (2)	I/O pin source/sink current			-20		20	mA
V_{IH}	High level input voltage	V_{CC} = 2.4 - 3.6V		0.7*Vcc		V_{CC}+0.5	V
		V_{CC} = 1.6 - 2.4V		0.8*V_{CC}		V_{CC}+0.5	
V_{IL}	Low level input voltage	V_{CC} = 2.4- 3.6V		-0.5		0.3*V_{CC}	
		V_{CC} = 1.6 - 2.4V		-0.5		0.2*V_{CC}	
V_{OH}	High level output voltage	V_{CC} = 3.3V	I_{OH} = -4mA	2.6	2.9		
		V_{CC} = 3.0V	I_{OH} = -3mA	2.1	2.7		
		V_{CC} = 1.8V	I_{OH} = -1mA	1.4	1.6		
V_{OL}	Low level output voltage	V_{CC} = 3.3V	I_{OL} = 8mA		0.4	0.76	
		V_{CC} = 3.0V	I_{OL} = 5mA		0.3	0.64	
		V_{CC} = 1.8V	I_{OL} = 3mA		0.2	0.46	
I_{IN}	Input leakage current I/O pin	T = 25°C			<0.01	1	µA
R_P	Pull/buss keeper resistor				25		kΩ

Notes:
1. The sum of all I_{OH} for PORTA and PORTB must not exceed 100mA.
   The sum of all I_{OH} for PORTC, PORTD, PORTE must for each port not exceed 200mA.
   The sum of all I_{OH} for pins PF[0-5] on PORTF must not exceed 200mA.
   The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR and PDI must not exceed 100mA.
2. The sum of all I_{OL} for PORTA and PORTB must not exceed 100mA.
   The sum of all I_{OL} for PORTC, PORTD, PORTE must for each port not exceed 200mA.
   The sum of all I_{OL} for pins PF[0-5] on PORTF must not exceed 200mA.
   The sum of all I_{OL} for pins PF[6-7] on PORTF, PORTR and PDI must not exceed 100mA.

32.3.6 ADC Characteristics

Table 32-64. Power Supply, Reference and Input Range

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
AV_{CC}	Analog supply voltage		V_{CC}- 0.3		V_{CC}+ 0.3	V
V_{REF}	Reference voltage		1.0		AV_{CC}- 0.6	
R_{in}	Input resistance	Switched		4.0		kΩ
C_{sample}	Input capacitance	Switched		4.4		pF
R_{AREF}	Reference input resistance	(leakage only)		>10		MΩ
C_{AREF}	Reference input capacitance	Static load		7.0		pF
V_{IN}	Input range		-0.1		AV_{CC}+0.1	V
	Conversion range	Differential mode, Vinp - Vinn	$-V_{REF}$		V_{REF}	
V_{IN}	Conversion range	Single ended unsigned mode, Vinp	-ΔV		V_{REF}-ΔV	
ΔV	Fixed offset voltage			190		LSB

Table 32-65. Clock and Timing

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{ADC}	ADC clock frequency	Maximum is 1/4 of Peripheral clock frequency	100		1400	kHz
		Measuring internal signals	100		125	
f_{ClkADC}	Sample rate		14		200	ksps
f_{ADC}	Sample rate	Current limitation (CURRLIMIT) off			200	
		CURRLIMIT = LOW			150	
		CURRLIMIT = MEDIUM			100	
		CURRLIMIT = HIGH			50	
	Sampling time	1/2 Clk_{ADC} cycle	0.25		5	µs
	Conversion time (latency)	(RES+2)/2+GAIN RES = 8 or 12, GAIN = 0, 1, 2 or 3	5	7	10	Clk_{ADC} cycles
	Start-up time	ADC clock cycles		12	24	Clk_{ADC} cycles
	ADC settling time	After changing reference or input mode		7	7	
		After ADC flush		1	1	

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
C_{XTAL1}	Parasitic capacitance XTAL1 pin			5.9		pF
C_{XTAL2}	Parasitic capacitance XTAL2 pin			8.3		
C_{LOAD}	Parasitic capacitance load			3.5		

Note: 1. Numbers for negative impedance are not tested in production but guaranteed from design and characterization.

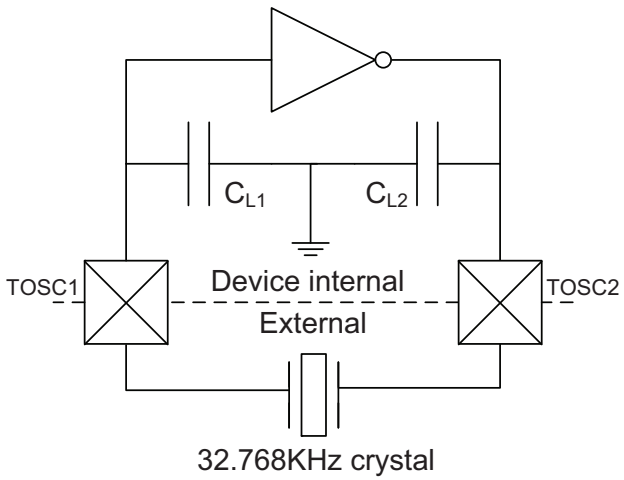
32.3.13.8 External 32.768kHz Crystal Oscillator and TOSC Characteristics

Table 32-83. External 32.768kHz Crystal Oscillator and TOSC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ESR/R1	Recommended crystal equivalent series resistance (ESR)	Crystal load capacitance 6.5pF			60	kΩ
		Crystal load capacitance 9.0pF			35	
C_{TOSC}	Parasitic capacitance	Normal mode		4.7		pF
		Low power mode		5.2		
	Recommended safety factor	Capacitance load matched to crystal specification	3			

Note: 1. See Figure 32-18 on page 118 for definition.

Figure 32-18.TOSC Input Capacitance



The parasitic capacitance between the TOSC pins is C_{L1} + C_{L2} in series as seen from the crystal when oscillating without external capacitors.

Figure 33-25. I/O Pin Output Voltage vs. Source Current

V_{CC} = 3.0V

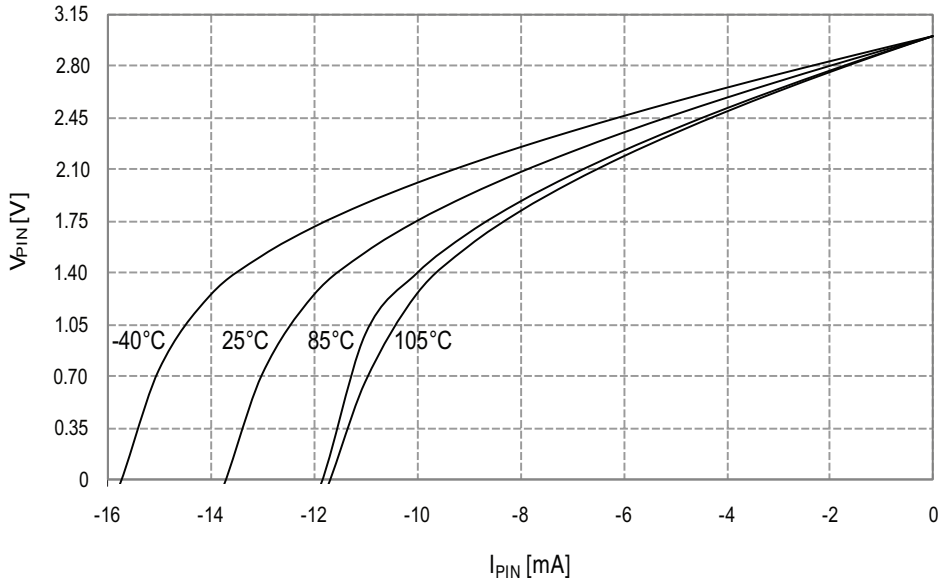


Figure 33-26. I/O Pin Output Voltage vs. Source Current

V_{CC} = 3.3V

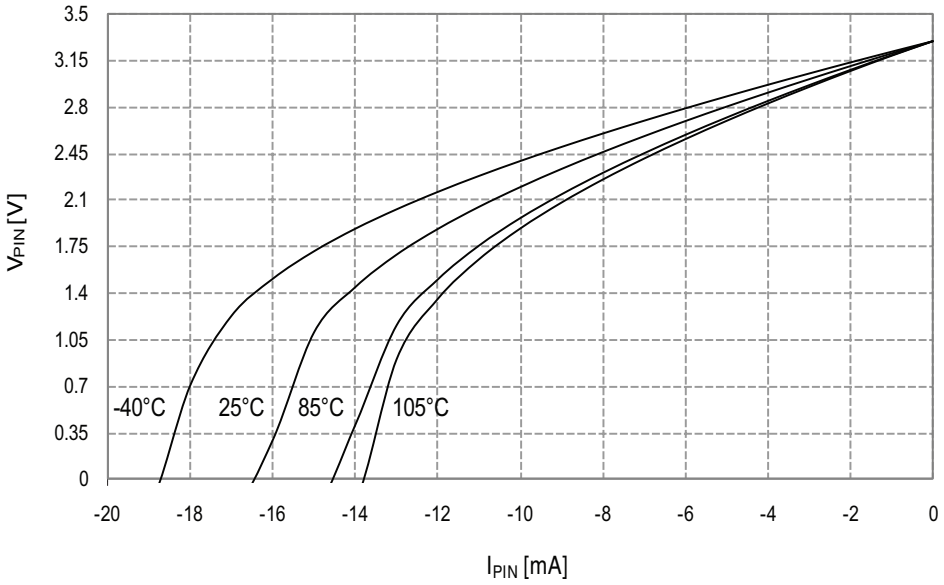


Figure 33-75. 48MHz Internal Oscillator Frequency vs. Temperature

DFLL enabled, from the 32.768kHz internal oscillator

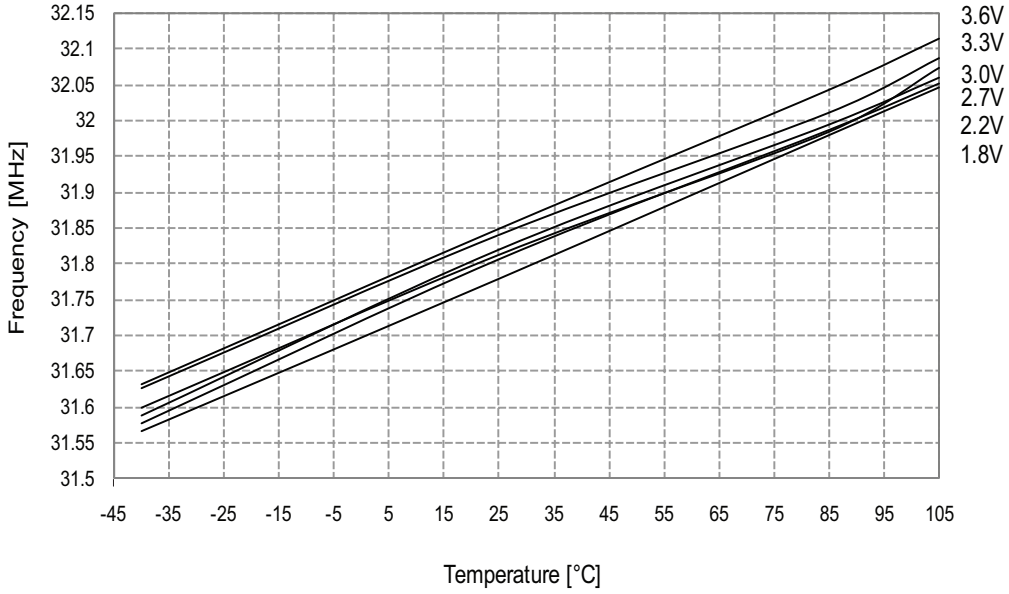


Figure 33-76. 48MHz Internal Oscillator CALA Calibration Step Size

V_{CC} = 3.0V

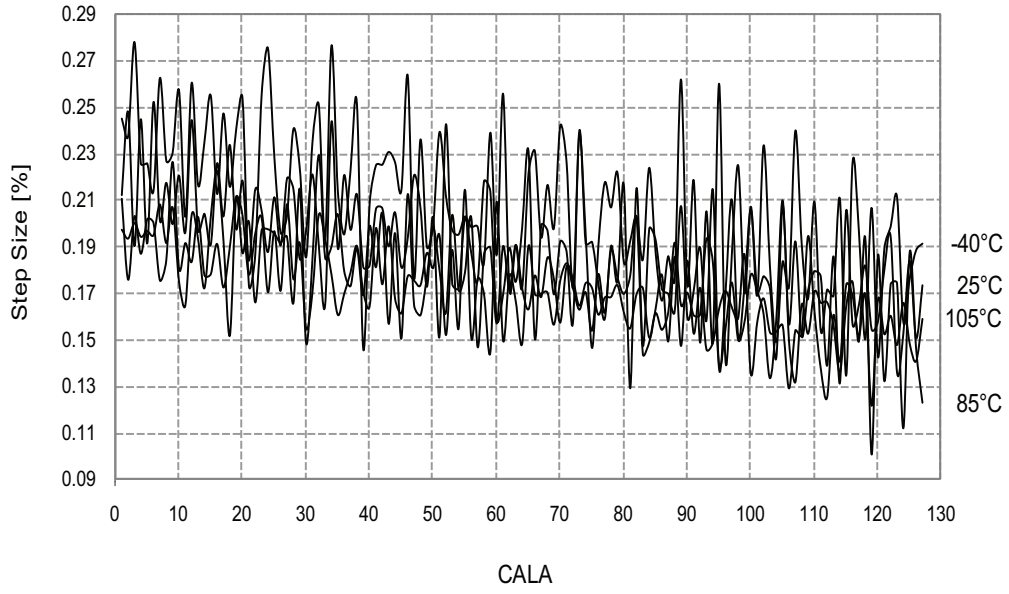


Figure 33-92. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator prescaled to 8MHz

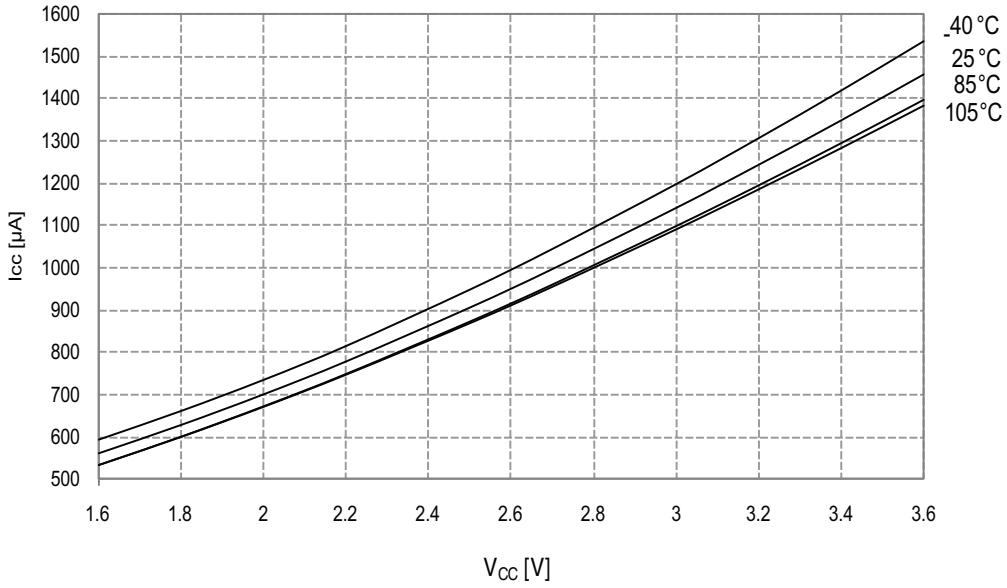


Figure 33-93. Idle Mode Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator

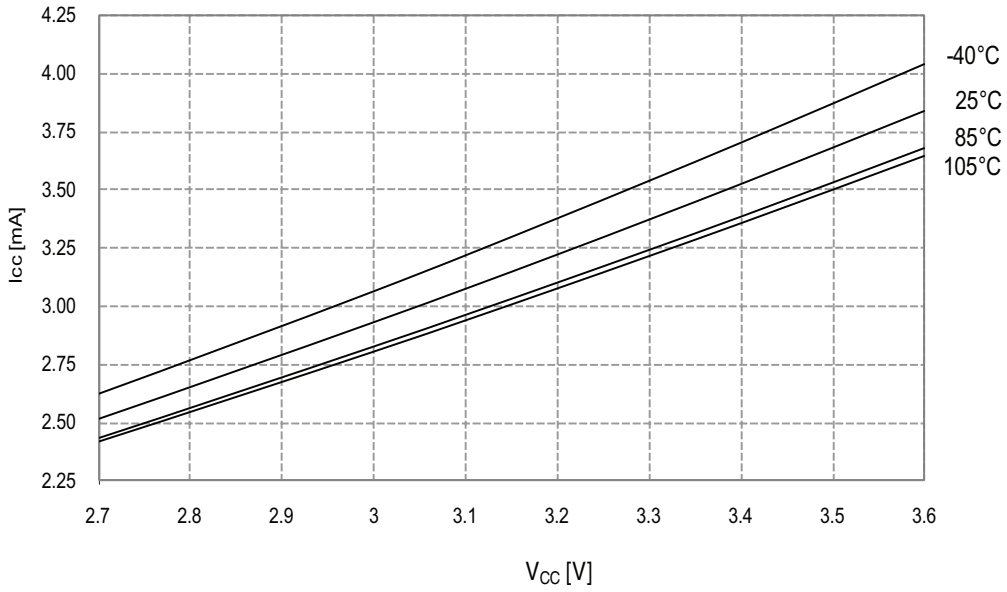


Figure 33-112. I/O Pin Input Threshold Voltage vs. V_{CC}

V_{IH} I/O pin read as "1"

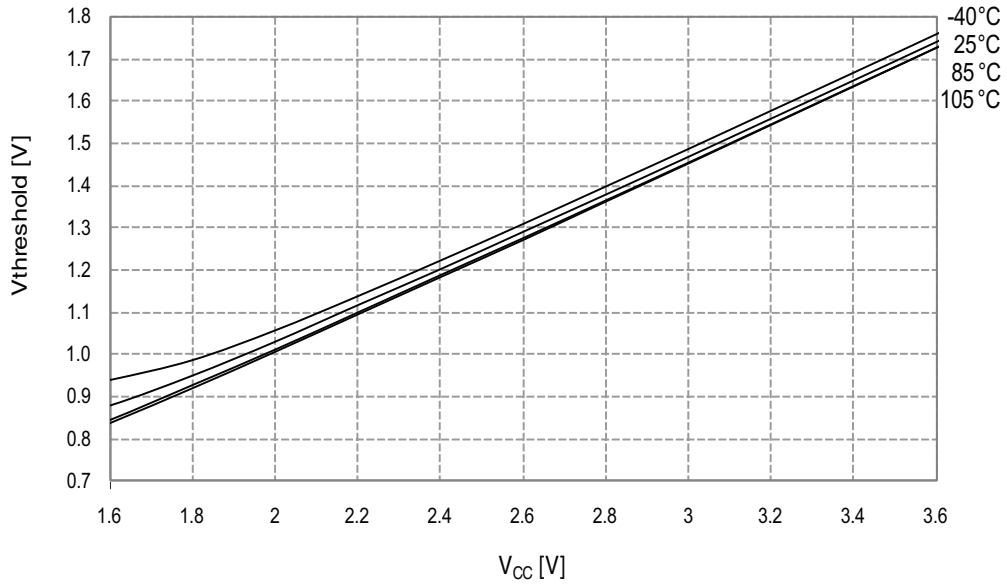


Figure 33-113. I/O Pin Input Threshold Voltage vs. V_{CC}

V_{IL} I/O pin read as "0"

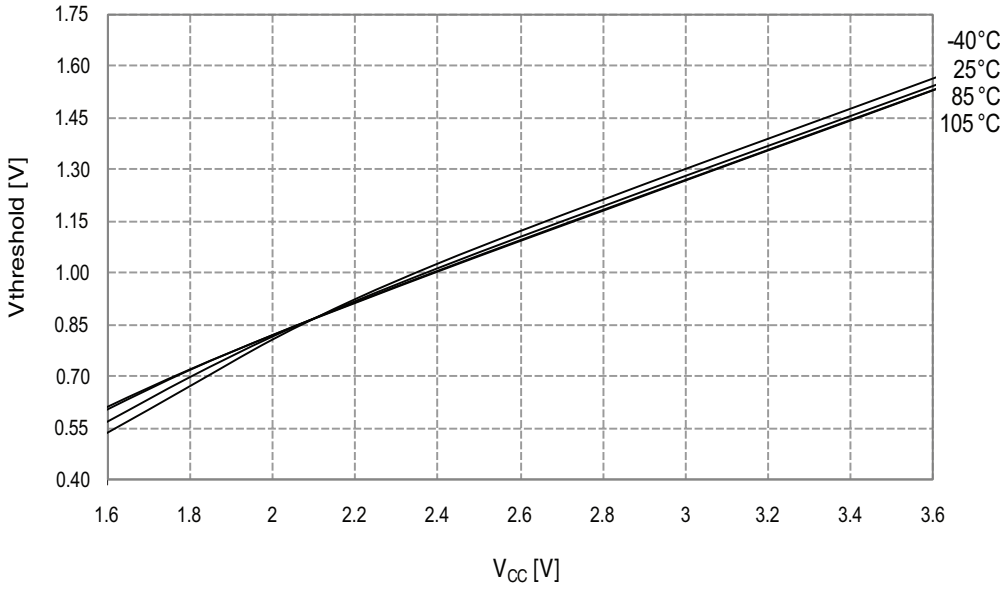
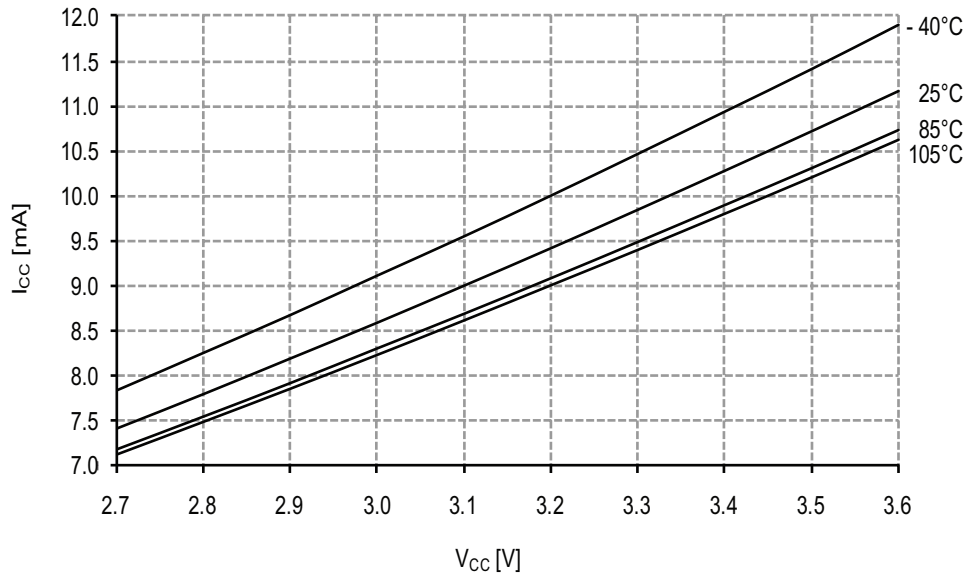


Figure 33-165. Active Mode Supply Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator



33.3.1.2 Idle Mode Supply Current

Figure 33-166. Idle Mode Supply Current vs. Frequency

f_{SYS} = 0 - 1MHz external clock, T = 25°C

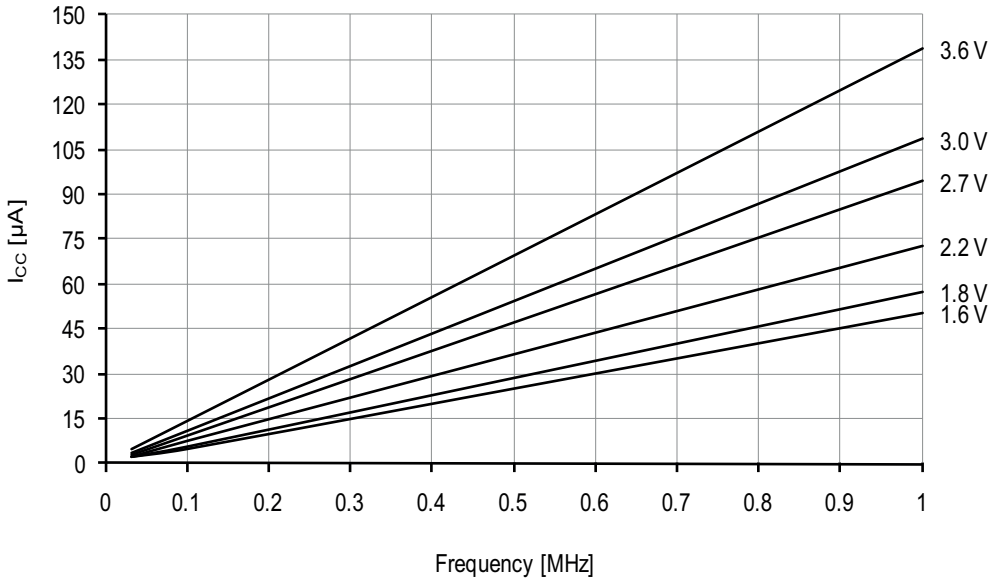


Figure 33-197. DNL Error vs. External V_{REF}

T = 25°C, V_{CC} = 3.6V, external reference

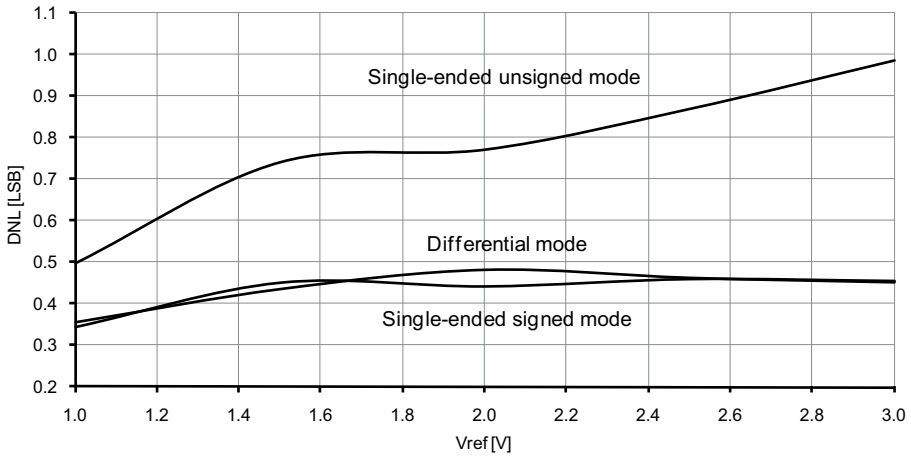


Figure 33-198. DNL Error vs. Sample rate

T = 25°C, V_{CC} = 2.7V, V_{REF} = 1.0V external

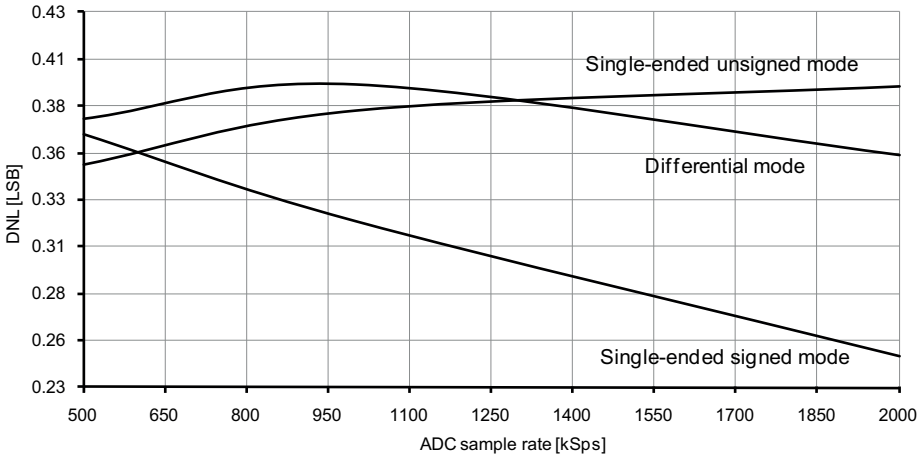
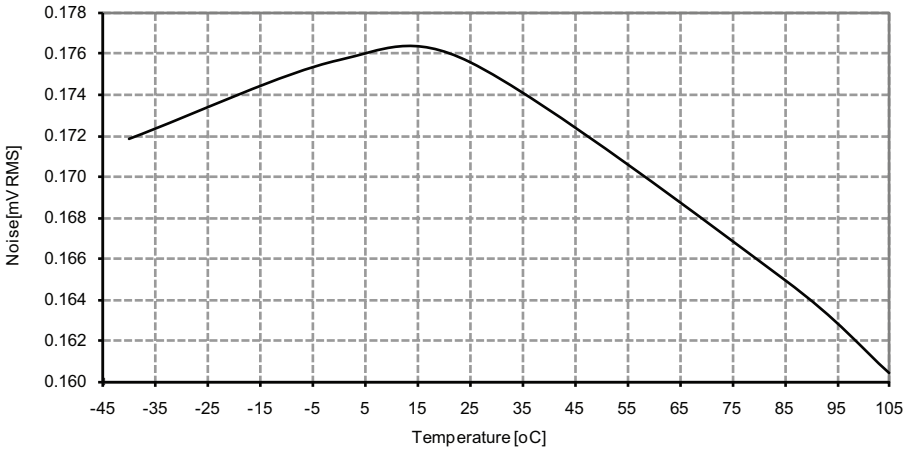


Figure 33-209. DAC Noise vs. Temperature

V_{CC} = 2.7V, V_{REF} = 1.0V



33.3.5 Analog Comparator Characteristics

Figure 33-210. Analog Comparator Hysteresis vs. V_{CC}

High-speed, small hysteresis

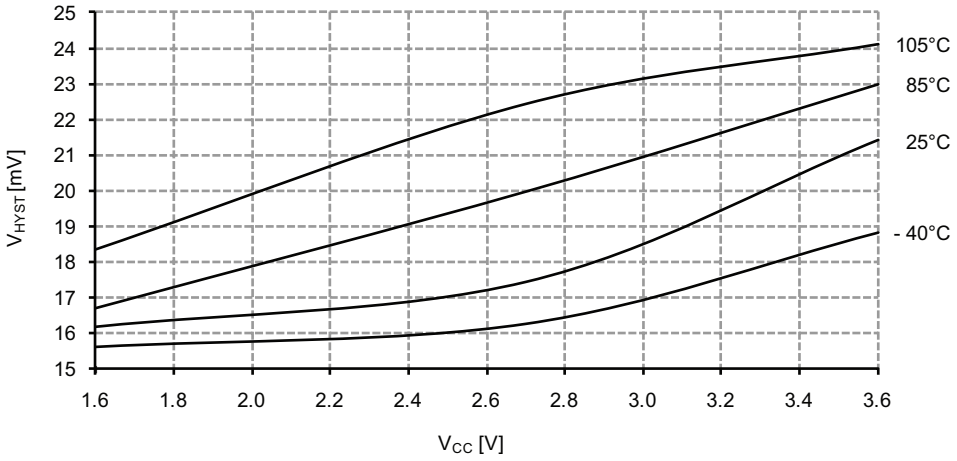


Figure 33-223. Reset Pin Pull-up Resistor Current vs. Reset Pin Voltage

V_{CC} = 3.3V

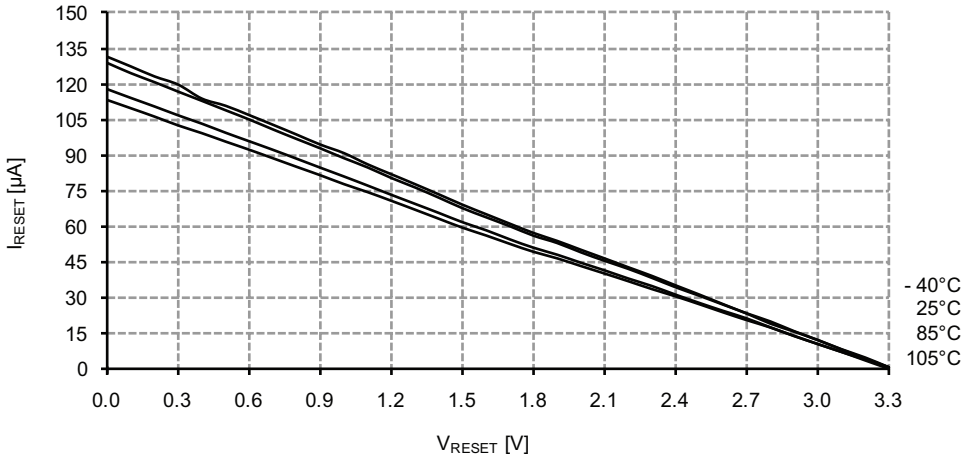
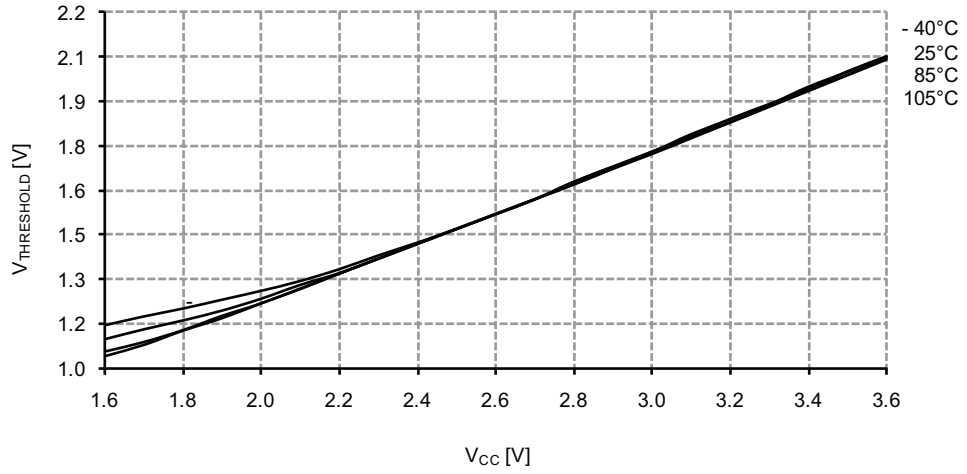


Figure 33-224. Reset Pin Input Threshold Voltage vs. V_{CC}

V_{IH} - Reset pin read as "1"



33.3.10.2 32.768kHz Internal Oscillator

Figure 33-229. 32.768kHz Internal Oscillator Frequency vs. Temperature

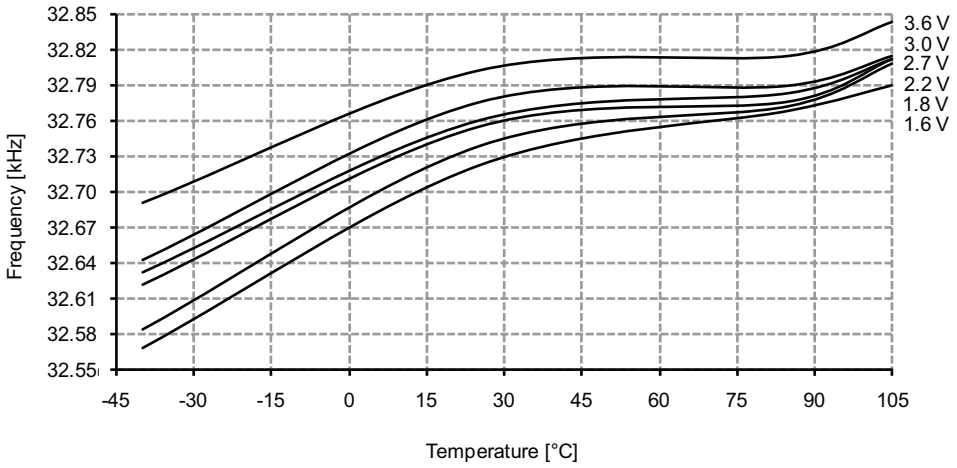
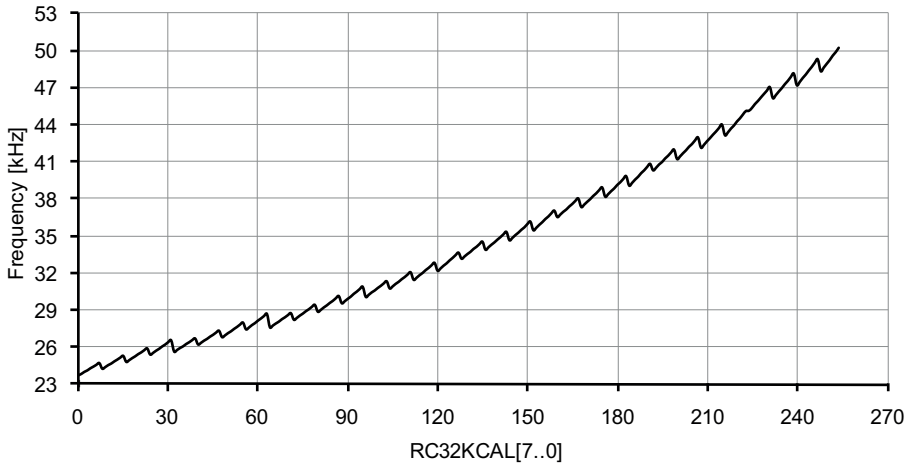


Figure 33-230. 32.768kHz Internal Oscillator Frequency vs. Calibration Value

V_{CC} = 3.0V, T = 25°C



33.4.2 I/O Pin Characteristics

33.4.2.1 Pull-up

Figure 33-263. I/O Pin Pull-up Resistor Current vs. Input Voltage

V_{CC} = *1.8V*

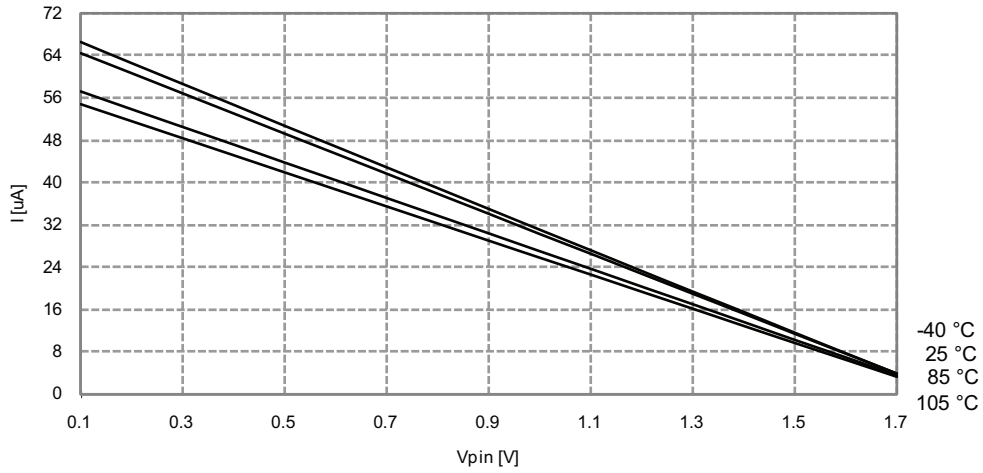


Figure 33-264. I/O Pin Pull-up Resistor Current vs. Input Voltage

V_{CC} = *3.0V*

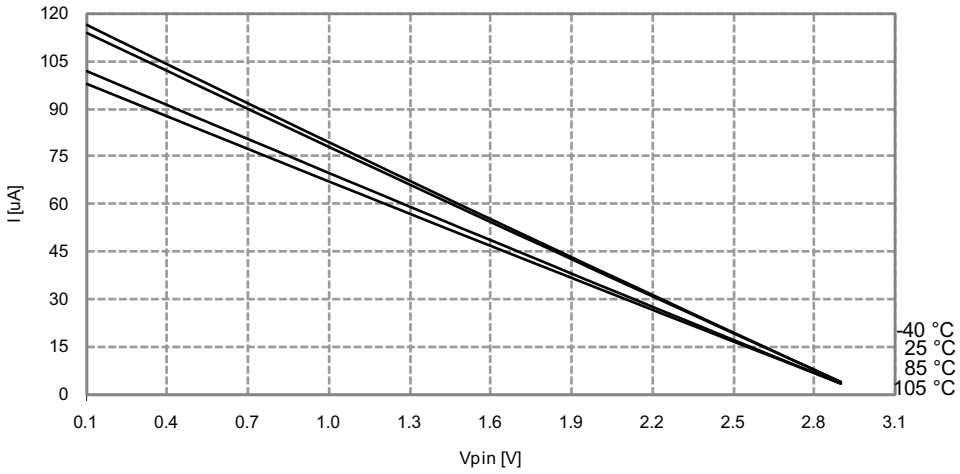


Figure 33-299. Analog Comparator Current Source vs. Calibration Value

V_{CC} = 3.0V

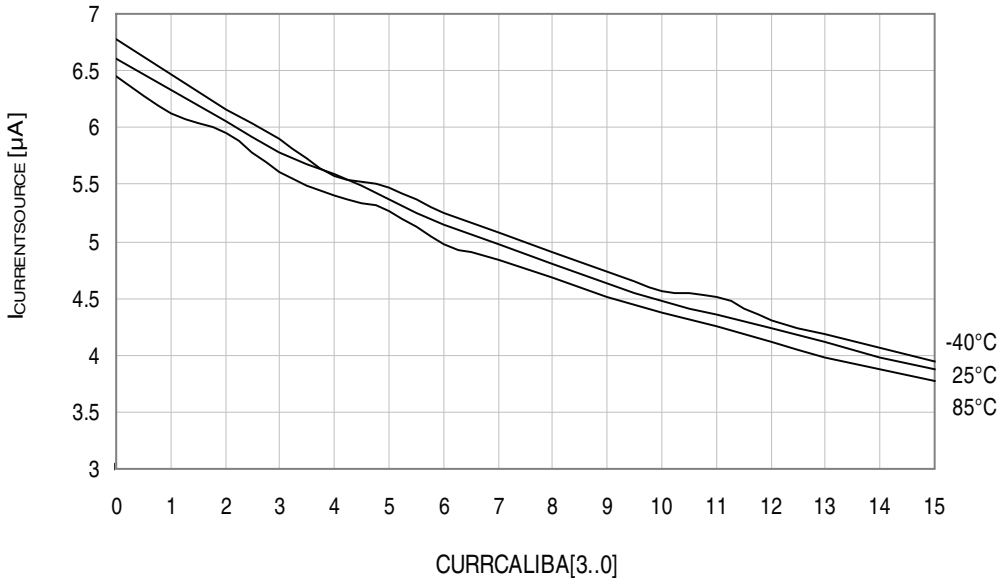


Figure 33-300. Voltage Scaler INL vs. SCALEFAC

T = 25°C, V_{CC} = 3.0V

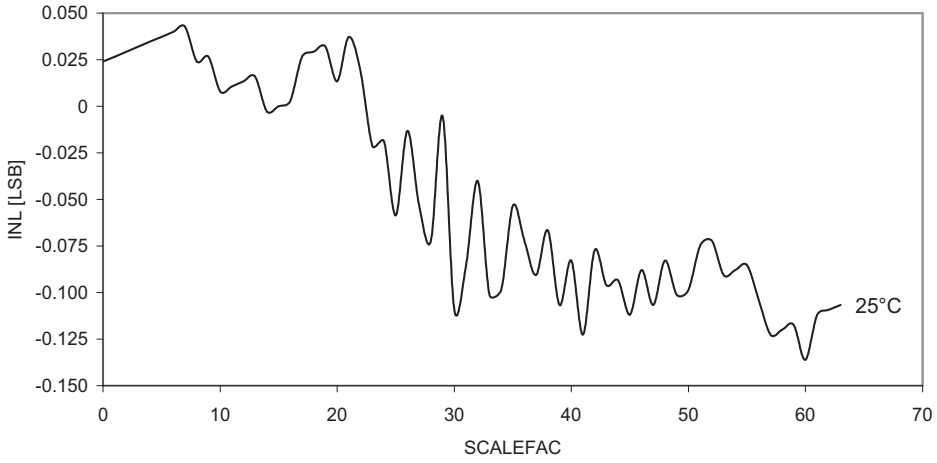
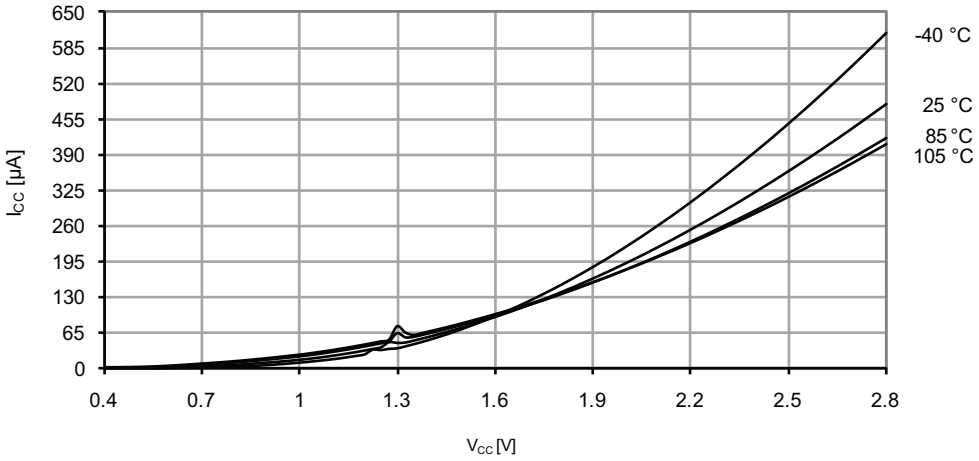


Figure 33-311. Power-on Reset Current Consumption vs. V_{CC}

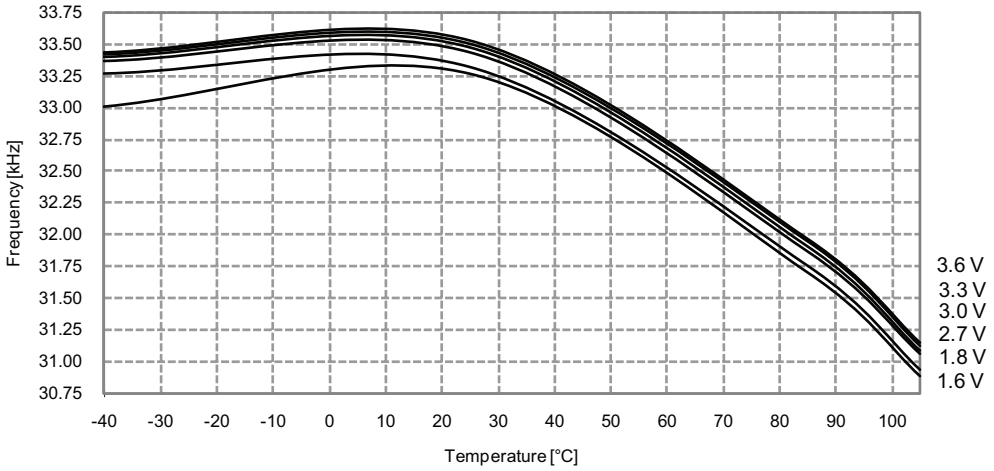
BOD level = 3.0V, enabled in sampled mode



33.4.10 Oscillator Characteristics

33.4.10.1 Ultra Low-Power Internal Oscillator

Figure 33-312. Ultra Low-Power Internal Oscillator Frequency vs. Temperature



34. Errata

34.1 ATxmega16D4 / ATxmega32D4

34.1.1 Rev. I

- Temperature sensor not calibrated

1. Temperature sensor not calibrated

Temperature sensor factory calibration not implemented.

Problem fix/Workaround

None.

34.1.2 Rev. F/G/H

Not sampled.

34.1.3 Rev. E

- ADC propagation delay is not correct when gain is used
- CRC fails for Range CRC when end address is the last word address of a flash section
- AWeX fault protection restore is not done correct in Pattern Generation Mode
- Erroneous interrupt when using Timer/Counter with QDEC
- AC system status flags are only valid if AC-system is enabled
- Temperature sensor not calibrated

1. ADC propagation delay is not correct when gain is used

The propagation delay will increase by only one ADC clock cycle for all gain setting.

Problem fix/Workaround

None.

2. CRC fails for Range CRC when end address is the last word address of a flash section

If boot read lock is enabled, the range CRC cannot end on the last address of the application section. If application table read lock is enabled, the range CRC cannot end on the last address before the application table.

Problem fix/Workaround

Ensure that the end address used in Range CRC does not end at the last address before a section with read lock enabled. Instead, use the dedicated CRC commands for complete applications sections.

3. AWeX fault protection restore is not done correct in Pattern Generation Mode

When a fault is detected the OUTOVEN register is cleared, and when fault condition is cleared, OUTOVEN is restored according to the corresponding enabled DTI channels. For Common Waveform Channel Mode (CWCM), this has no effect as the OUTOVEN is correct after restoring from fault. For Pattern Generation Mode (PGM), OUTOVEN should instead have been restored according to the DTILSBUF register.

35. Datasheet Revision History

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

35.1 8135S – 09/2016

1.	Updated “Instruction Set Summary” on page 56. Removed “DES” instruction.
2.	Updated “Gain Stage Characteristics” : Table 32-11 on page 72, Table 32-39 on page 91Table 32-67 on page 110 and Table 32-96 on page 131. “Offset Error, input referred” is changed to “Offset Error, output referred.

35.2 8135R – 02/2015

1.	Updated Figure 25-1 on page 45
2.	Updated the “Packaging information” on page 61. Replaced “44M1” on page 62 by a correct package.
3.	Updated tables Table 32-8 on page 70and Table 32-36 on page 89 with information on fixed voltage offset.
4.	Updated use of capitals in heading, table headings and figure titles.

35.3 8135Q – 09/2014

1.	Updated the “Ordering Information” on page 2. Added ordering information for ATxmega16D4/32D4/64D4/128D4 @ 105°C.
2.	Updated the Application table section from 4K/4K/4K/4K to 8K/4K/4K/4K in the Figure 7-1 on page 13
3.	Updated Table 32-4 on page 66, Table 32-33 on page 86, Table 32-60 on page 104 and Table 32-89 on page 125. Added Icc Power-down power consumption for T=105°C for all functions disabled and for WDT and sampled BOD enabled
4.	Updated Table 32-17 on page 74, Table 32-45 on page 93, Table 32-73 on page 112 and Table 32-102 on page 133. Updated all tables to include values for T=85°C and T=105°C. Removed T=55°C
5.	Changed Vcc to AVcc in Figure 25-1 on page 45 and in the text in Section 25. “ADC – 12-bit Analog to Digital Converter” on page 44 and in Section 26. “AC – Analog Comparator” on page 46
6.	Changed unit parameter for $t_{SU;DAT}$ to ns in Table 32-28 on page 82, Table 32-56 on page 101, Table 32-85 on page 121 and Table 32-114 on page 142.
7.	Added ERRATA information on disabling of USART transmitter to Section 34.1 “ATxmega16D4 / ATxmega32D4” on page 308.
8.	Updated the typical characteristics of “ATxmega64D4” and “ATxmega128D4” with characterizations @105°C

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1.	Updated the typical characteristics of “ATxmega16D4” and “ATxmega32D4” with characterizations @ 105°C