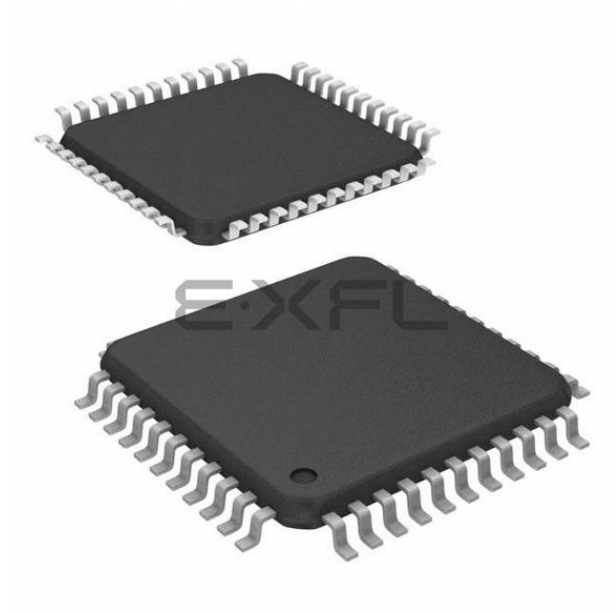

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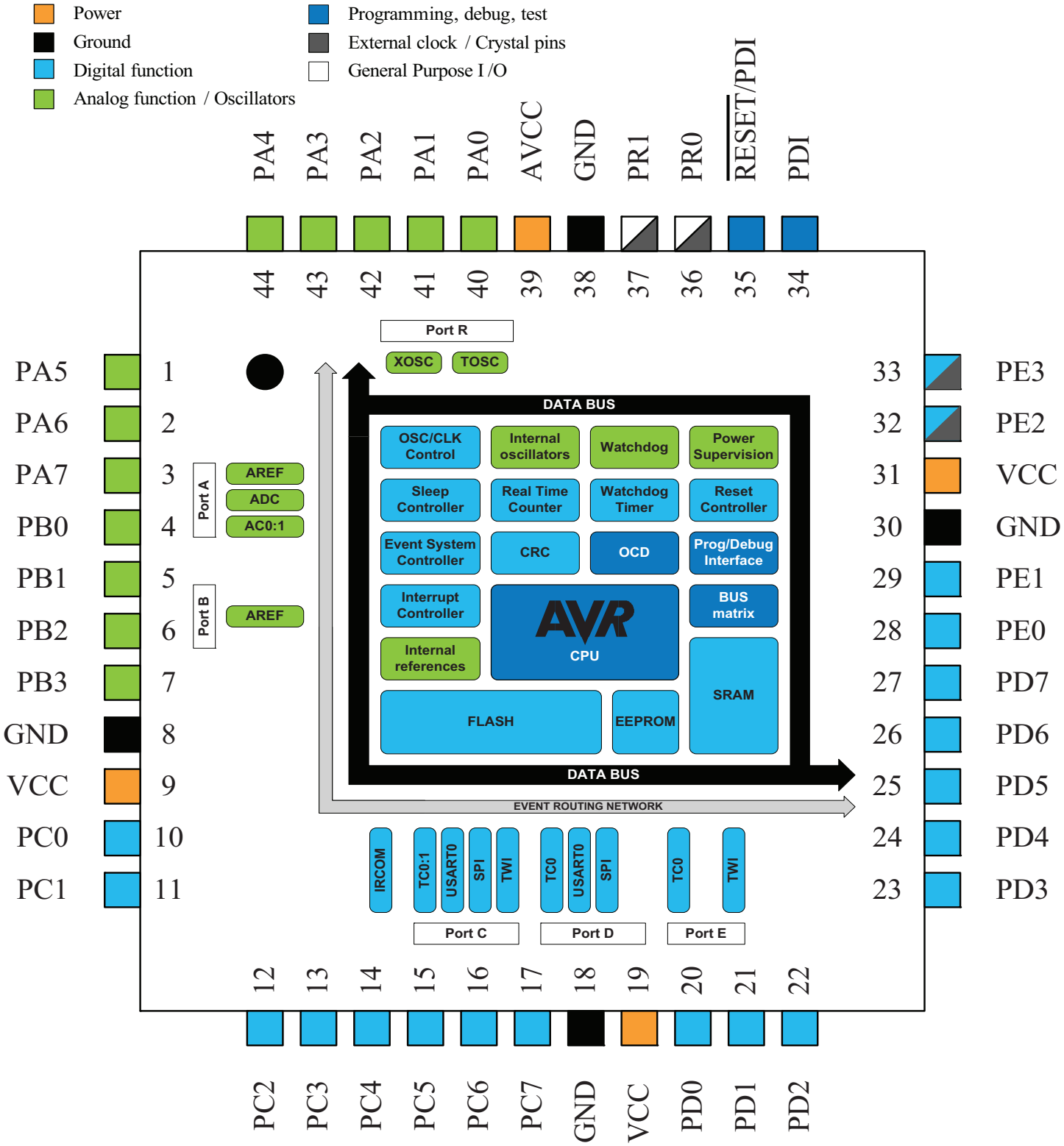
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	34
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega64d4-au

2. Pinout/Block diagram

Figure 2-1. Block Diagram and QFN/TQFP Pinout



Note: 1. For full details on pinout and pin functions refer to "Pinout and Pin Functions" on page 49.

7.3 Flash Program Memory

The Atmel AVR XMEGA devices contain on-chip, in-system reprogrammable flash memory for program storage. The flash memory can be accessed for read and write from an external programmer through the PDI or from application software running in the device.

All AVR CPU instructions are 16 or 32 bits wide, and each flash location is 16 bits wide. The flash memory is organized in two main sections, the application section and the boot loader section. The sizes of the different sections are fixed, but device-dependent. These two sections have separate lock bits, and can have different levels of protection. The store program memory (SPM) instruction, which is used to write to the flash from the application software, will only operate when executed from the boot loader section.

The application section contains an application table section with separate lock settings. This enables safe storage of nonvolatile data in the program memory.

Figure 7-1. Flash Program Memory (Hexadecimal Address)

Word address							
ATxmega128D4		**ATxmega64D4**		**ATxmega32D4**		**ATxmega16D4**	
0		0		0		0	Application section (128K/64K/32K/16K)
							...
EFFF	/	77FF	/	37FF	/	17FF	
F000	/	7800	/	3800	/	1800	Application table section (8K/4K/4K/4K)
FFFF	/	7FFF	/	3FFF	/	1FFF	
10000	/	8000	/	4000	/	2000	Boot section (8K/4K/4K/4K)
10FFF	/	87FF	/	47FF	/	27FF	

7.3.1 Application Section

The Application section is the section of the flash that is used for storing the executable application code. The protection level for the application section can be selected by the boot lock bits for this section. The application section can not store any boot loader code since the SPM instruction cannot be executed from the application section.

7.3.2 Application Table Section

The application table section is a part of the application section of the flash memory that can be used for storing data. The size is identical to the boot loader section. The protection level for the application table section can be selected by the boot lock bits for this section. The possibilities for different protection levels on the application section and the application table section enable safe parameter storage in the program memory. If this section is not used for data, application code can reside here.

7.3.3 Boot Loader Section

While the application section is used for storing the application code, the boot loader software must be located in the boot loader section because the SPM instruction can only initiate programming when executing from this section. The SPM instruction can access the entire flash, including the boot loader section itself. The protection level for the boot loader section can be selected by the boot loader lock bits. If this section is not used for boot loader software, application code can be stored here.

7.3.4 Production Signature Row

The production signature row is a separate memory section for factory programmed data. It contains calibration data for functions such as oscillators and analog modules. Some of the calibration values will be automatically loaded to the corresponding module or peripheral unit during reset. Other values must be loaded from the signature row and written to the corresponding peripheral registers from software. For details on calibration conditions, refer to “Electrical Characteristics” on page 64.

The production signature row also contains an ID that identifies each microcontroller device type and a serial number for each manufactured device. The serial number consists of the production lot number, wafer number, and wafer coordinates for the device. The device ID for the available devices is shown in Table 7-1 on page 14.

The production signature row cannot be written or erased, but it can be read from application software and external programmers.

Table 7-1. Device ID Bytes for Atmel AVR XMEGA D4 Devices

Device	Device ID bytes		
	Byte 2	Byte 1	Byte 0
ATxmega16D4	42	94	1E
ATxmega32D4	42	95	1E
ATxmega64D4	47	96	1E
ATxmega128D4	47	97	1E

7.3.5 User Signature Row

The user signature row is a separate memory section that is fully accessible (read and write) from application software and external programmers. It is one flash page in size, and is meant for static user parameter storage, such as calibration data, custom serial number, identification numbers, random number seeds, etc. This section is not erased by chip erase commands that erase the flash, and requires a dedicated erase command. This ensures parameter storage during multiple program/erase operations and on-chip debug sessions.

7.4 Fuses and Lock Bits

The fuses are used to configure important system functions, and can only be written from an external programmer. The application software can read the fuses. The fuses are used to configure reset sources such as brownout detector and watchdog, startup configuration, JTAG enable, and JTAG user ID.

The lock bits are used to set protection levels for the different flash sections (that is, if read and/or write access should be blocked). Lock bits can be written by external programmers and application software, but only to stricter protection levels. Chip erase is the only way to erase the lock bits. To ensure that flash contents are protected even during chip erase, the lock bits are erased after the rest of the flash memory has been erased.

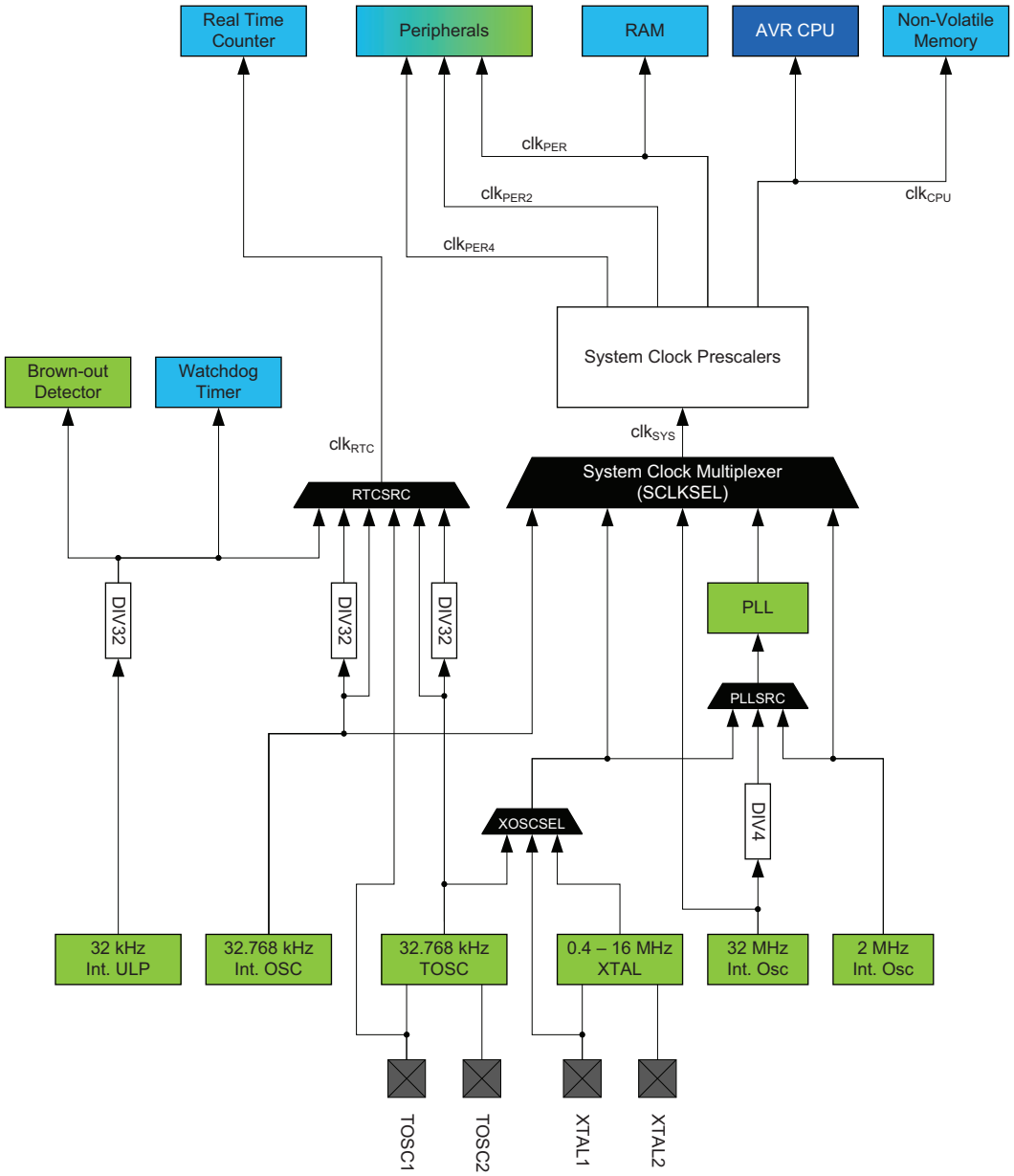
An unprogrammed fuse or lock bit will have the value one, while a programmed fuse or lock bit will have the value zero.

Both fuses and lock bits are reprogrammable like the flash program memory.

7.5 Data Memory

The data memory contains the I/O memory, internal SRAM, optionally memory mapped EEPROM, and external memory if available. The data memory is organized as one continuous memory section, see Figure 7-2 on page 15. To simplify development, I/O Memory, EEPROM and SRAM will always have the same start addresses for all Atmel AVR XMEGA devices.

Figure 9-1. The Clock System, Clock Sources and Clock Distribution



9.3 Clock Sources

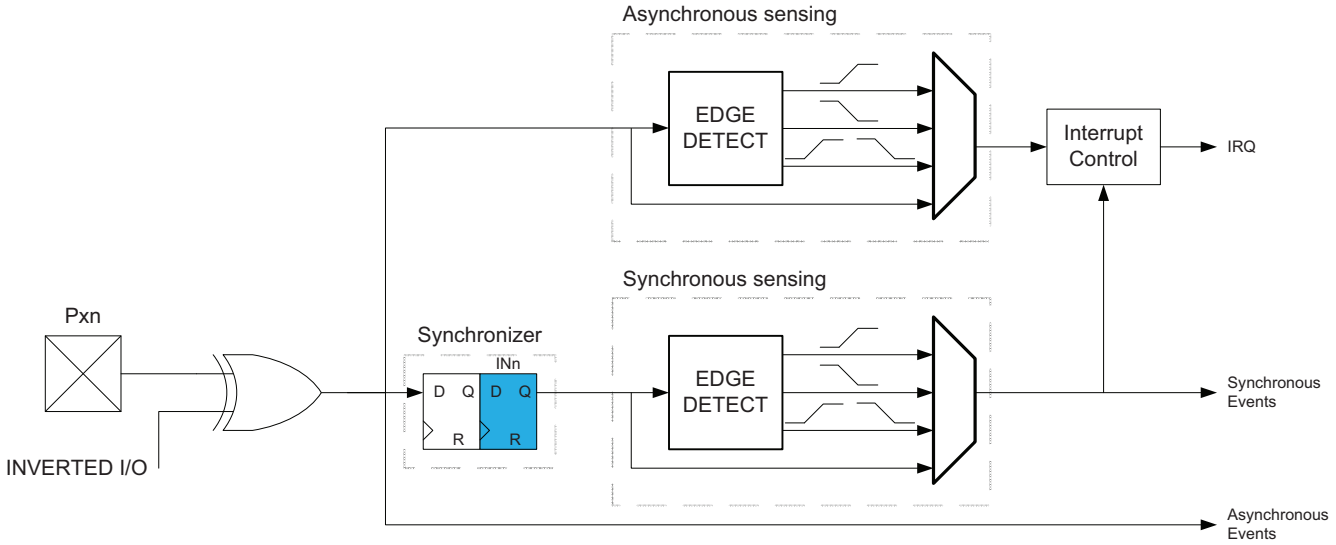
The clock sources are divided in two main groups: internal oscillators and external clock sources. Most of the clock sources can be directly enabled and disabled from software, while others are automatically enabled or disabled, depending on peripheral settings. After reset, the device starts up running from the 2MHz internal oscillator. The other clock sources, DFLLs and PLL, are turned off by default.

The internal oscillators do not require any external components to run. For details on characteristics and accuracy of the internal oscillators, refer to the device datasheet.

9.3.1 32kHz Ultra Low Power Internal Oscillator

This oscillator provides an approximate 32kHz clock. The 32kHz ultra low power (ULP) internal oscillator is a very low power clock source, and it is not designed for high accuracy. The oscillator employs a built-in prescaler that provides a

Figure 14-7. Input Sensing System Overview



When a pin is configured with inverted I/O, the pin value is inverted before the input sensing.

14.5 Alternate Port Functions

Most port pins have alternate pin functions in addition to being a general purpose I/O pin. When an alternate function is enabled, it might override the normal port pin function or pin value. This happens when other peripherals that require pins are enabled or configured to use pins. If and how a peripheral will override and use pins is described in the section for that peripheral. “Pinout and Pin Functions” on page 49 shows which modules on peripherals that enable alternate functions on a pin, and which alternate functions that are available on a pin.

Table 32-66. Accuracy Characteristics

Symbol	Parameter	Condition[2]		Min.	Typ.	Max.	Units
RES	Resolution	Programmable to 8 or 12 bit		8	12	12	Bits
INL[1]	Integral non-linearity	50ksps	V_{CC}-1.0V < V_{REF}< V_{CC}-0.6V		±1.2	±3	lsb
			All V_{REF}		±1.5	±4	
		200ksps	V_{CC}-1.0V < V_{REF}< V_{CC}-0.6V		±1.0	±3	
			All V_{REF}		±1.5	±4	
DNL[1]	Differential non-linearity	guaranteed monotonic			<±0.8	<±1	
	Offset error				-1		mV
		Temperature drift			<0.01		mV/K
		Operating voltage drift			<0.6		mV/V
	Gain error	Differential mode	External reference		-1		mV
			AV_{CC}/1.6		10		
			AV_{CC}/2.0		8		
			Bandgap		±5		
		Temperature drift			<0.02		mV/K
		Operating voltage drift			<0.5		mV/V
	Noise	Differential mode, shorted input 200ksps, V_{CC} = 3.6V, Clk_{PER} = 16MHz			0.4		mV rms

Notes:
1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% input voltage range.
2. Unless otherwise noted all linearity, offset and gain error numbers are valid under the condition that external V_{REF} is used.

Table 32-95. Accuracy Characteristics

Symbol	Parameter	Condition[2]		Min.	Typ.	Max.	Units
RES	Resolution	Programmable to 8 or 12 bit		8	12	12	Bits
INL[1]	Integral non-linearity	50ksps	V_{CC}-1.0V < V_{REF}< V_{CC}-0.6V		±1.2	±2	lsb
			All V_{REF}		±1.5	±3	
		200ksps	V_{CC}-1.0V < V_{REF}< V_{CC}-0.6V		±1.0	±2	
			All V_{REF}		±1.5	±3	
DNL[1]	Differential non-linearity	guaranteed monotonic			<±0.8	<±1	
	Offset error				-1		mV
		Temperature drift			<0.01		mV/K
		Operating voltage drift			<0.6		mV/V
	Gain error	Differential mode	External reference		-1		mV
			AV_{CC}/1.6		10		
			AV_{CC}/2.0		8		
			Bandgap		±5		
		Temperature drift			<0.02		mV/K
		Operating voltage drift			<0.5		mV/V
	Noise	Differential mode, shorted input 200ksps, V_{CC} = 3.6V, Clk_{PER} = 16MHz			0.4		mV rms

Notes:
1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% input voltage range.
2. Unless otherwise noted all linearity, offset and gain error numbers are valid under the condition that external V_{REF} is used.

33.1.1.3 Power-down Mode Supply Current

Figure 33-15. Power-down Mode Supply Current vs. V_{CC}

All functions disabled

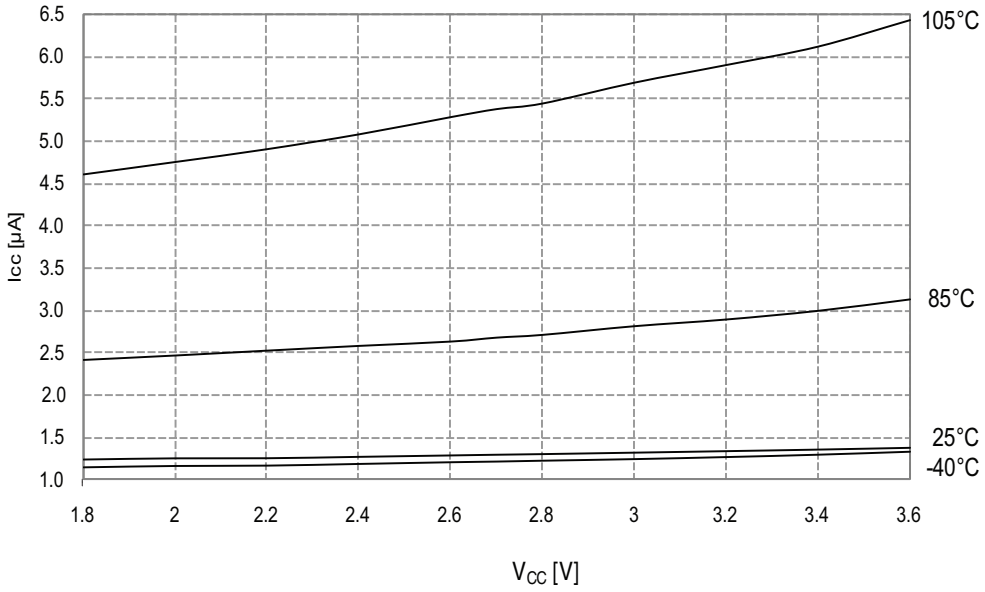
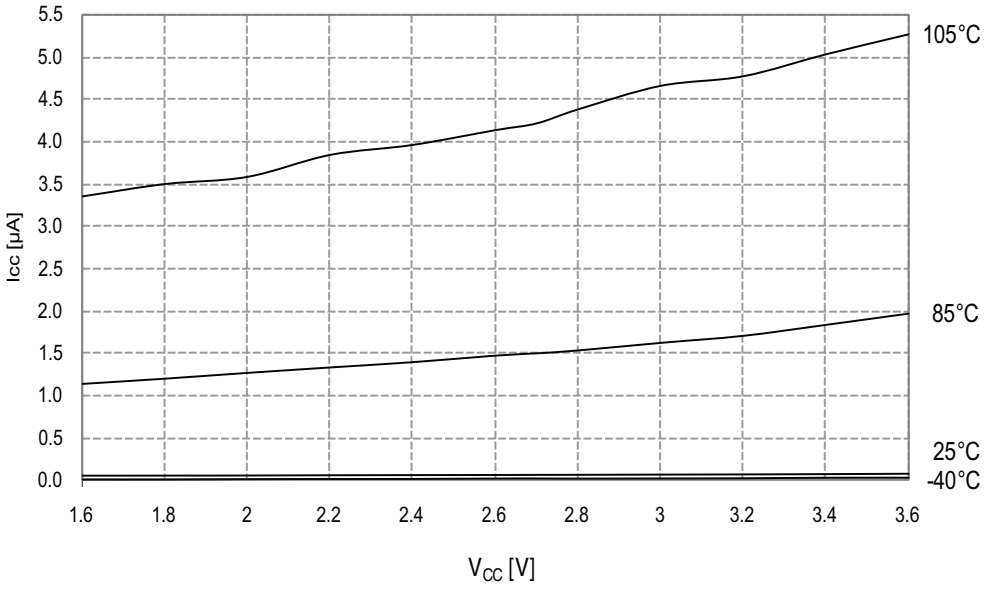


Figure 33-16. Power-down Mode Supply Current vs. V_{CC}

Watchdog and sampled BOD enabled



33.1.1.5 Standby Mode Supply Current

Figure 33-19. Standby Supply Current vs. V_{CC}

Standby, f_{SYS} = 1MHz

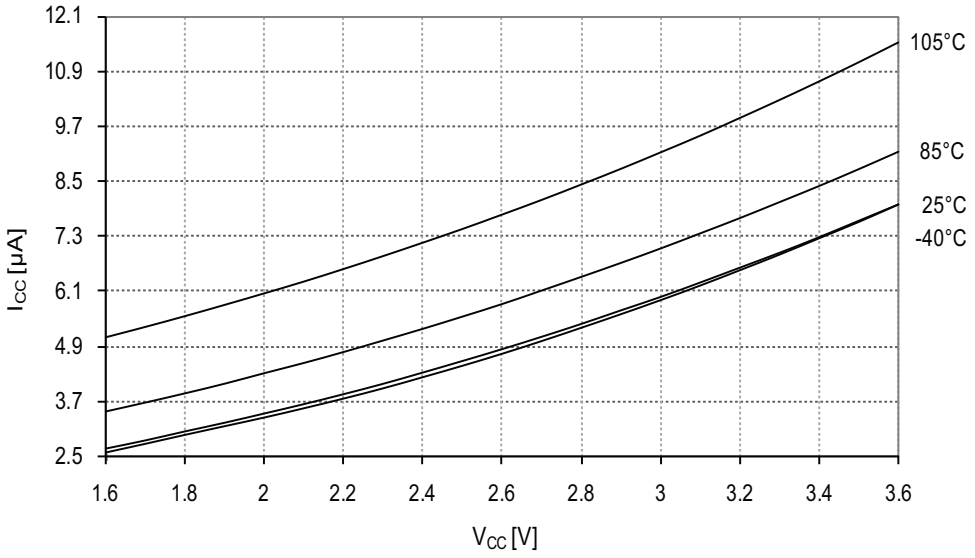


Figure 33-20. Standby Supply Current vs. V_{CC}

25°C, running from different crystal oscillators

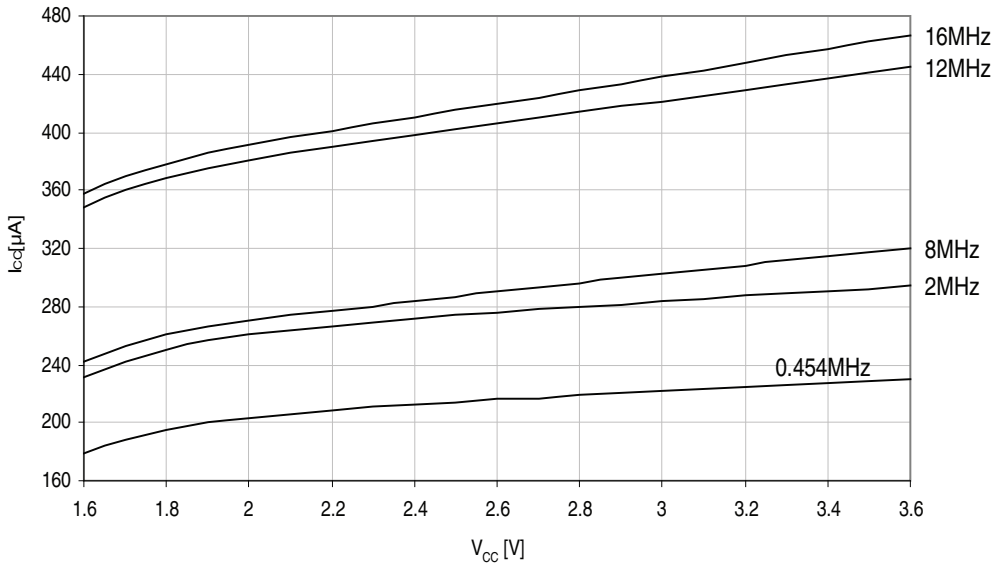


Figure 33-61. Reset Pin Input Threshold Voltage vs. V_{CC}

V_{IH} - Reset pin read as "1"

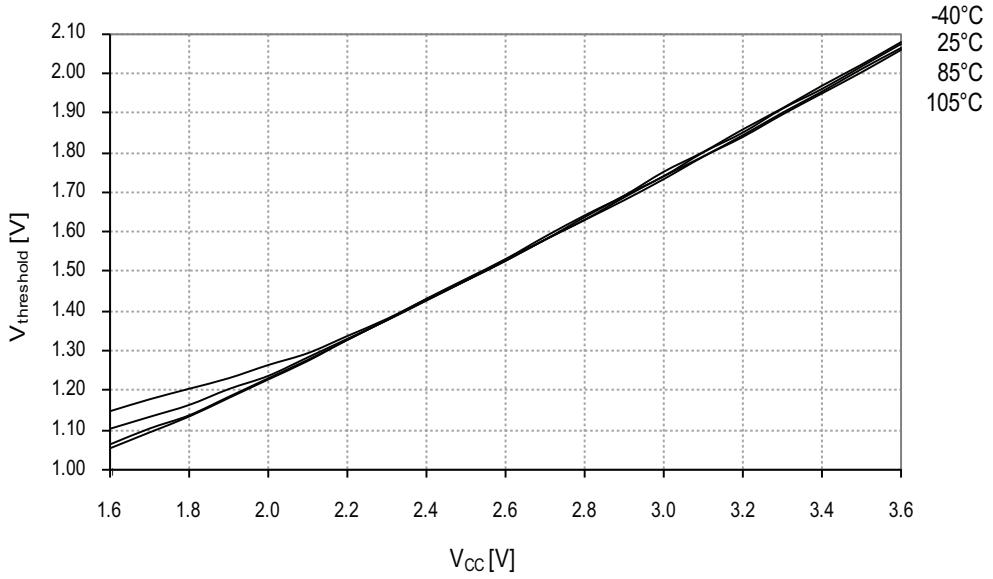


Figure 33-62. Reset Pin Input Threshold Voltage vs. V_{CC}

V_{IL} - Reset pin read as "0"

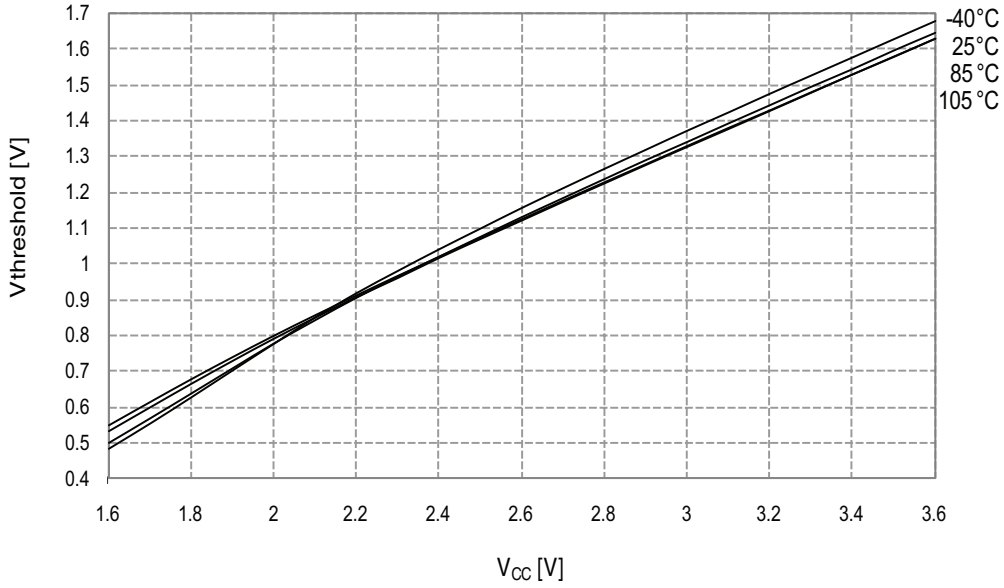


Figure 33-104. I/O Pin Output Voltage vs. Source Current

V_{CC} = 3.0V

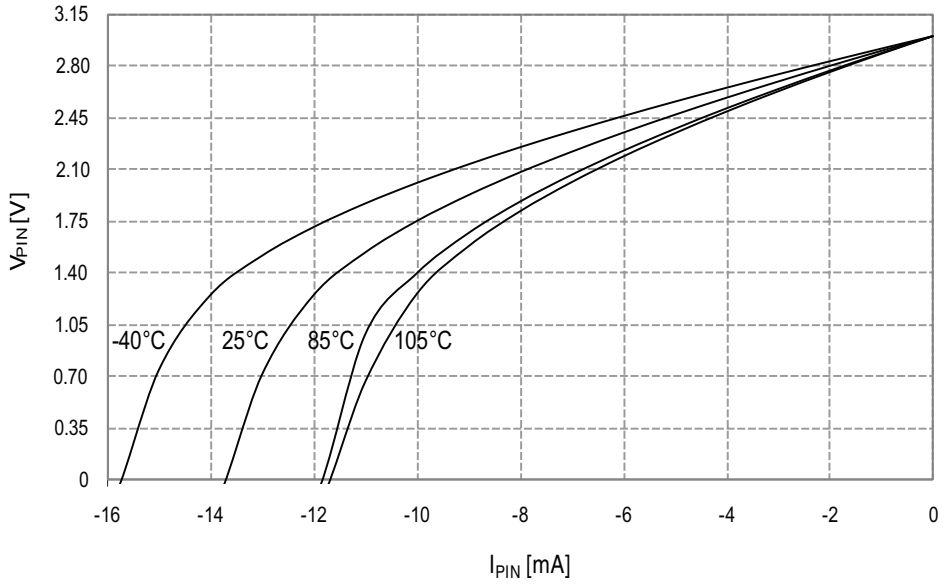


Figure 33-105. I/O Pin Output Voltage vs. Source Current

V_{CC} = 3.3V

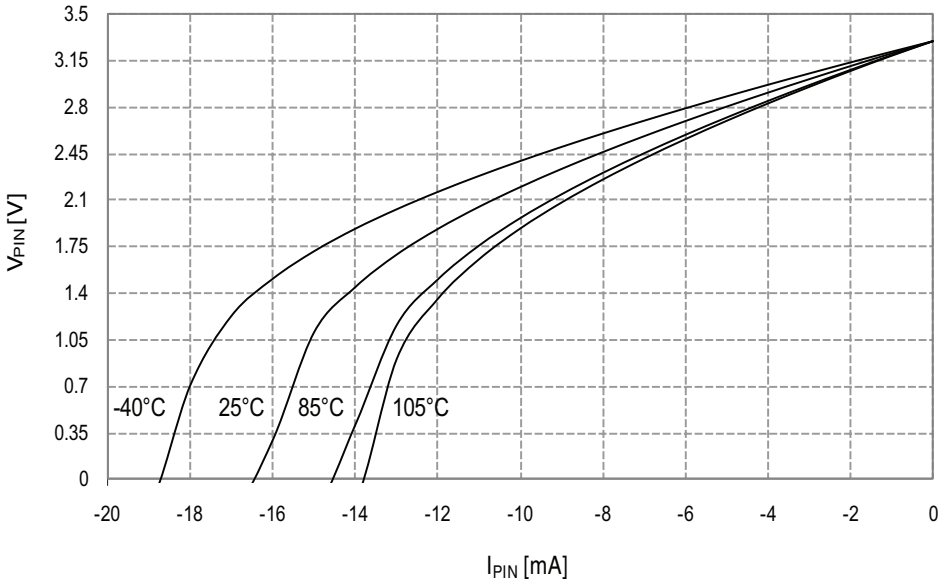


Figure 33-122. Gain Error vs. V_{CC}

T = 25°C, V_{REF} = external 1.0V, ADC sample rate = 200ksps

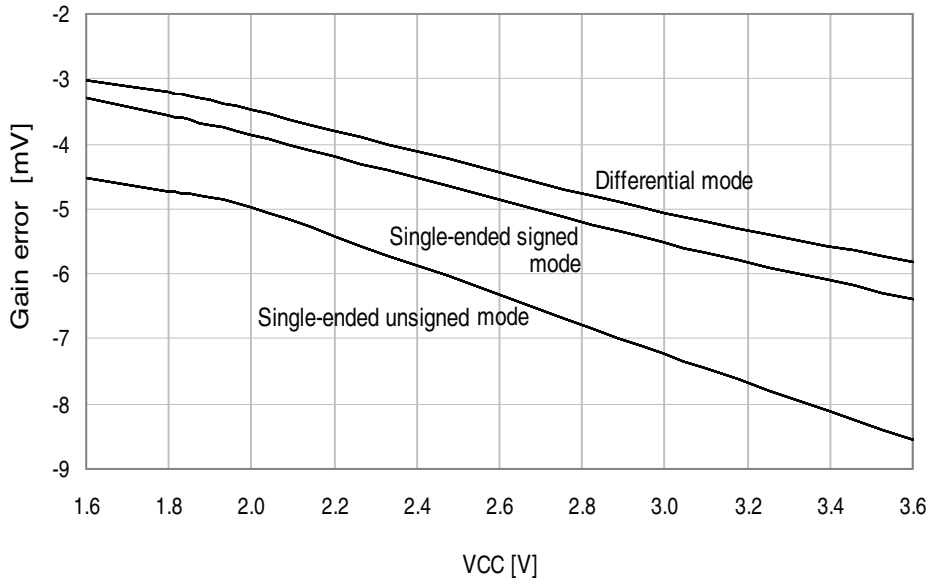


Figure 33-123. Gain Error vs. Temperature

V_{CC} = 3.0V, V_{REF} = external 2.0V

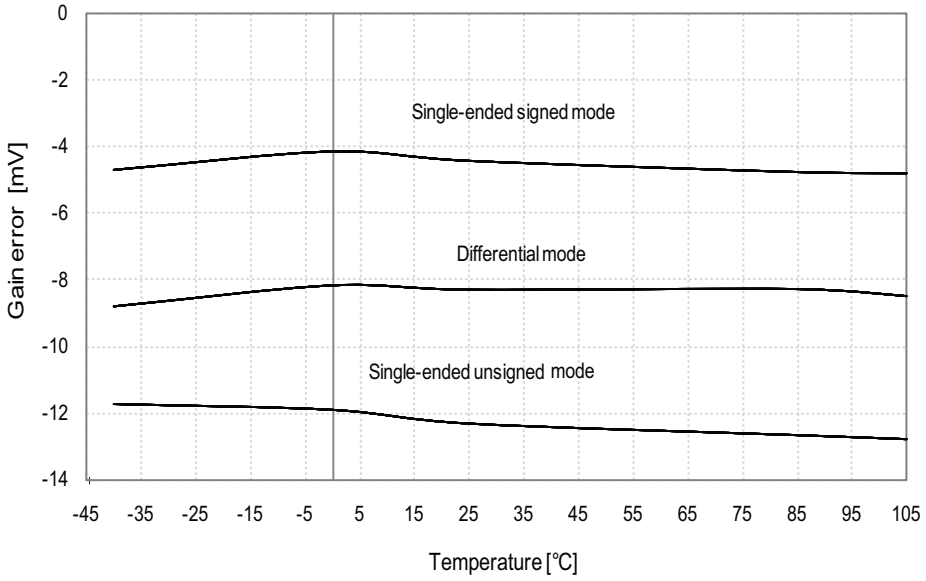


Figure 33-205. Noise vs. V_{REF}

T = 25°C, V_{CC} = 3.6V, ADC sampling speed = 500ksps

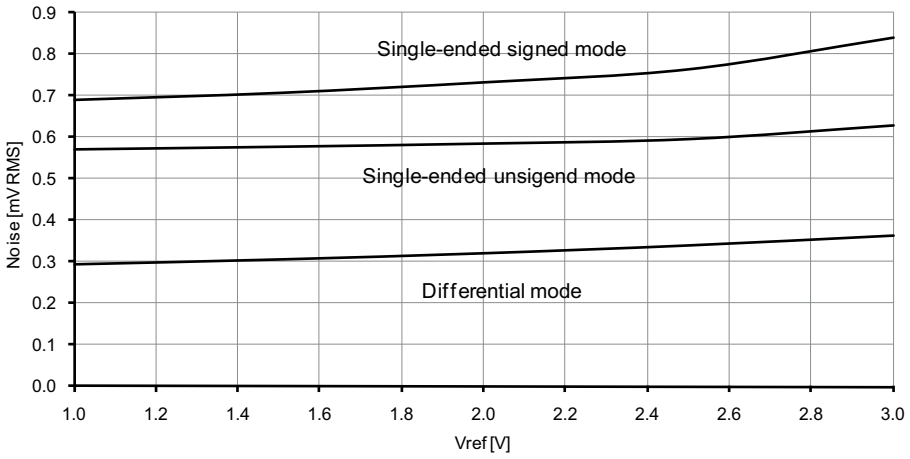


Figure 33-206. Noise vs. V_{CC}

T = 25°C, V_{REF} = external 1.0V, ADC sampling speed = 500ksps

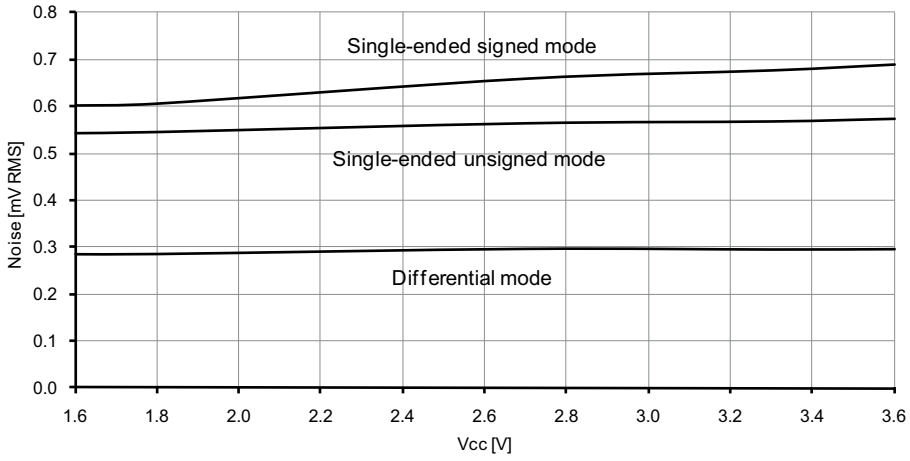


Figure 33-213. Analog Comparator Hysteresis vs. V_{CC}

Low power, large hysteresis

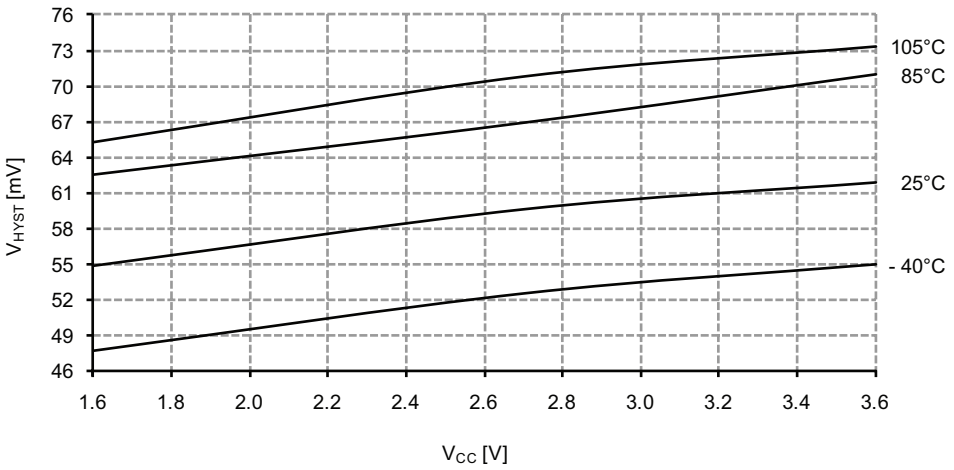


Figure 33-214. Analog Comparator Current Source vs. Calibration Value

Temperature = 25°C

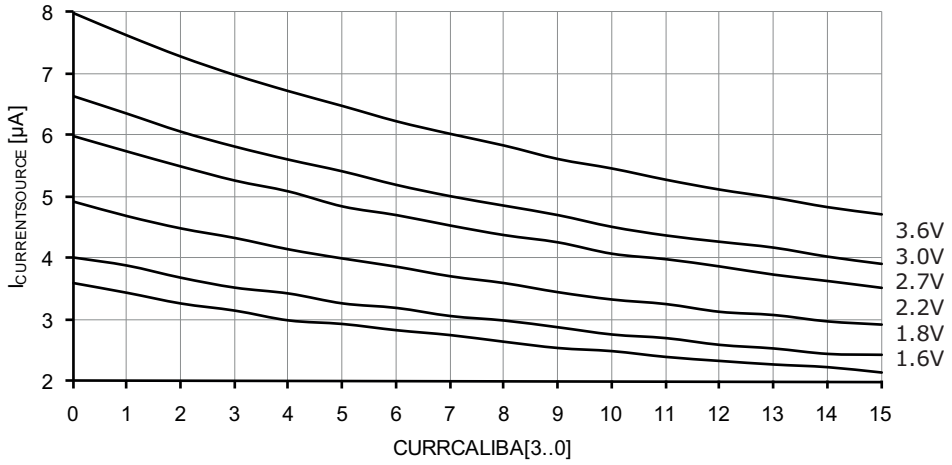


Figure 33-223. Reset Pin Pull-up Resistor Current vs. Reset Pin Voltage

V_{CC} = 3.3V

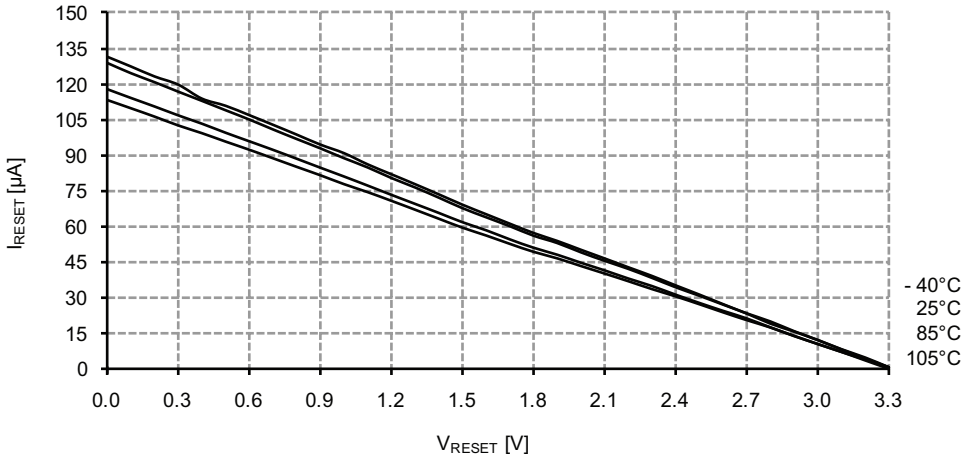


Figure 33-224. Reset Pin Input Threshold Voltage vs. V_{CC}

V_{IH} - Reset pin read as "1"

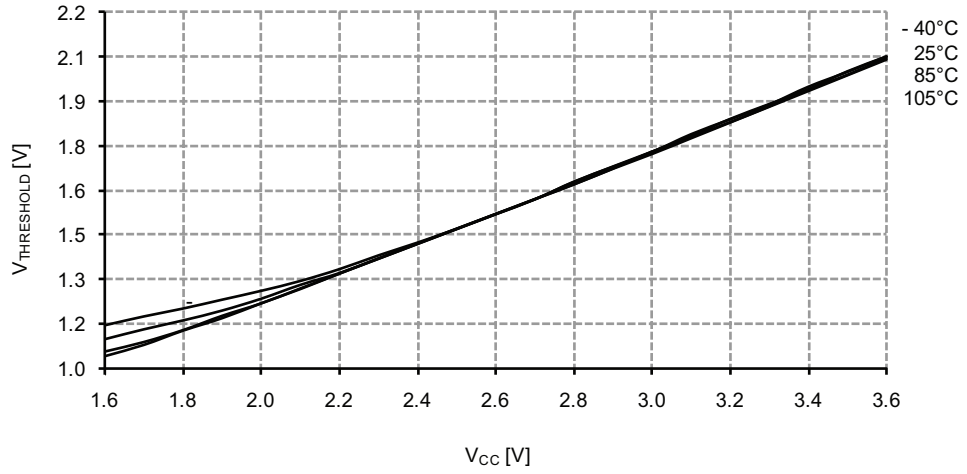


Figure 33-253. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 1MHz external clock

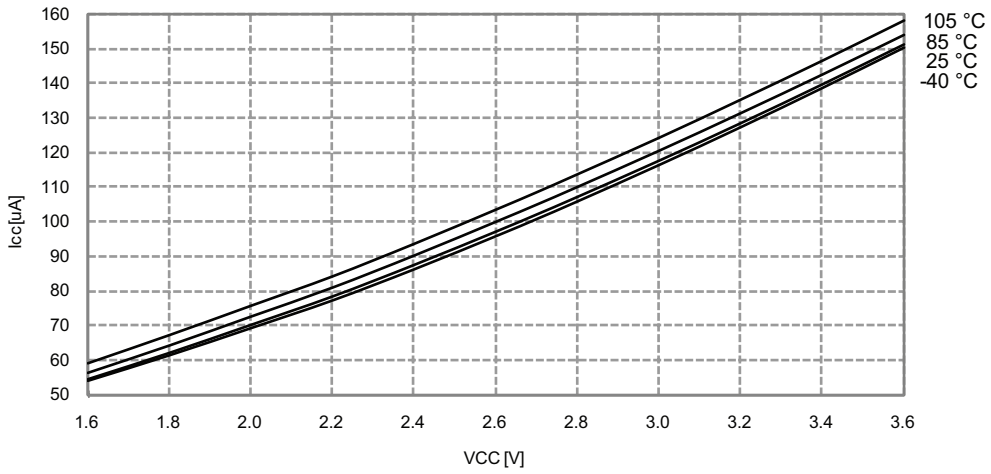


Figure 33-254. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 2MHz internal oscillator

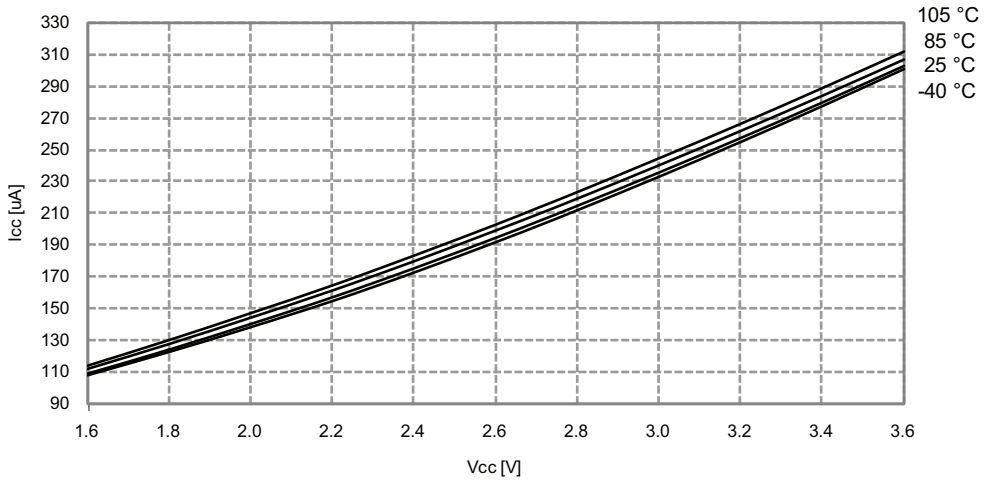
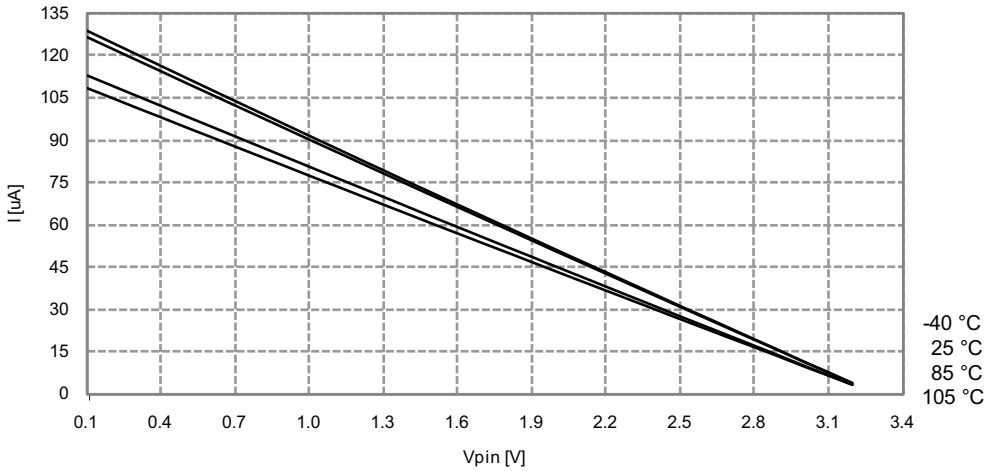


Figure 33-265. I/O Pin Pull-up Resistor Current vs. Input Voltage

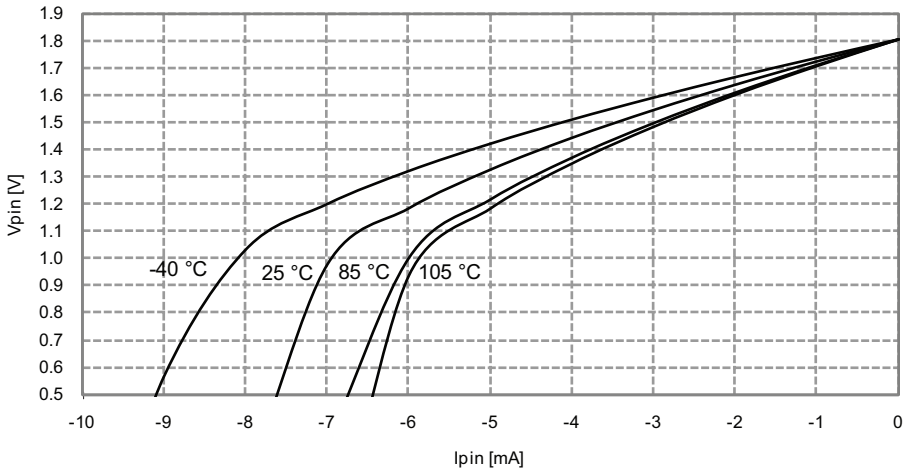
V_{CC} = 3.3V



33.4.2.2 Output Voltage vs. Sink/Source Current

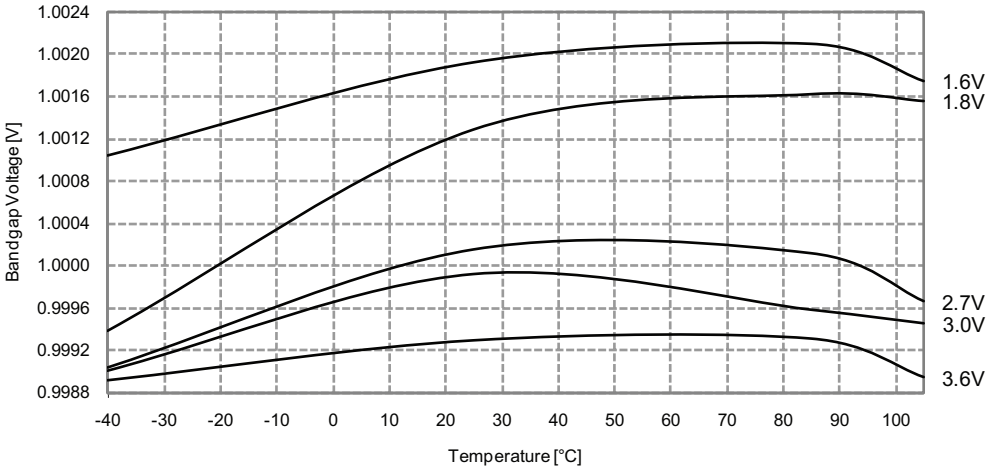
Figure 33-266. I/O Pin Output Voltage vs. Source Current

V_{CC} = 1.8V



33.4.6 Internal 1.0V Reference Characteristics

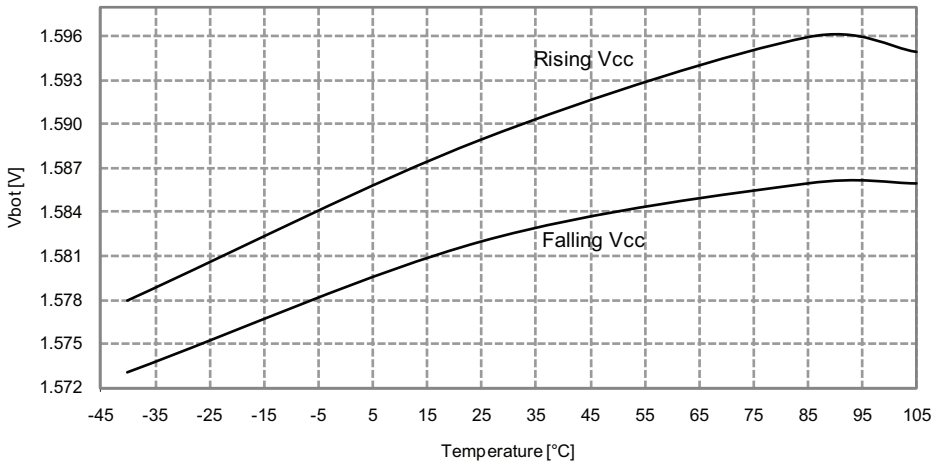
Figure 33-301. ADC/DAC Internal 1.0V Reference vs. Temperature



33.4.7 BOD Characteristics

Figure 33-302. BOD Thresholds vs. Temperature

BOD level = 1.6V



34. Errata

34.1 ATxmega16D4 / ATxmega32D4

34.1.1 Rev. I

- Temperature sensor not calibrated

1. Temperature sensor not calibrated

Temperature sensor factory calibration not implemented.

Problem fix/Workaround

None.

34.1.2 Rev. F/G/H

Not sampled.

34.1.3 Rev. E

- ADC propagation delay is not correct when gain is used
- CRC fails for Range CRC when end address is the last word address of a flash section
- AWeX fault protection restore is not done correct in Pattern Generation Mode
- Erroneous interrupt when using Timer/Counter with QDEC
- AC system status flags are only valid if AC-system is enabled
- Temperature sensor not calibrated

1. ADC propagation delay is not correct when gain is used

The propagation delay will increase by only one ADC clock cycle for all gain setting.

Problem fix/Workaround

None.

2. CRC fails for Range CRC when end address is the last word address of a flash section

If boot read lock is enabled, the range CRC cannot end on the last address of the application section. If application table read lock is enabled, the range CRC cannot end on the last address before the application table.

Problem fix/Workaround

Ensure that the end address used in Range CRC does not end at the last address before a section with read lock enabled. Instead, use the dedicated CRC commands for complete applications sections.

3. AWeX fault protection restore is not done correct in Pattern Generation Mode

When a fault is detected the OUTOVEN register is cleared, and when fault condition is cleared, OUTOVEN is restored according to the corresponding enabled DTI channels. For Common Waveform Channel Mode (CWCM), this has no effect as the OUTOVEN is correct after restoring from fault. For Pattern Generation Mode (PGM), OUTOVEN should instead have been restored according to the DTILSBUF register.

Problem fix/Workaround

Table 34-1. Configure PWM and CWCM According to this Table

PGM	CWCM	Description
0	0	PGM and CWCM disabled
0	1	PGM enabled
1	0	PGM and CWCM enabled
1	1	PGM enabled

10 PWM is not restarted properly after a fault in cycle-by-cycle mode

When the AWeX fault restore mode is set to cycle-by-cycle, the waveform output will not return to normal operation at first update after fault condition is no longer present.

Problem fix/Workaround

Do a write to any AWeX I/O register to re-enable the output.

11. BOD will be enabled after any reset

If any reset source goes active, the BOD will be enabled and keep the device in reset if the VCC voltage is below the programmed BOD level. During Power-On Reset, reset will not be released until VCC is above the programmed BOD level even if the BOD is disabled.

Problem fix/Workaround

Do not set the BOD level higher than VCC even if the BOD is not used.

12. Sampled BOD in Active mode will cause noise when bandgap is used as reference

Using the BOD in sampled mode when the device is running in Active or Idle mode will add noise on the bandgap reference for ADC and Analog Comparator.

Problem fix/Workaround

If the bandgap is used as reference for either the ADC or the Analog Comparator, the BOD must not be set in sampled mode.

13. EEPROM page buffer always written when NVM DATA0 is written

If the EEPROM is memory mapped, writing to NVM DATA0 will corrupt data in the EEPROM page buffer.

Problem fix/Workaround

Before writing to NVM DATA0, for example when doing software CRC or flash page buffer write, check if EEPROM page buffer active loading flag (EELOAD) is set. Do not write NVM DATA0 when EELOAD is set.

14. Pending full asynchronous pin change interrupts will not wake the device

Any full asynchronous pin-change Interrupt from pin 2, on any port, that is pending when the sleep instruction is executed, will be ignored until the device is woken from another source or the source triggers again. This applies when entering all sleep modes where the System Clock is stopped.

Problem fix/Workaround

None.

15. Pin configuration does not affect Analog Comparator output

The Output/Pull and inverted pin configuration does not affect the Analog Comparator output.