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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	34
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega64d4-aur

Ordering Code	Flash (Bytes)	EEPROM (Bytes)	SRAM (Bytes)	Speed (MHz)	Power Supply	Package[1][2][3]	Temp
ATxmega128D4-AN	128K + 8K	2K	8K	32	1.6 - 3.6V	44A	-40°C - 105°C
ATxmega128D4-ANR[4]	128K + 8K	2K	8K				
ATxmega64D4-AN	64K + 4K	2K	4K				
ATxmega64D4-ANR[4]	64K + 4K	2K	4K				
ATxmega32D4-AN	32K + 4K	1K	4K				
ATxmega32D4-ANR[4]	32K + 4K	1K	4K				
ATxmega16D4-AN	16K + 4K	1K	2K				
ATxmega16D4-ANR[4]	16K + 4K	1K	2K				
ATxmega128D4-M7	128K + 8K	2K	8K			44M1	
ATxmega128D4-M7R[4]	128K + 8K	2K	8K				
ATxmega64D4-M7	64K + 4K	2K	4K				
ATxmega64D4-M7R[4]	64K + 4K	2K	4K				
ATxmega32D4-M7	32K + 4K	1K	4K				
ATxmega32D4-M7R[4]	32K + 4K	1K	4K				
ATxmega16D4-M7	16K + 4K	1K	2K				
ATxmega16D4-M7R[4]	16K + 4K	1K	2K				

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For packaging information see "Packaging information" on page 64.
4. Tape and Reel.

Package type	
44A	44-lead, 10*10mm body size, 1.0mm body thickness, 0.8mm lead pitch, thin profile plastic quad flat package (TQFP)
44M1	44-Pad, 7*7*1mm body, lead pitch 0.50mm, 5.20mm exposed pad, thermally enhanced plastic very thin quad no lead package (VQFN)
49C2	49-ball (7 * 7 Array), 0.65mm pitch, 5.0*5.0*1.0mm, very thin, fine-pitch ball grid array package (VFBGA)

Typical Applications

Industrial control	Climate control	Low power battery applications
Factory automation	RF and ZigBee®	Power tools
Building control	USB connectivity	HVAC
Board control	Sensor control	Utility metering
White goods	Optical	Medical applications

7.8 Data Memory and Bus Arbitration

Since the data memory is organized as four separate sets of memories, the bus masters (CPU, etc.) can access different memory sections at the same time.

7.9 Memory Timing

Read and write access to the I/O memory takes one CPU clock cycle. A write to SRAM takes one cycle, and a read from SRAM takes two cycles. EEPROM page load (write) takes one cycle, and three cycles are required for read. For burst read, new data are available every second cycle. Refer to the instruction summary for more details on instructions and instruction timing.

7.10 Device ID and Revision

Each device has a three-byte device ID. This ID identifies Atmel as the manufacturer of the device and the device type. A separate register contains the revision number of the device.

7.11 I/O Memory Protection

Some features in the device are regarded as critical for safety in some applications. Due to this, it is possible to lock the I/O register related to the clock system, the event system, and the advanced waveform extensions. As long as the lock is enabled, all related I/O registers are locked and they can not be written from the application software. The lock registers themselves are protected by the configuration change protection mechanism.

7.12 Flash and EEPROM Page Size

The flash program memory and EEPROM data memory are organized in pages. The pages are word accessible for the flash and byte accessible for the EEPROM.

Table 7-2 on page 16 shows the Flash Program Memory organization and Program Counter (PC) size. Flash write and erase operations are performed on one page at a time, while reading the Flash is done one byte at a time. For Flash access the Z-pointer (Z[m:n]) is used for addressing. The most significant bits in the address (FPAGE) give the page number and the least significant address bits (FWORD) give the word in the page.

Table 7-2. Number of Words and Pages in the Flash

Devices	PC size	Flash size	Page Size	FWORD	FPAGE	Application		Boot	
	bits	bytes	words			Size	No of pages	Size	No of pages
ATxmega16D4	14	16K + 4K	128	Z[7:1]	Z[13:8]	16K	64	4K	16
ATxmega32D4	15	32K + 4K	128	Z[7:1]	Z[14:8]	32K	128	4K	16
ATxmega64D4	16	64K + 4K	128	Z[7:1]	Z[15:8]	64K	256	4K	16
ATxmega128D4	17	128K + 8K	128	Z[9:1]	Z[16:8]	128K	512	8K	32

Table 7-3 on page 17 shows EEPROM memory organization for the Atmel AVR XMEGA D4 devices. EEEPROM write and erase operations can be performed one page or one byte at a time, while reading the EEPROM is done one byte at a time. For EEPROM access the NVM address register (ADDR[m:n]) is used for addressing. The most significant bits in the address (E2PAGE) give the page number and the least significant address bits (E2BYTE) give the byte in the page.

1kHz output. The oscillator is automatically enabled/disabled when it is used as clock source for any part of the device. This oscillator can be selected as the clock source for the RTC.

9.3.2 32.768kHz Calibrated Internal Oscillator

This oscillator provides an approximate 32.768kHz clock. It is calibrated during production to provide a default frequency close to its nominal frequency. The calibration register can also be written from software for run-time calibration of the oscillator frequency. The oscillator employs a built-in prescaler, which provides both a 32.768kHz output and a 1.024kHz output.

9.3.3 32.768kHz Crystal Oscillator

A 32.768kHz crystal oscillator can be connected between the TOSC1 and TOSC2 pins and enables a dedicated low frequency oscillator input circuit. A low power mode with reduced voltage swing on TOSC2 is available. This oscillator can be used as a clock source for the system clock and RTC, and as the DFLL reference clock.

9.3.4 0.4 - 16MHz Crystal Oscillator

This oscillator can operate in four different modes optimized for different frequency ranges, all within 0.4 - 16MHz.

9.3.5 2MHz Run-time Calibrated Internal Oscillator

The 2MHz run-time calibrated internal oscillator is the default system clock source after reset. It is calibrated during production to provide a default frequency close to its nominal frequency. A DFLL can be enabled for automatic run-time calibration of the oscillator to compensate for temperature and voltage drift and optimize the oscillator accuracy.

9.3.6 32MHz Run-time Calibrated Internal Oscillator

The 32MHz run-time calibrated internal oscillator is a high-frequency oscillator. It is calibrated during production to provide a default frequency close to its nominal frequency. A digital frequency looked loop (DFLL) can be enabled for automatic run-time calibration of the oscillator to compensate for temperature and voltage drift and optimize the oscillator accuracy. This oscillator can also be adjusted and calibrated to any frequency between 30MHz and 55MHz.

9.3.7 External Clock Sources

The XTAL1 and XTAL2 pins can be used to drive an external oscillator, either a quartz crystal or a ceramic resonator. XTAL1 can be used as input for an external clock signal. The TOSC1 and TOSC2 pins is dedicated to driving a 32.768kHz crystal oscillator.

9.3.8 PLL with 1x-31x Multiplication Factor

The built-in phase locked loop (PLL) can be used to generate a high-frequency system clock. The PLL has a user-selectable multiplication factor of from 1 to 31. In combination with the prescalers, this gives a wide range of output frequencies from all clock sources.

17. AWeX – Advanced Waveform Extension

17.1 Features

- Waveform output with complementary output from each compare channel
- Four dead-time insertion (DTI) units
  - 8-bit resolution
  - Separate high and low side dead-time setting
  - Double buffered dead time
  - Optionally halts timer during dead-time insertion
- Pattern generation unit creating synchronised bit pattern across the port pins
  - Double buffered pattern generation
  - Optional distribution of one compare channel output across the port pins
- Event controlled fault protection for instant and predictable fault triggering

17.2 Overview

The advanced waveform extension (AWeX) provides extra functions to the timer/counter in waveform generation (WG) modes. It is primarily intended for use with different types of motor control and other power control applications. It enables low- and high side output with dead-time insertion and fault protection for disabling and shutting down external drivers. It can also generate a synchronized bit pattern across the port pins.

Each of the waveform generator outputs from the timer/counter 0 are split into a complimentary pair of outputs when any AWeX features are enabled. These output pairs go through a dead-time insertion (DTI) unit that generates the non-inverted low side (LS) and inverted high side (HS) of the WG output with dead-time insertion between LS and HS switching. The DTI output will override the normal port value according to the port override setting.

The pattern generation unit can be used to generate a synchronized bit pattern on the port it is connected to. In addition, the WG output from compare channel A can be distributed to and override all the port pins. When the pattern generator unit is enabled, the DTI unit is bypassed.

The fault protection unit is connected to the event system, enabling any event to trigger a fault condition that will disable the AWeX output. The event system ensures predictable and instant fault reaction, and gives flexibility in the selection of fault triggers.

The AWeX is available for TCC0. The notation of this is AWEXC.

25. ADC – 12-bit Analog to Digital Converter

25.1 Features

- One Analog to Digital Converters (ADC)
- 12-bit resolution
- Up to 200 thousand samples per second
  - Down to 3.6µs conversion time with 8-bit resolution
  - Down to 5.0µs conversion time with 12-bit resolution
- Differential and single-ended input
  - Up to 12 single-ended inputs
  - 12x4 differential inputs without gain
  - 12x4 differential input with gain
- Built-in differential gain stage
  - 1/2x, 1x, 2x, 4x, 8x, 16x, 32x, and 64x gain options
- Single, continuous and scan conversion options
- Three internal inputs
  - Internal temperature sensor
  - AV_{CC} voltage divided by 10
  - 1.1V bandgap voltage
- Internal and external reference options
- Compare function for accurate monitoring of user defined thresholds
- Optional event triggered conversion for accurate timing
- Optional interrupt/event on compare result

25.2 Overview

The ADC converts analog signals to digital values. The ADC has 12-bit resolution and is capable of converting up to 200 thousand samples per second (ksps). The input selection is flexible, and both single-ended and differential measurements can be done. For differential measurements, an optional gain stage is available to increase the dynamic range. In addition, several internal signal inputs are available. The ADC can provide both signed and unsigned results.

The ADC measurements can either be started by application software or an incoming event from another peripheral in the device. The ADC measurements can be started with predictable timing, and without software intervention.

Both internal and external reference voltages can be used. An integrated temperature sensor is available for use with the ADC. The AV_{CC}/10 and the bandgap voltage can also be measured by the ADC.

The ADC has a compare function for accurate monitoring of user defined thresholds with minimum software intervention required.

28.2 Alternate Pin Functions

The tables below show the primary/default function for each pin on a port in the first column, the pin number in the second column, and then all alternate pin functions in the remaining columns. The head row shows what peripheral that enable and use the alternate pin functions.

For better flexibility, some alternate functions also have selectable pin locations for their functions, this is noted under the first table where this apply.

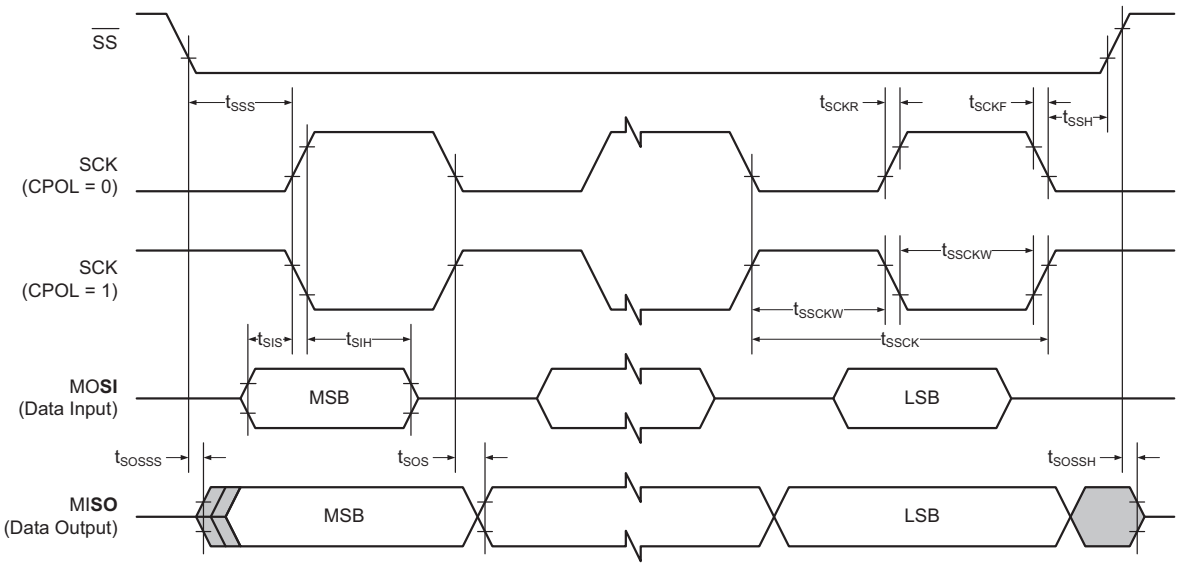
Table 28-1. Port A - Alternate Functions

PORT A	PIN#	INTERRUPT	ADCA POS/GAINPOS	ADCA NEG	ADCA GAINNEG	ACAPOS	ACANEG	ACAOUT	REFA
GND	38								
AVCC	39								
PA0	40	SYNC	ADC0	ADC0		AC0	AC0		AREF
PA1	41	SYNC	ADC1	ADC1		AC1	AC1		
PA2	42	SYNC/ASYNC	ADC2	ADC2		AC2			
PA3	43	SYNC	ADC3	ADC3		AC3	AC3		
PA4	44	SYNC	ADC4		ADC4	AC4			
PA5	1	SYNC	ADC5		ADC5	AC5	AC5		
PA6	2	SYNC	ADC6		ADC6	AC6			
PA7	3	SYNC	ADC7		ADC7		AC7	AC0OUT	

Table 28-2. Port B - Alternate Functions

PORT B	PIN#	INTERRUPT	ADCAPOS/GAINPOS	REFB
PB0	4	SYNC	ADC8	AREF
PB1	5	SYNC	ADC9	
PB2	6	SYNC/ASYNC	ADC10	
PB3	7	SYNC	ADC11	

Figure 32-6. SPI Timing Requirements in Slave Mode



32.2 ATxmega32D4

32.2.1 Absolute Maximum Ratings

Stresses beyond those listed in Table 32-29 under may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 32-29. Absolute Maximum Ratings

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		-0.3		4	V
I_{VCC}	Current into a V_{CC} pin				200	mA
I_{GND}	Current out of a Gnd pin				200	
V_{PIN}	Pin voltage with respect to Gnd and V_{CC}		-0.5		V_{CC}+0.5	V
I_{PIN}	I/O pin sink/source current		-25		25	mA
T_A	Storage temperature		-65		150	°C
T_j	Junction temperature				150	

32.2.2 General Operating Ratings

The device must operate within the ratings listed in Table 32-30 in order for all other electrical characteristics and typical characteristics of the device to be valid.

Table 32-30. General Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		1.60		3.6	V
AV_{CC}	Analog supply voltage		1.60		3.6	
T_A	Temperature range		-40		85	°C
T_j	Junction temperature		-40		105	

Table 32-31. Operating Voltage and Frequency

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{CPU}	CPU clock frequency	V_{CC} = 1.6V	0		12	MHz
		V_{CC} = 1.8V	0		12	
		V_{CC} = 2.7V	0		32	
		V_{CC} = 3.6V	0		32	

The maximum CPU clock frequency depends on V_{CC}. As shown in Figure 32-8 the Frequency vs. V_{CC} curve is linear between 1.8V < V_{CC} < 2.7V.

Figure 33-13. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator prescaled to 8MHz

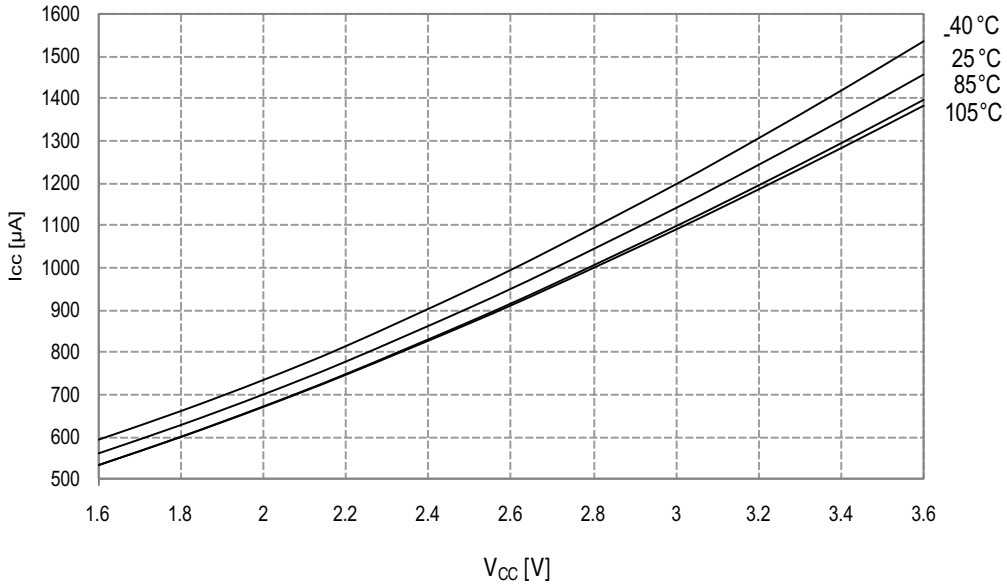


Figure 33-14. Idle Mode Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator

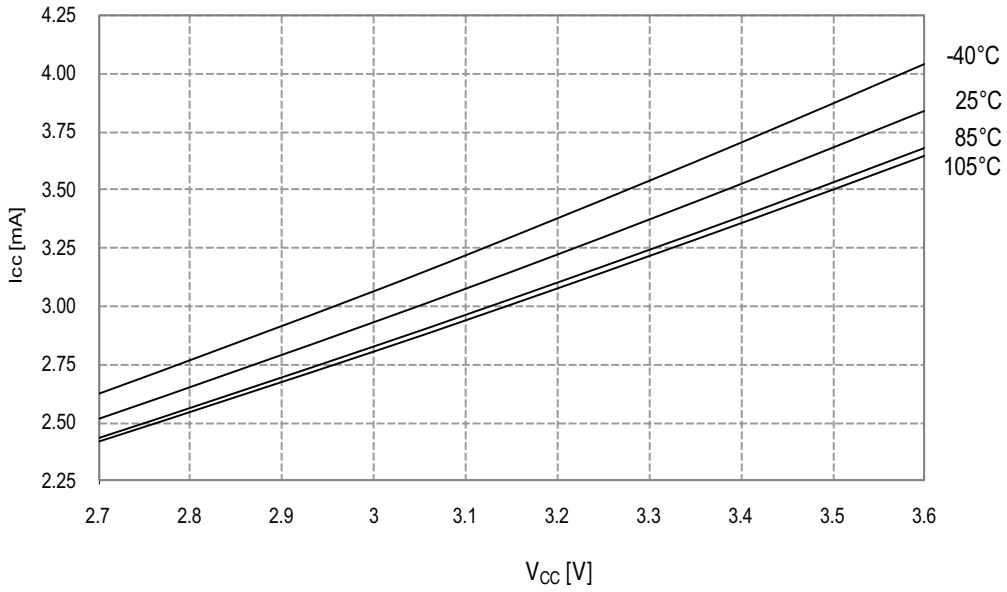


Figure 33-82. Active Mode Supply Current vs. V_{CC}

f_{SYS} = 32.768kHz internal oscillator

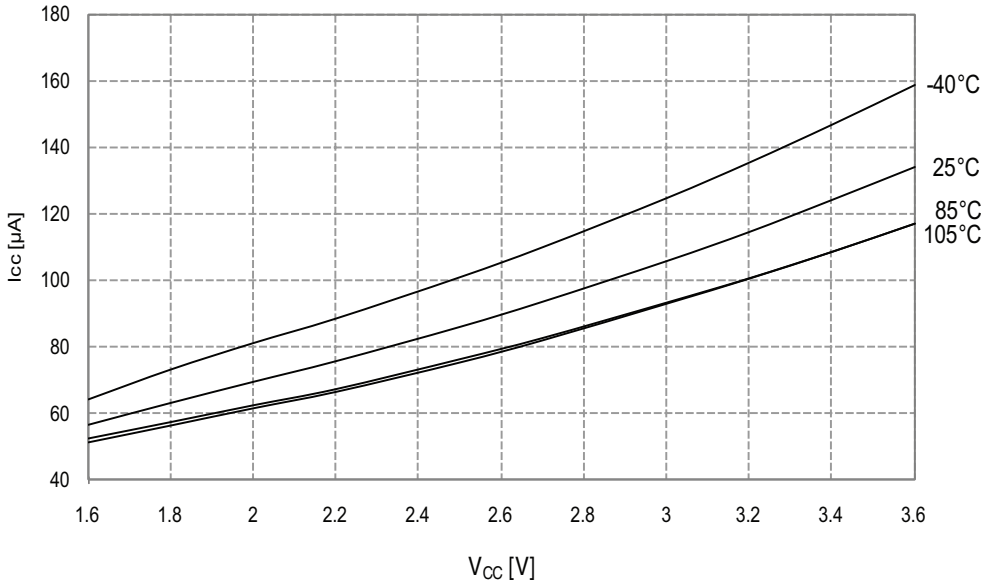


Figure 33-83. Active Mode Supply Current vs. V_{CC}

f_{SYS} = 1MHz external clock

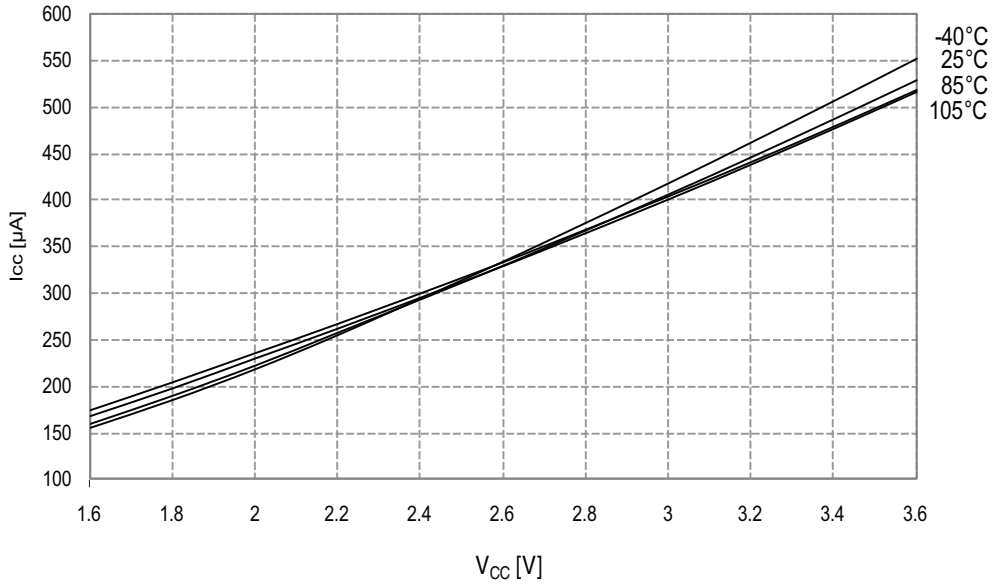


Figure 33-106. I/O Pin Output Voltage vs. Source Current

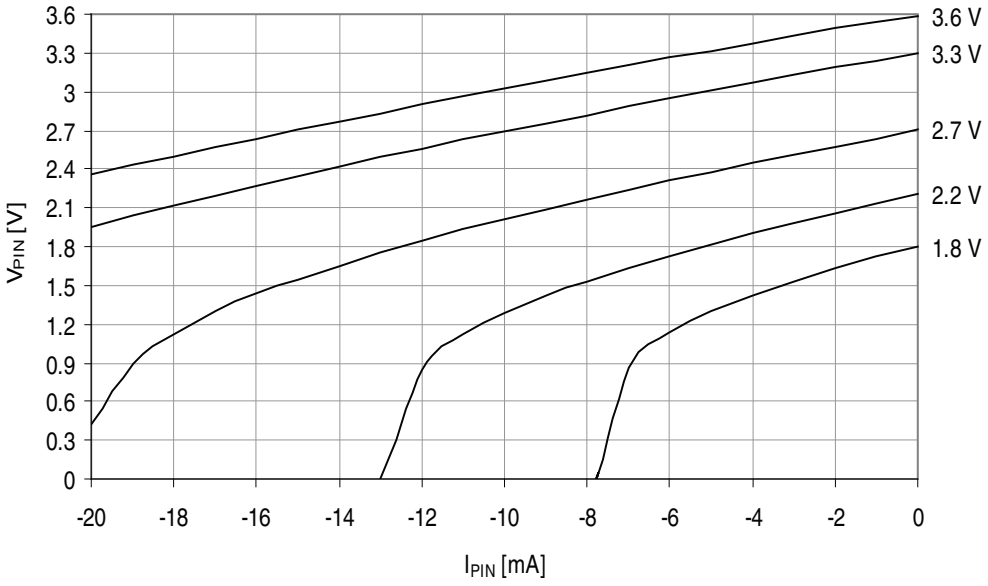


Figure 33-107. I/O Pin Output Voltage vs. Sink Current

V_{CC} = 1.8V

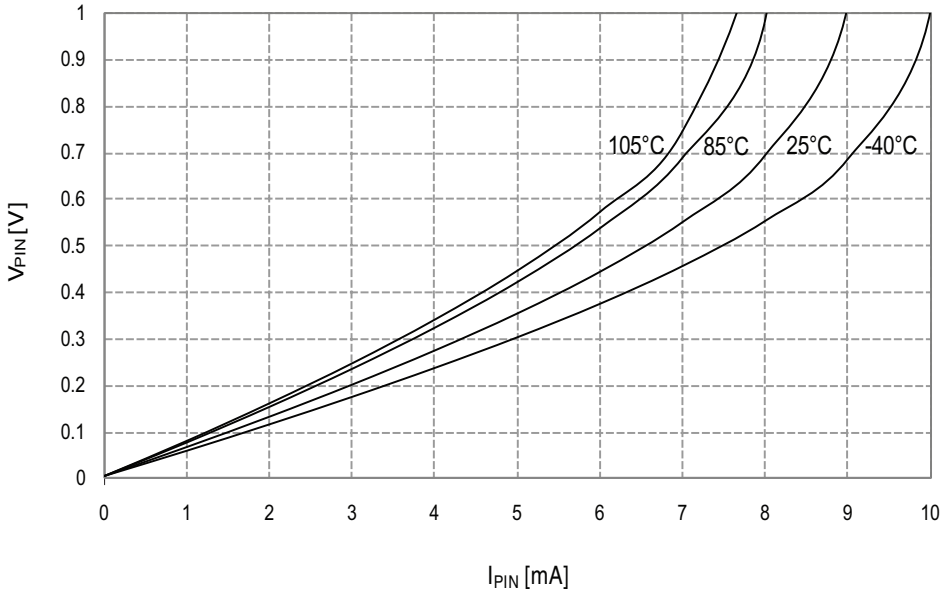


Figure 33-120. DNL Error vs. Input code

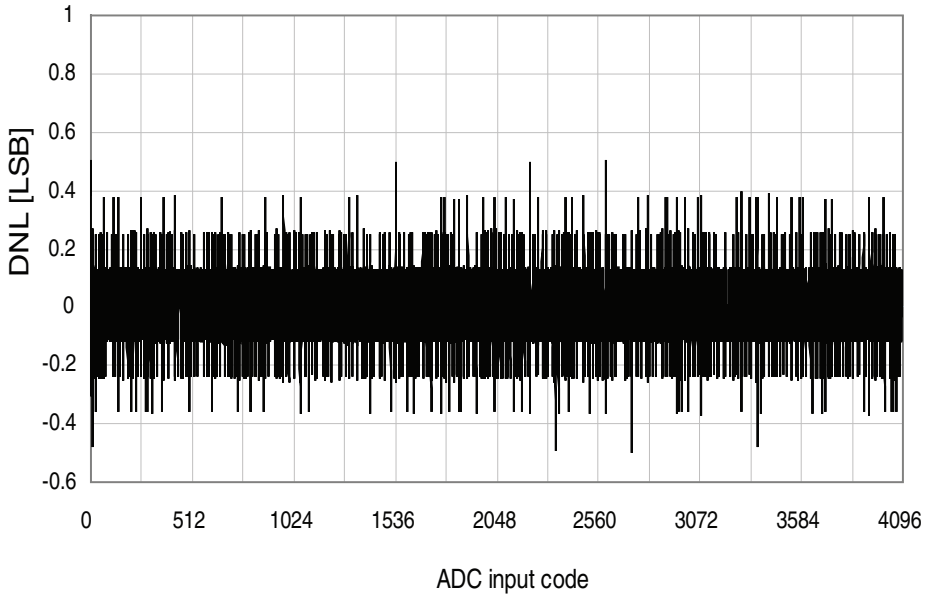
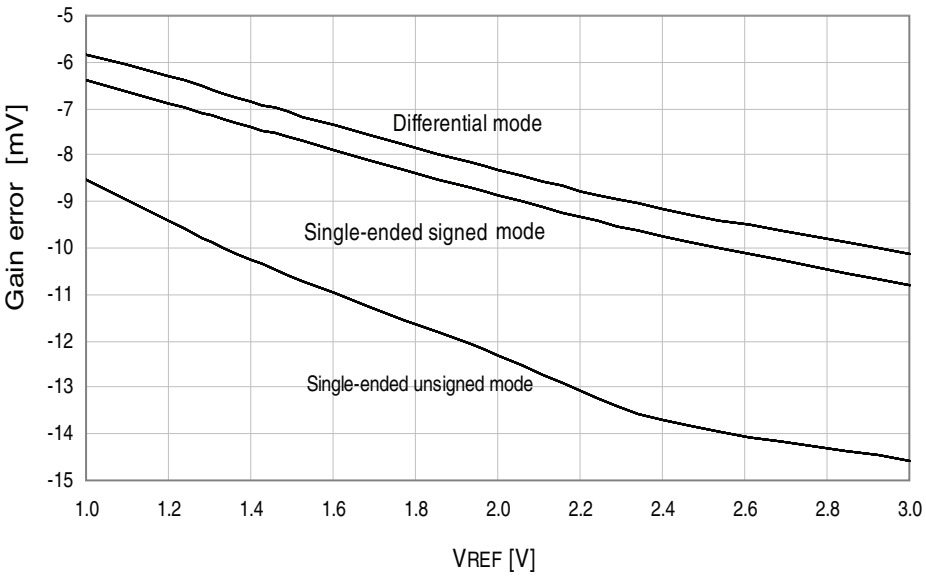


Figure 33-121. Gain Error vs. V_{REF}

T = 25°C, V_{CC} = 3.6V, ADC sample rate = 200ksps



33.2.10 Two-Wire Interface Characteristics

Figure 33-156. SDA Hold Time vs. Temperature

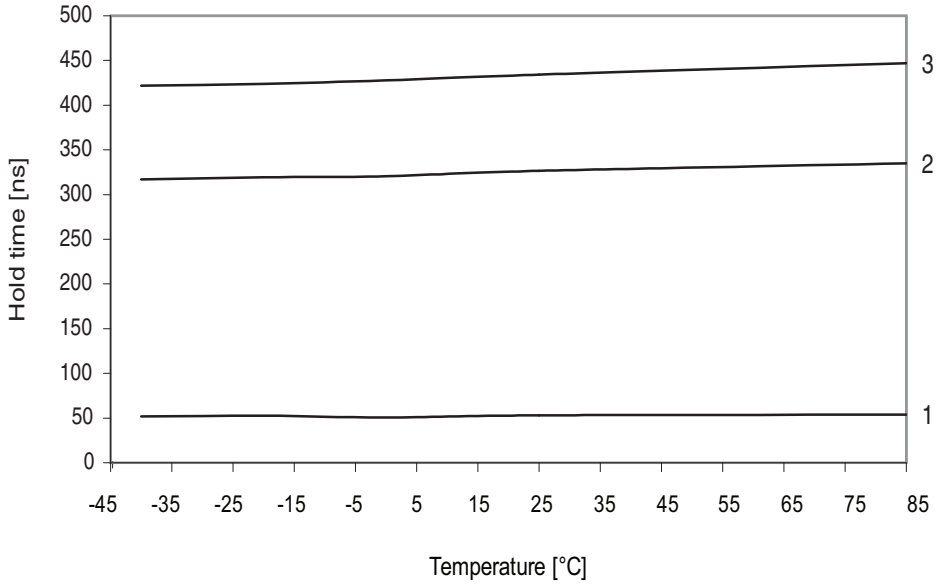


Figure 33-157. SDA Hold Time vs. Supply Voltage

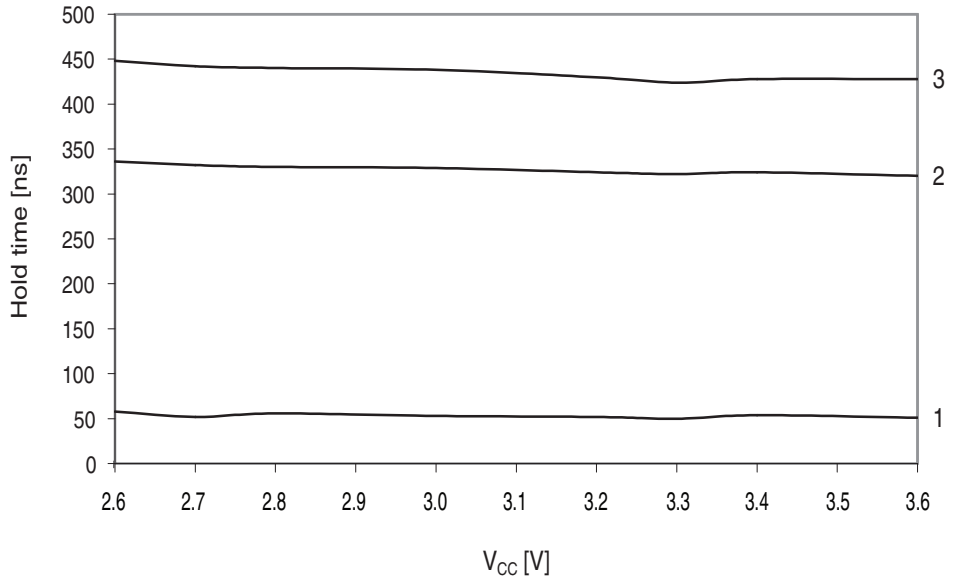


Figure 33-171. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator prescaled to 8MHz

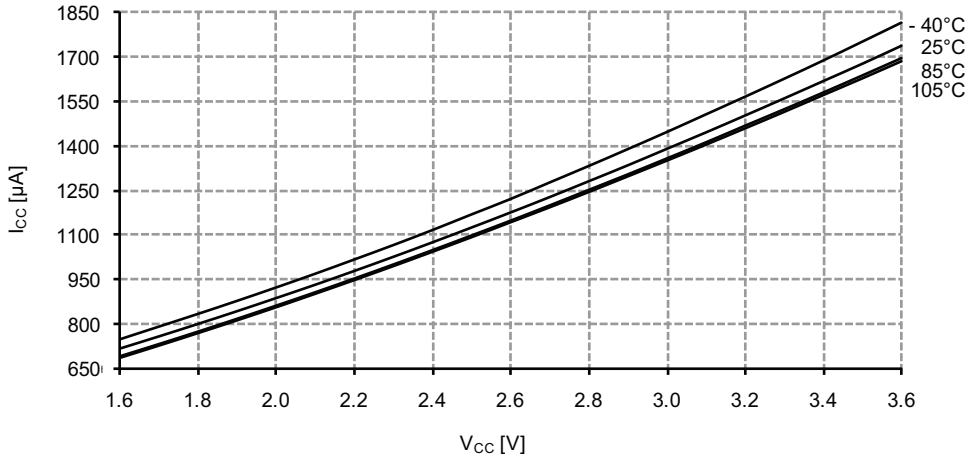


Figure 33-172. Idle Mode Current vs. V_{CC}

f_{SYS} = 32MHz internal oscillator

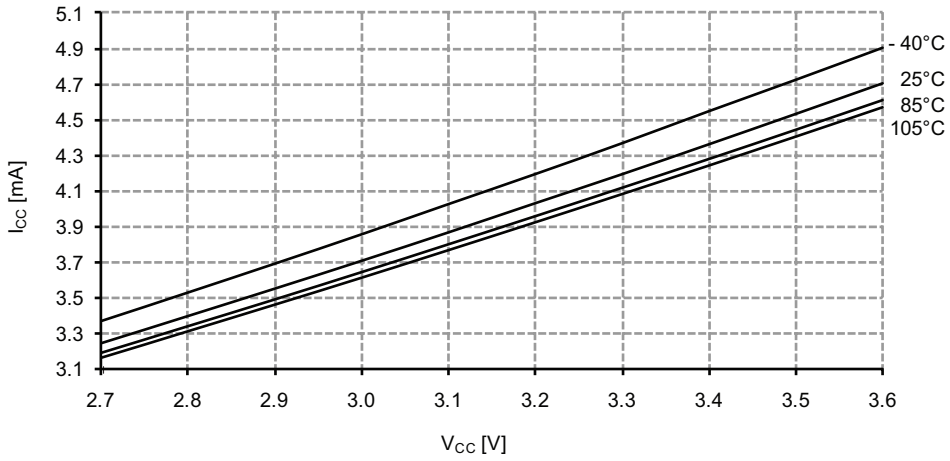


Figure 33-199. DNL Error vs. Input Code

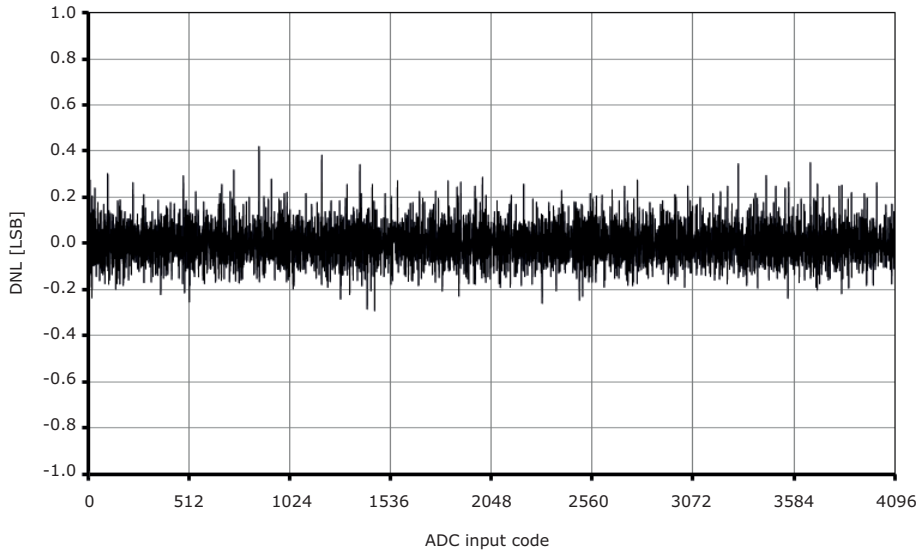


Figure 33-200. Gain Error vs. V_{REF}

T = 25°C, V_{CC} = 3.6V, ADC sampling speed = 500ksps

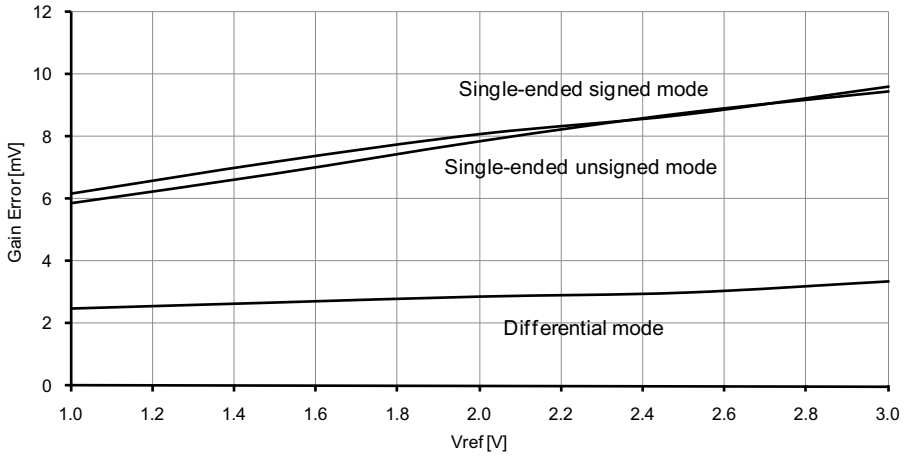


Figure 33-213. Analog Comparator Hysteresis vs. V_{CC}

Low power, large hysteresis

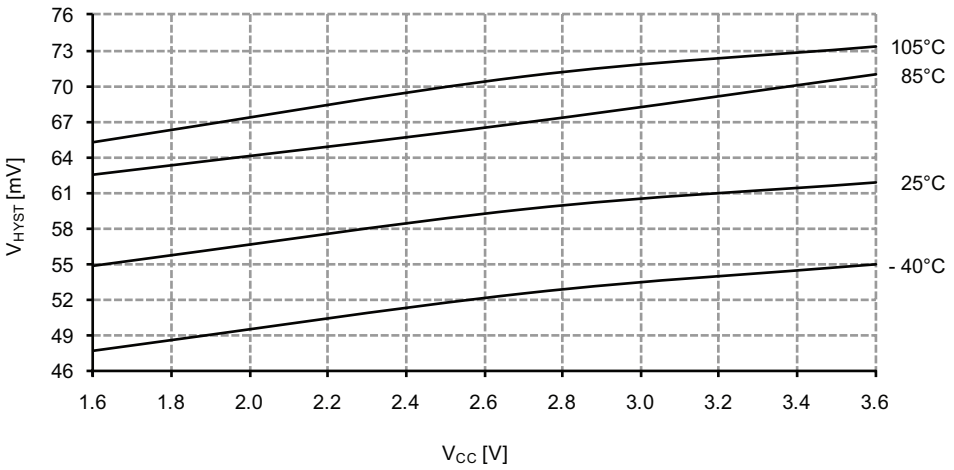


Figure 33-214. Analog Comparator Current Source vs. Calibration Value

Temperature = 25°C

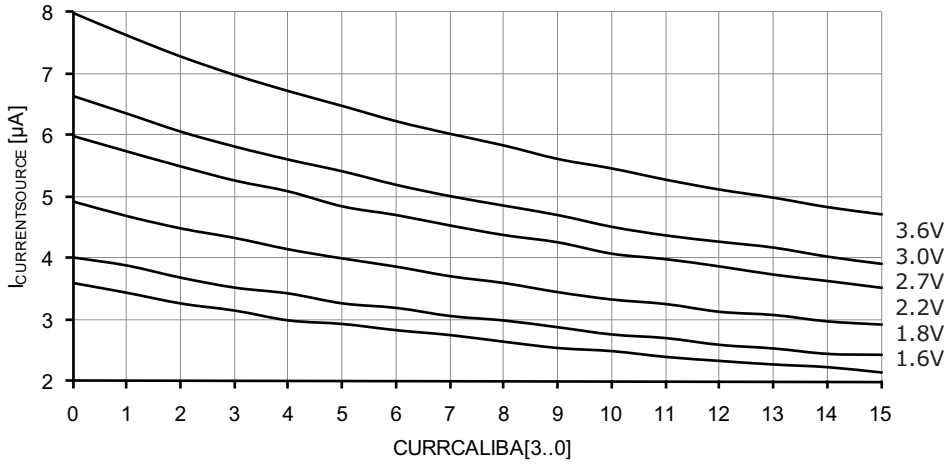


Figure 33-215. Analog Comparator Current Source vs. Calibration Value

V_{CC} = 3.0V

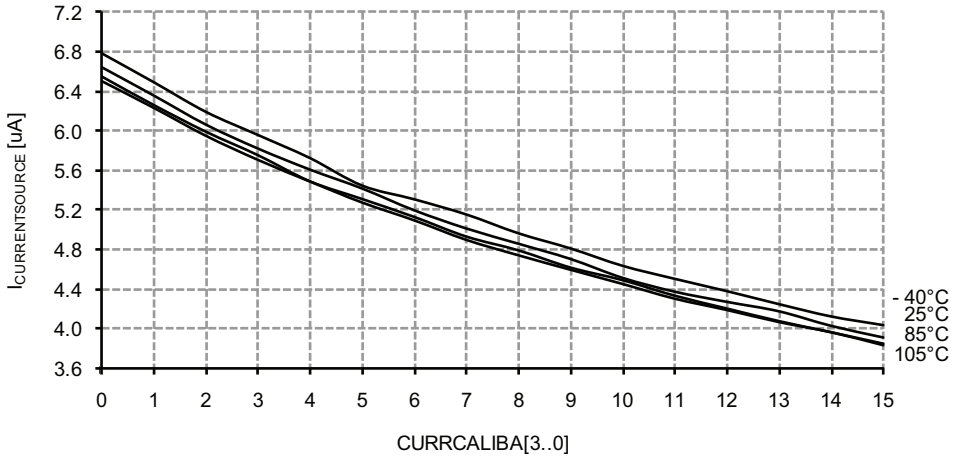


Figure 33-216. Voltage Scaler INL vs. SCALEFAC

T = 25°C, V_{CC} = 3.0V

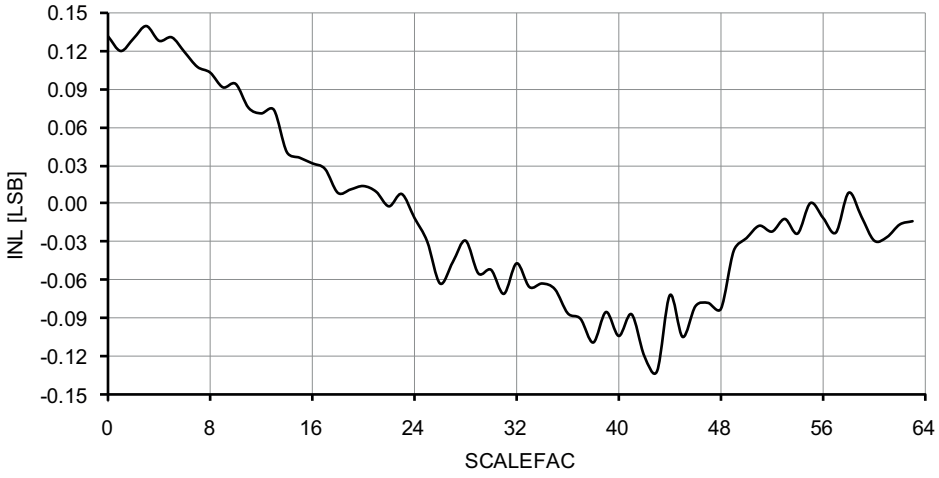
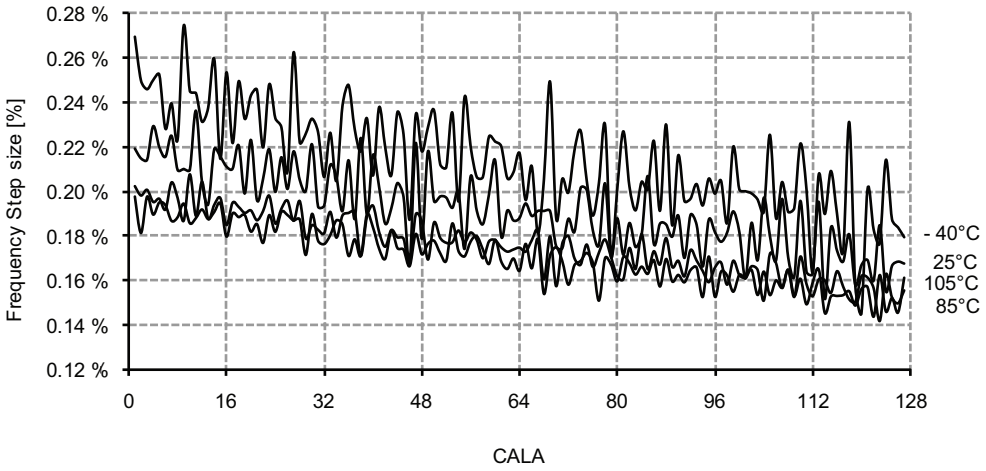


Figure 33-233. 2MHz Internal Oscillator CALA Calibration Step Size

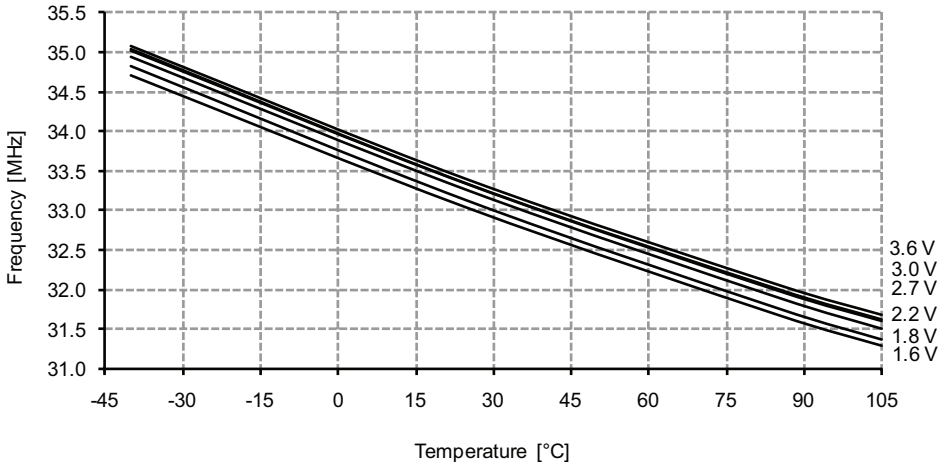
V_{CC} = 3V



33.3.10.4 32MHz Internal Oscillator

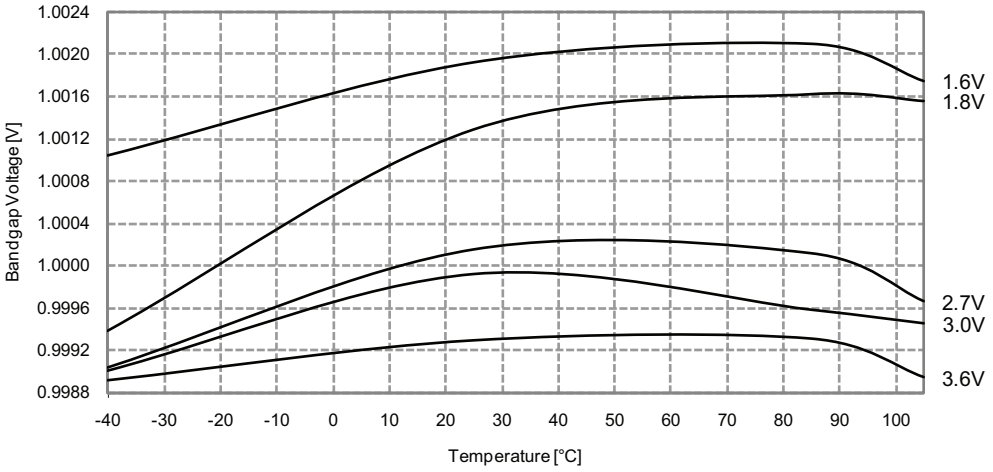
Figure 33-234. 32MHz Internal Oscillator Frequency vs. Temperature

DFLL disabled



33.4.6 Internal 1.0V Reference Characteristics

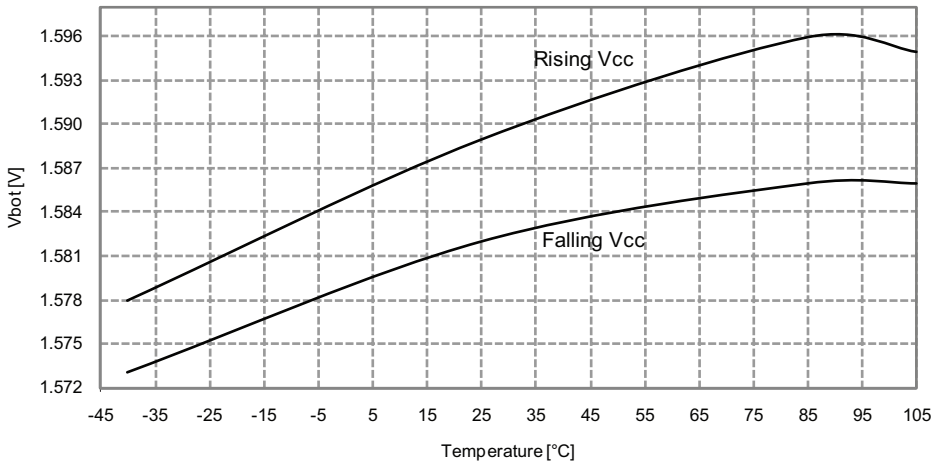
Figure 33-301. ADC/DAC Internal 1.0V Reference vs. Temperature



33.4.7 BOD Characteristics

Figure 33-302. BOD Thresholds vs. Temperature

BOD level = 1.6V



34.1.5 Rev. A/B

- Bandgap voltage input for the ACs can not be changed when used for both ACs simultaneously
- VCC voltage scaler for AC is non-linear
- ADC gain stage cannot be used for single conversion
- ADC has increased INL error for some operating conditions
- ADC gain stage output range is limited to 2.4 V
- ADC Event on compare match non-functional
- ADC propagation delay is not correct when 8x -64x gain is used
- Bandgap measurement with the ADC is non-functional when VCC is below 2.7V
- Accuracy lost on first three samples after switching input to ADC gain stage
- Configuration of PGM and CWCM not as described in XMEGA A Manual
- PWM is not restarted properly after a fault in cycle-by-cycle mode
- BOD: BOD will be enabled at any reset
- Sampled BOD in Active mode will cause noise when bandgap is used as reference
- EEPROM page buffer always written when NVM DATA0 is written
- Pending full asynchronous pin change interrupts will not wake the device
- Pin configuration does not affect Analog Comparator Output
- NMI Flag for Crystal Oscillator Failure automatically cleared
- Flash Power Reduction Mode can not be enabled when entering sleep
- Crystal start-up time required after power-save even if crystal is source for RTC
- RTC Counter value not correctly read after sleep
- Pending asynchronous RTC-interrupts will not wake up device
- TWI Transmit collision flag not cleared on repeated start
- Clearing TWI Stop Interrupt Flag may lock the bus
- TWI START condition at bus timeout will cause transaction to be dropped
- TWI Data Interrupt Flag (DIF) erroneously read as set
- WDR instruction inside closed window will not issue reset
- Inverted I/O enable does not affect Analog Comparator Output
- TWIE is not available
- CRC generator module is not available
- ADC 1/x gain setting and VCC/2 reference setting is not available
- TOSC alternate pin locations is not available
- TWI SDAHOLD time configuration is not available
- Timer/Counter 2 is not available
- HIRES+ option is not available
- Alternate pin locations for digital peripherals are not available
- XOSCPWR high drive option for external crystal is not available
- PLL divide by two option is not available
- Real Time Counter non-prescaled 32kHZ clock options are not available
- PLL lock detection failure function is not available
- Non available functions and options
- Temperature sensor not calibrated
- Disabling the USART transmitter does not automatically set the TxD pin direction to output.