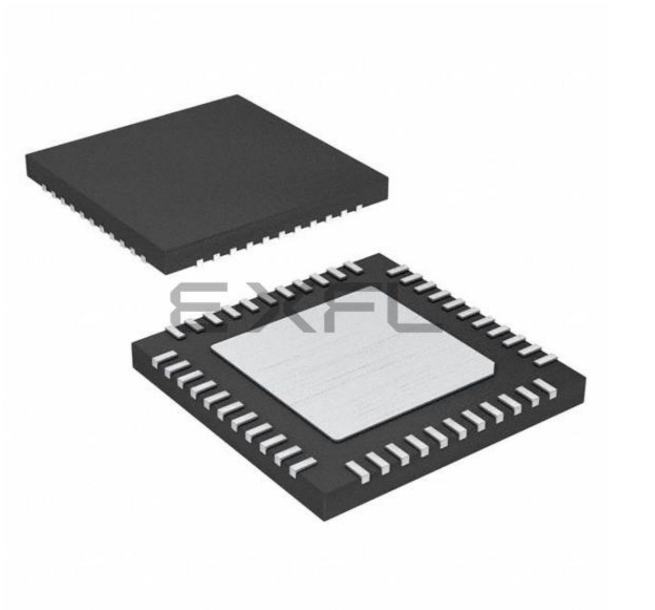

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What is "Embedded - Microcontrollers"?

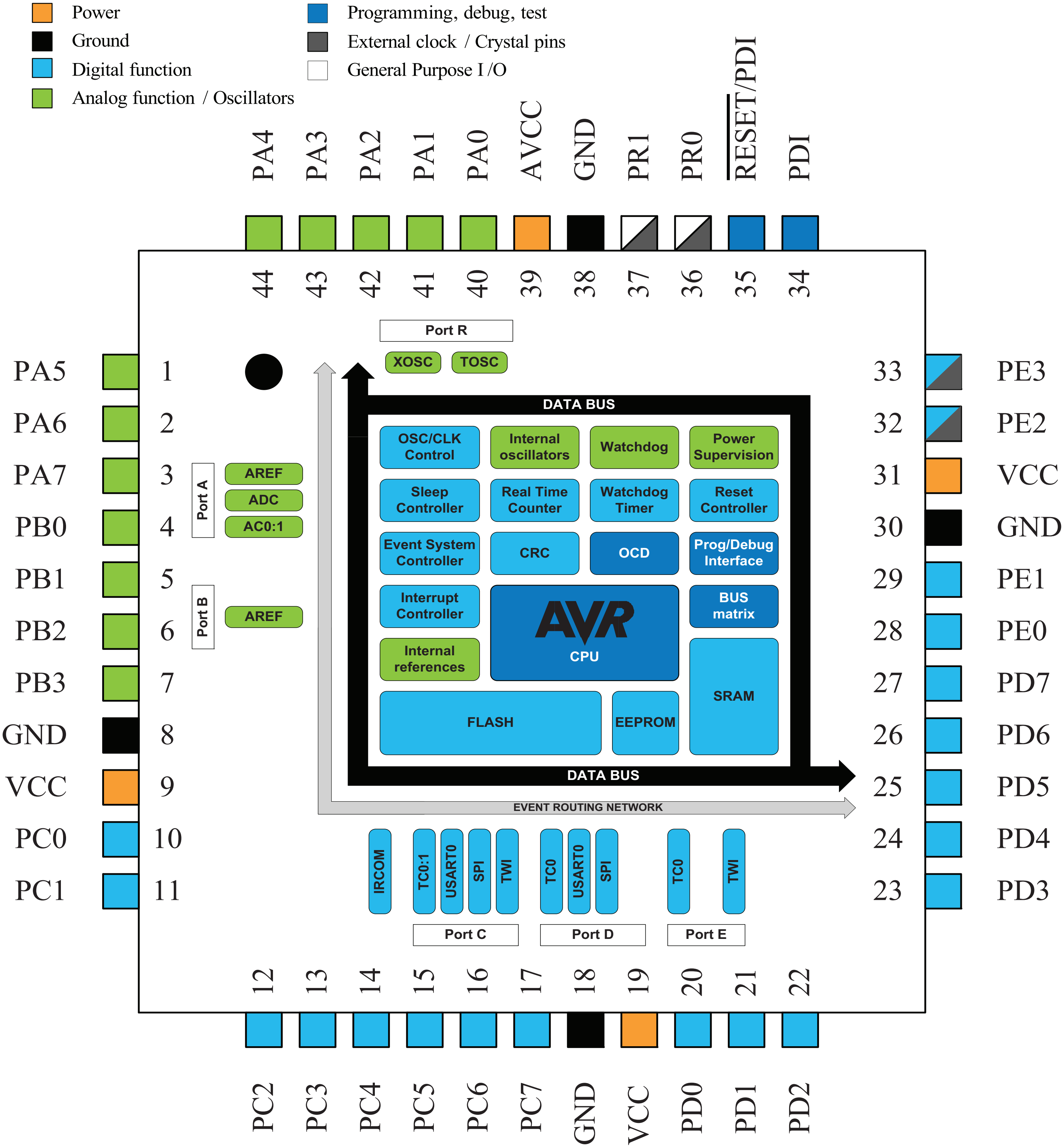
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	34
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFQFN Exposed Pad
Supplier Device Package	44-VQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega64d4-mhr

2. Pinout/Block diagram

Figure 2-1. Block Diagram and QFN/TQFP Pinout



Note: 1. For full details on pinout and pin functions refer to "Pinout and Pin Functions" on page 49.

24. CRC – Cyclic Redundancy Check Generator

24.1 Features

- Cyclic redundancy check (CRC) generation and checking for
  - Communication data
  - Program or data in flash memory
  - Data in SRAM and I/O memory space
- Integrated with flash memory and CPU
  - Automatic CRC of the complete or a selectable range of the flash memory
  - CPU can load data to the CRC generator through the I/O interface
- CRC polynomial software selectable to
  - CRC-16 (CRC-CCITT)
  - CRC-32 (IEEE 802.3)
- Zero remainder detection

24.2 Overview

A cyclic redundancy check (CRC) is an error detection technique test algorithm used to find accidental errors in data, and it is commonly used to determine the correctness of a data transmission, and data present in the data and program memories. A CRC takes a data stream or a block of data as input and generates a 16- or 32-bit output that can be appended to the data and used as a checksum. When the same data are later received or read, the device or application repeats the calculation. If the new CRC result does not match the one calculated earlier, the block contains a data error. The application will then detect this and may take a corrective action, such as requesting the data to be sent again or simply not using the incorrect data.

Typically, an n-bit CRC applied to a data block of arbitrary length will detect any single error burst not longer than n bits (any single alteration that spans no more than n bits of the data), and will detect the fraction $1-2^{-n}$ of all longer error bursts. The CRC module in Atmel AVR XMEGA devices supports two commonly used CRC polynomials; CRC-16 (CRC-CCITT) and CRC-32 (IEEE 802.3).

- **CRC-16:**

  Polynomial: $x^{16}+x^{12}+x^5+1$

  Hex value: 0x1021

- **CRC-32:**

  Polynomial: $x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^8+x^7+x^5+x^4+x^2+x+1$

  Hex value: 0x04C11DB7

26. AC – Analog Comparator

26.1 Features

- Two Analog Comparators (ACs)
- Selectable hysteresis
  - No
  - Small
  - Large
- Analog comparator output available on pin
- Flexible input selection
  - All pins on the port
  - Bandgap reference voltage
  - A 64-level programmable voltage scaler of the internal AV_{CC} voltage
- Interrupt and event generation on:
  - Rising edge
  - Falling edge
  - Toggle
- Window function interrupt and event generation on:
  - Signal above window
  - Signal inside window
  - Signal below window
- Constant current source with configurable output pin selection

26.2 Overview

The analog comparator (AC) compares the voltage levels on two inputs and gives a digital output based on this comparison. The analog comparator may be configured to generate interrupt requests and/or events upon several different combinations of input change.

The important property of the analog comparator's dynamic behavior is the hysteresis. It can be adjusted in order to achieve the optimal operation for each application.

The input selection includes analog port pins, several internal signals, and a 64-level programmable voltage scaler. The analog comparator output state can also be output on a pin for use by external devices.

A constant current source can be enabled and output on a selectable pin. This can be used to replace, for example, external resistors used to charge capacitors in capacitive touch sensing applications.

The analog comparators are always grouped in pairs on each port. These are called analog comparator 0 (AC0) and analog comparator 1 (AC1). They have identical behavior, but separate control registers. Used as pair, they can be set in window mode to compare a signal to a voltage range instead of a voltage level.

PORTA has one AC pair. Notation is ACA.

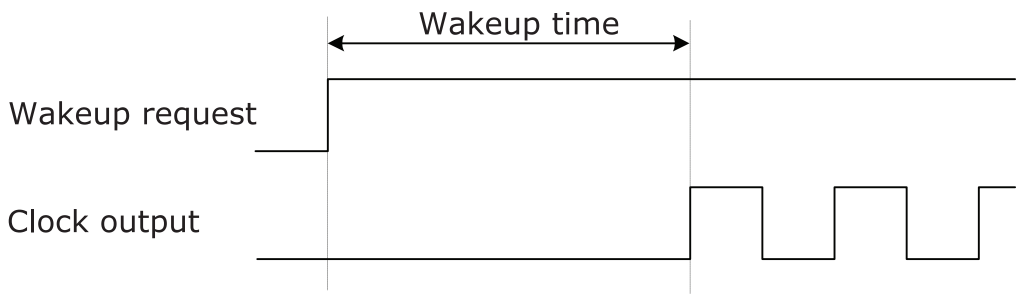
32.1.4 Wake-up Time from Sleep Modes

Table 32-6. Device Wake-up Time from Sleep Modes with Various System Clock Sources

Symbol	Parameter	Condition	Min.	Typ.[1]	Max.	Units
t_{wakeup}	Wake-up time from idle, standby, and extended standby mode	External 2MHz clock		2.0		µs
		32.768kHz internal oscillator		120		
		2MHz internal oscillator		2.0		
		32MHz internal oscillator		0.2		
	Wake-up time from power-save and power-down mode	External 2MHz clock		5.0		
		32.768kHz internal oscillator		320		
		2MHz internal oscillator		9.0		
		32MHz internal oscillator		5.0		

Note: 1. The wake-up time is the time from the wake-up request is given until the peripheral clock is available on pin, see Figure 32-2. All peripherals and modules start execution from the first clock cycle, expect the CPU that is halted for four clock cycles before program execution starts.

Figure 32-2. Wake-up Time Definition



32.2 ATxmega32D4

32.2.1 Absolute Maximum Ratings

Stresses beyond those listed in Table 32-29 under may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 32-29. Absolute Maximum Ratings

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		-0.3		4	V
I_{VCC}	Current into a V_{CC} pin				200	mA
I_{GND}	Current out of a Gnd pin				200	
V_{PIN}	Pin voltage with respect to Gnd and V_{CC}		-0.5		V_{CC}+0.5	V
I_{PIN}	I/O pin sink/source current		-25		25	mA
T_A	Storage temperature		-65		150	°C
T_j	Junction temperature				150	

32.2.2 General Operating Ratings

The device must operate within the ratings listed in Table 32-30 in order for all other electrical characteristics and typical characteristics of the device to be valid.

Table 32-30. General Operating Conditions

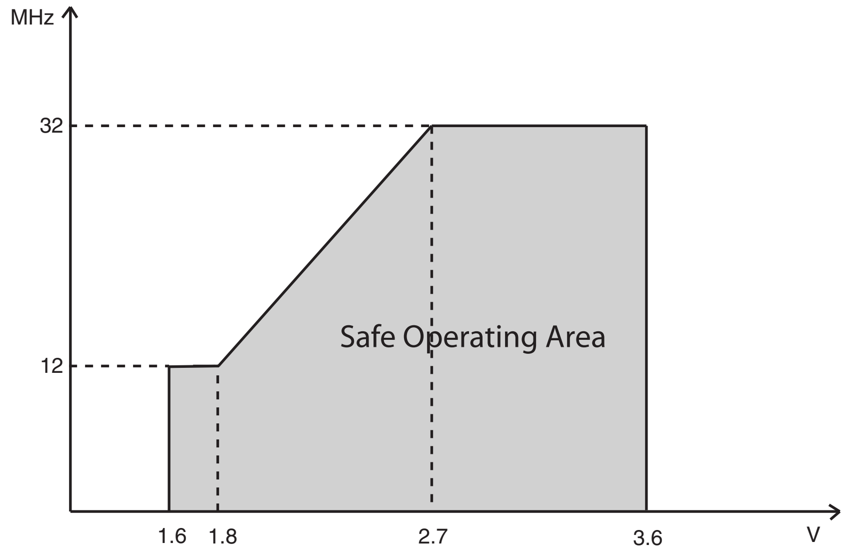
Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		1.60		3.6	V
AV_{CC}	Analog supply voltage		1.60		3.6	
T_A	Temperature range		-40		85	°C
T_j	Junction temperature		-40		105	

Table 32-31. Operating Voltage and Frequency

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{CPU}	CPU clock frequency	V_{CC} = 1.6V	0		12	MHz
		V_{CC} = 1.8V	0		12	
		V_{CC} = 2.7V	0		32	
		V_{CC} = 3.6V	0		32	

The maximum CPU clock frequency depends on V_{CC}. As shown in Figure 32-8 the Frequency vs. V_{CC} curve is linear between 1.8V < V_{CC} < 2.7V.

Figure 32-8. Maximum Frequency vs. V_{CC}



32.4.10 External Reset Characteristics

Table 32-100.External Reset Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{EXT}	Minimum reset pulse width		1000	95		ns
V_{RST}	Reset threshold voltage (V_{IH})	V_{CC} = 2.7 - 3.6V	0.60*V_{CC}			V
		V_{CC} = 1.6 - 2.7V	0.60*V_{CC}		0.50*V_{CC}	
	Reset threshold voltage (V_{IL})	V_{CC} = 2.7 - 3.6V			0.40*V_{CC}	
		V_{CC} = 1.6 - 2.7V			0.50*V_{CC}	
R_{RST}	Reset pin pull-up resistor			25		kΩ

32.4.11 Power-on Reset Characteristics

Table 32-101.Power-on Reset Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{POT-} (1)	POR threshold voltage falling V_{CC}	V_{CC} falls faster than 1V/ms	0.4	1.0		V
		V_{CC} falls at 1V/ms or slower	0.8	1.0		
V_{POT+}	POR threshold voltage rising V_{CC}			1.3	1.59	

Note: 1. V_{POT-} values are only valid when BOD is disabled. When BOD is enabled V_{POT-} = V_{POT+}.

32.4.12 Flash and EEPROM Memory Characteristics

Table 32-102.Endurance and Data Retention

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Flash	Write/Erase cycles	25°C	10K			Cycle
			85°C	10K			
			105°C	2K			
		Data retention	25°C	100			Year
			85°C	25			
			105°C	10			
	EEPROM	Write/Erase cycles	25°C	100K			Cycle
			85°C	100K			
			105°C	30K			
		Data retention	25°C	100			Year
			85°C	25			
			105°C	10			

Figure 33-9. Idle Mode Supply Current vs. Frequency

f_{SYS} = 1 - 32MHz external clock, T = 25°C

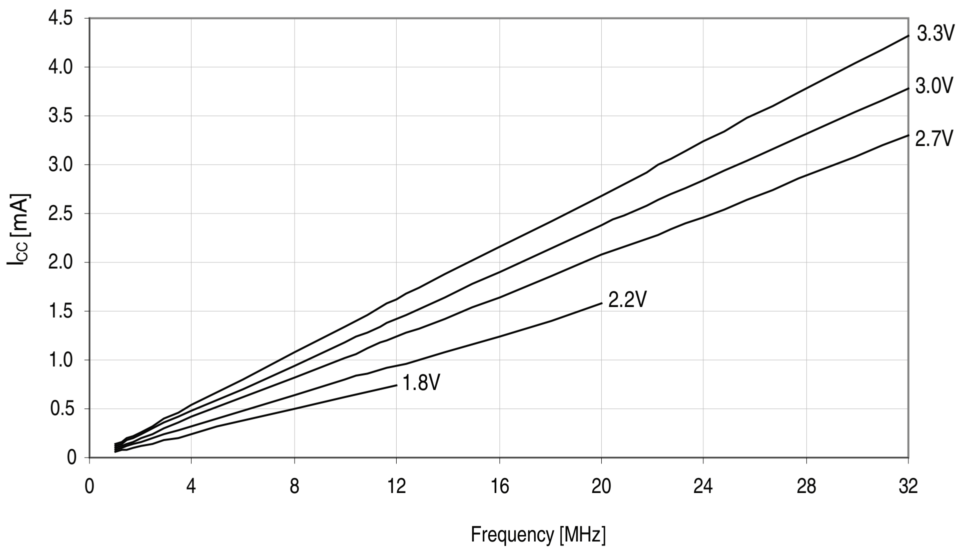


Figure 33-10. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 32.768kHz internal oscillator

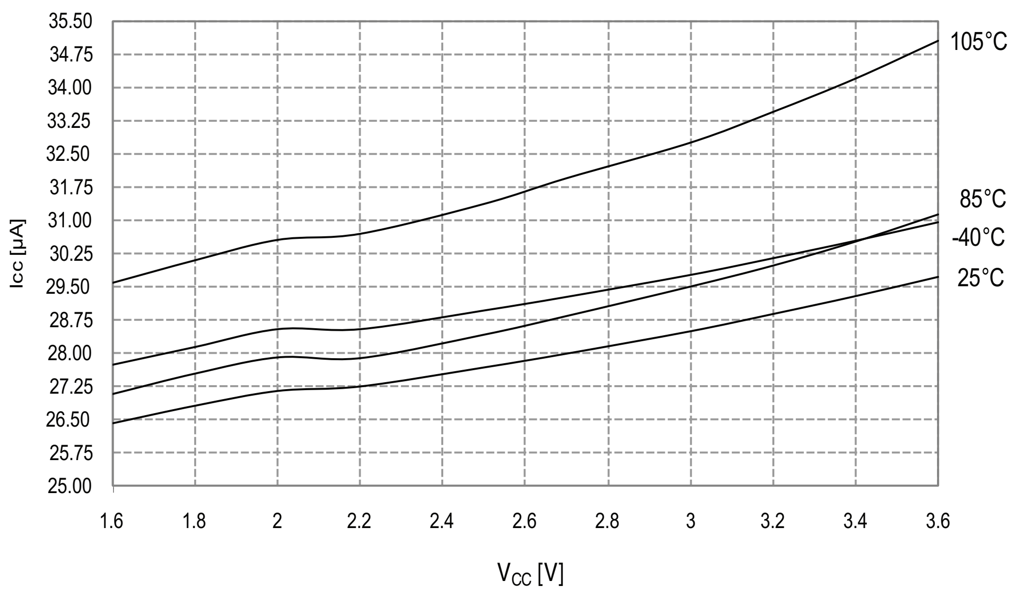


Figure 33-39. DNL Error vs. External V_{REF}

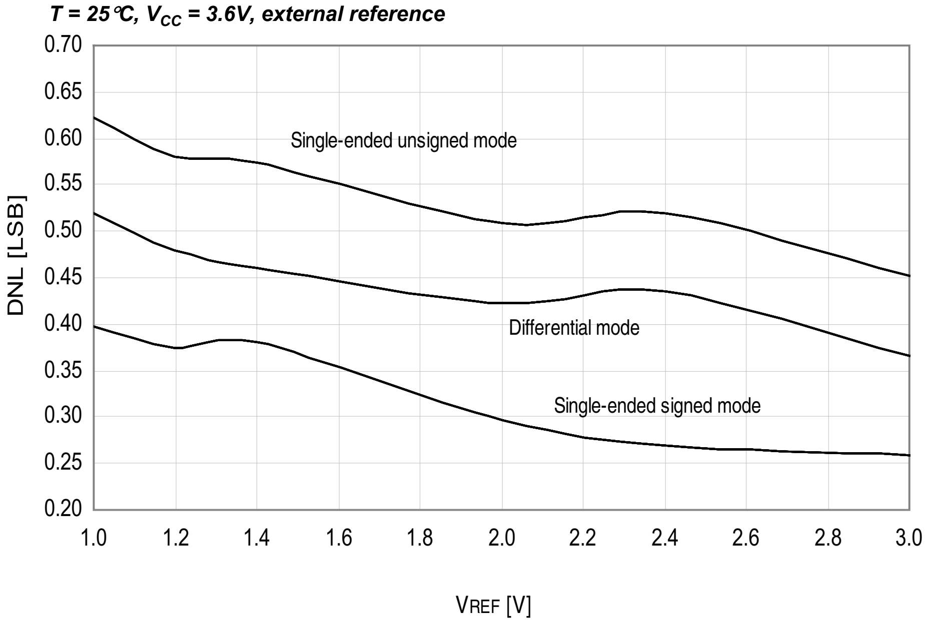


Figure 33-40. DNL Error vs. Sample Rate

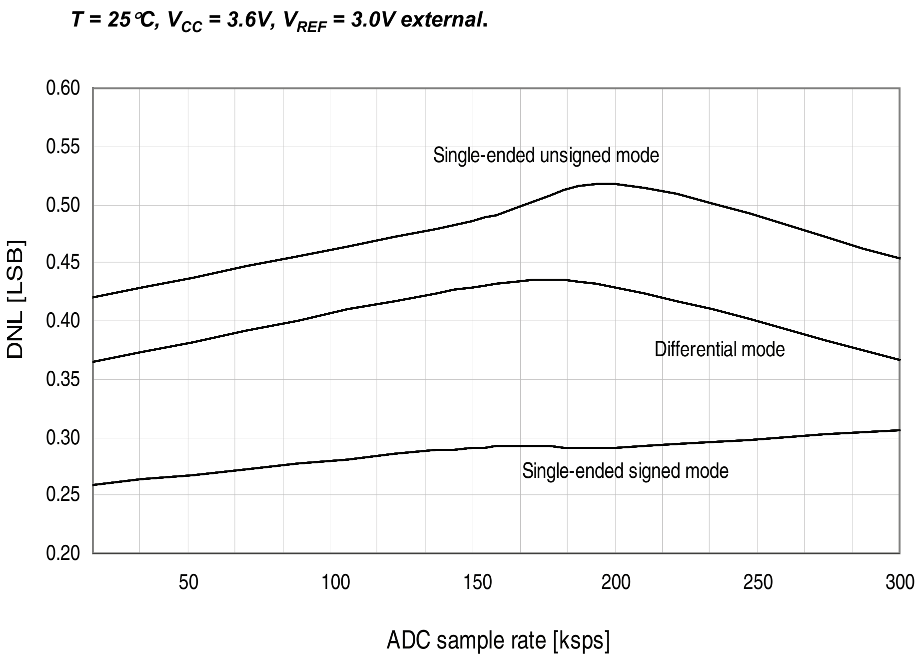


Figure 33-43. Gain Error vs. V_{CC}

T = 25°C, V_{REF} = external 1.0V, ADC sample rate = 200ksps

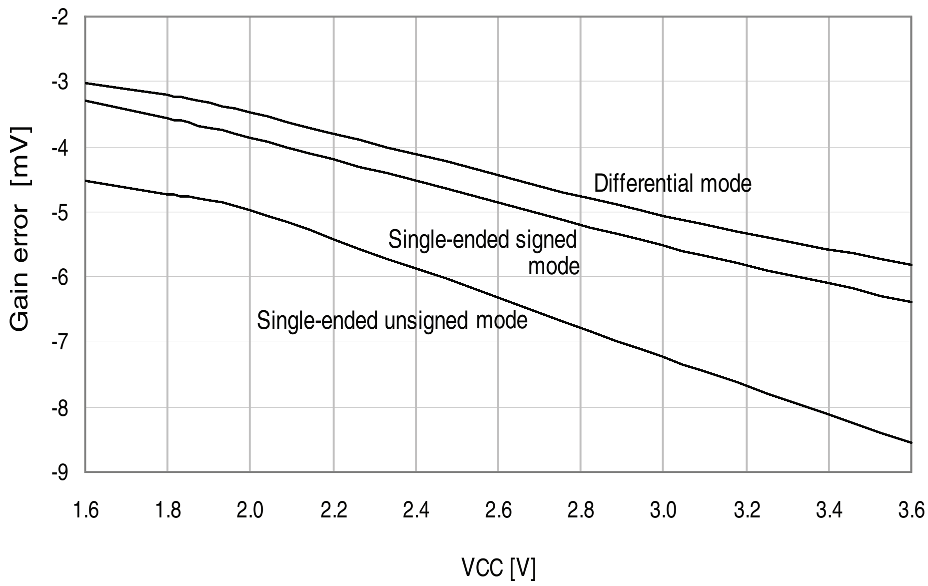


Figure 33-44. Offset Error vs. V_{REF}

T = 25°C, V_{CC} = 3.6V, ADC sample rate = 200ksps

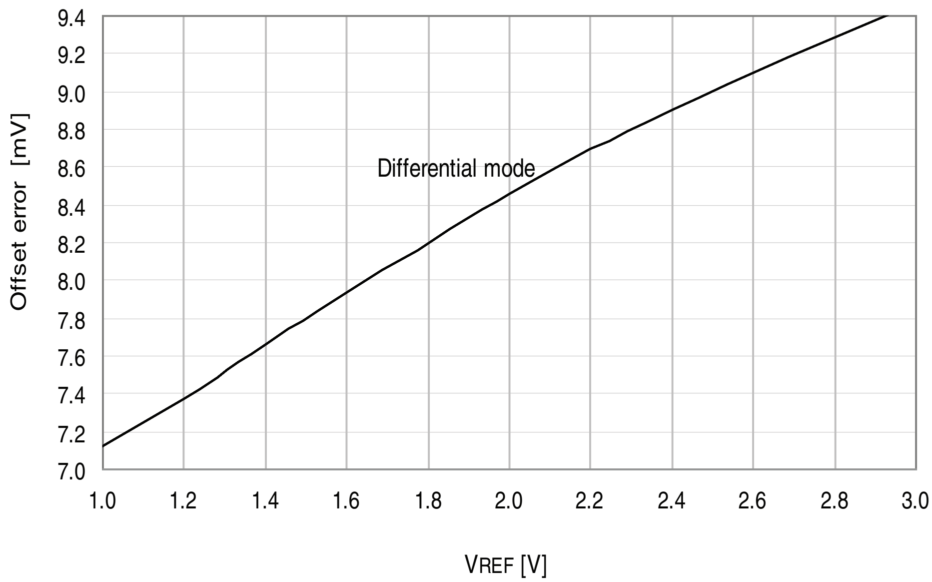
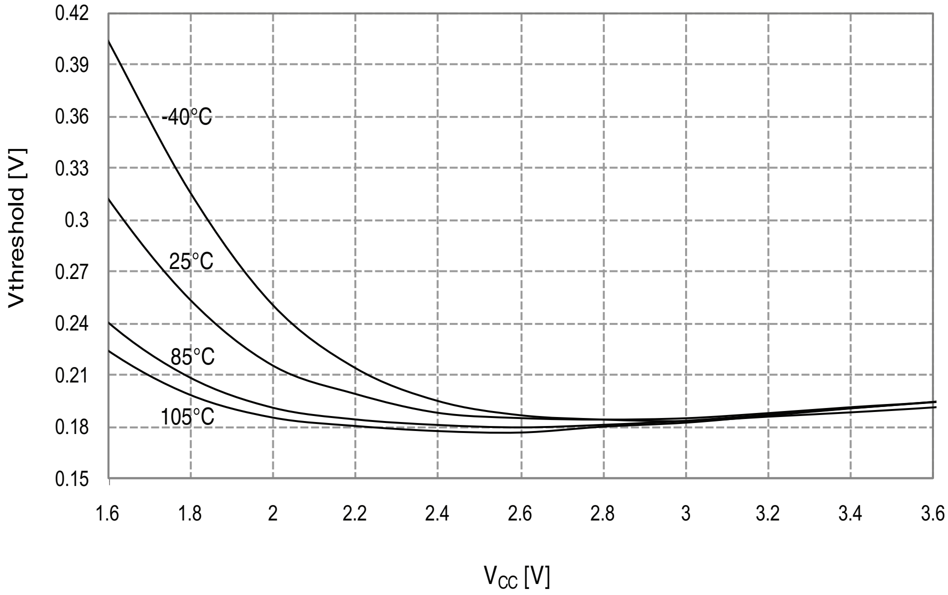


Figure 33-114. I/O Pin Input Hysteresis vs. V_{CC}



33.2.3 ADC Characteristics

Figure 33-115. INL Error vs. External V_{REF}

T = 25°C, V_{CC} = 3.6V, external reference

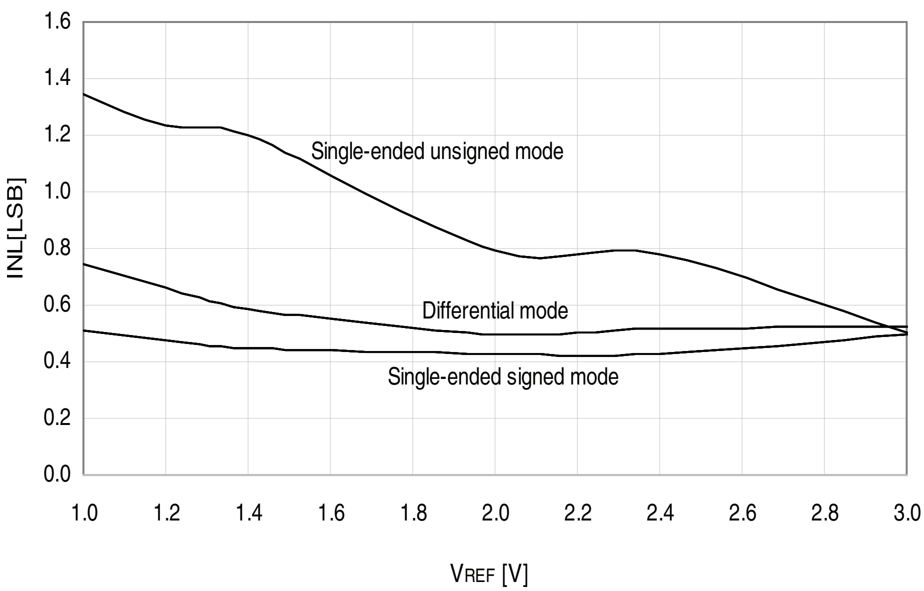


Figure 33-120. DNL Error vs. Input code

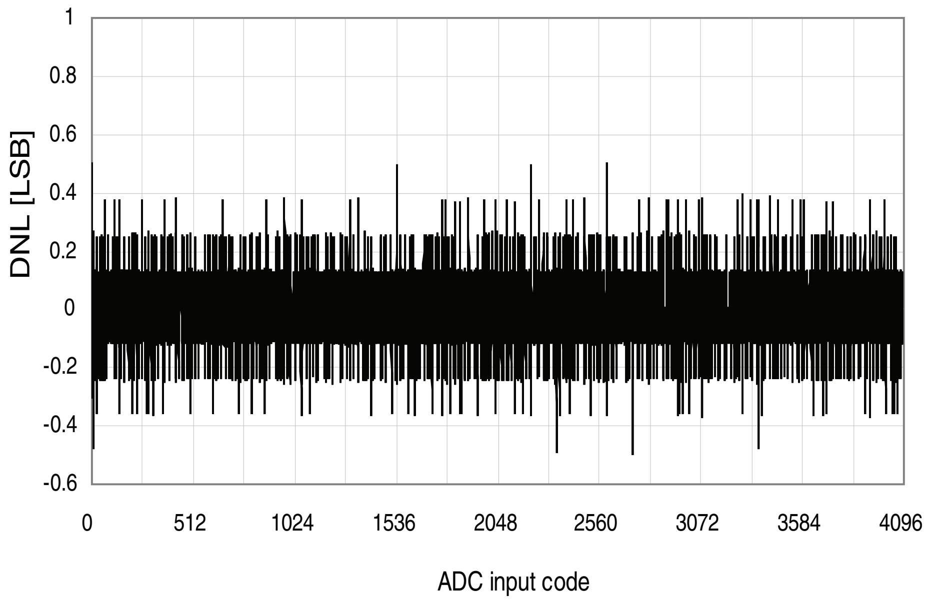


Figure 33-121. Gain Error vs. V_{REF}

T = 25°C, V_{CC} = 3.6V, ADC sample rate = 200ksps

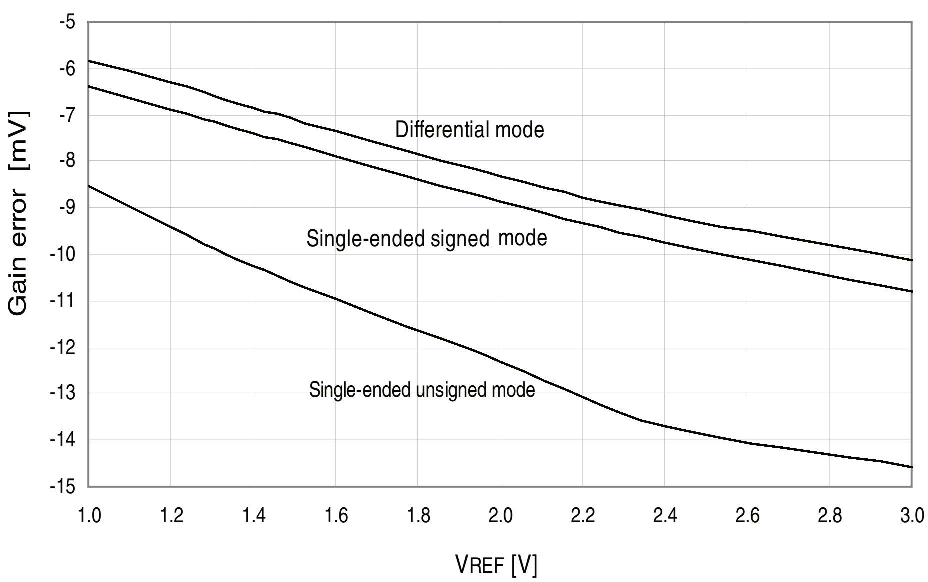


Figure 33-128. Analog Comparator Hysteresis vs. V_{CC}

Low power, small hysteresis

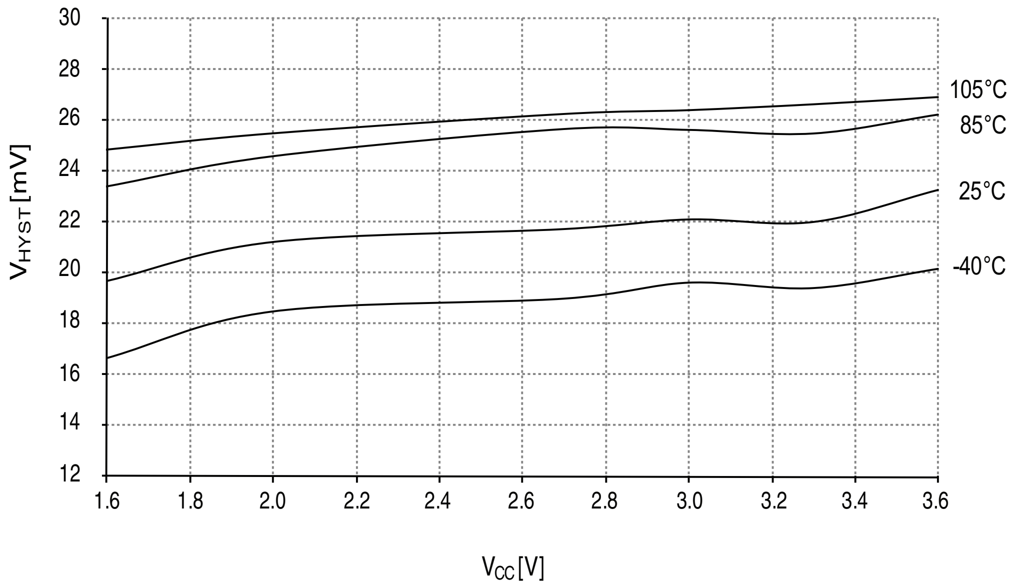


Figure 33-129. Analog Comparator Hysteresis vs. V_{CC}

Low power, large hysteresis

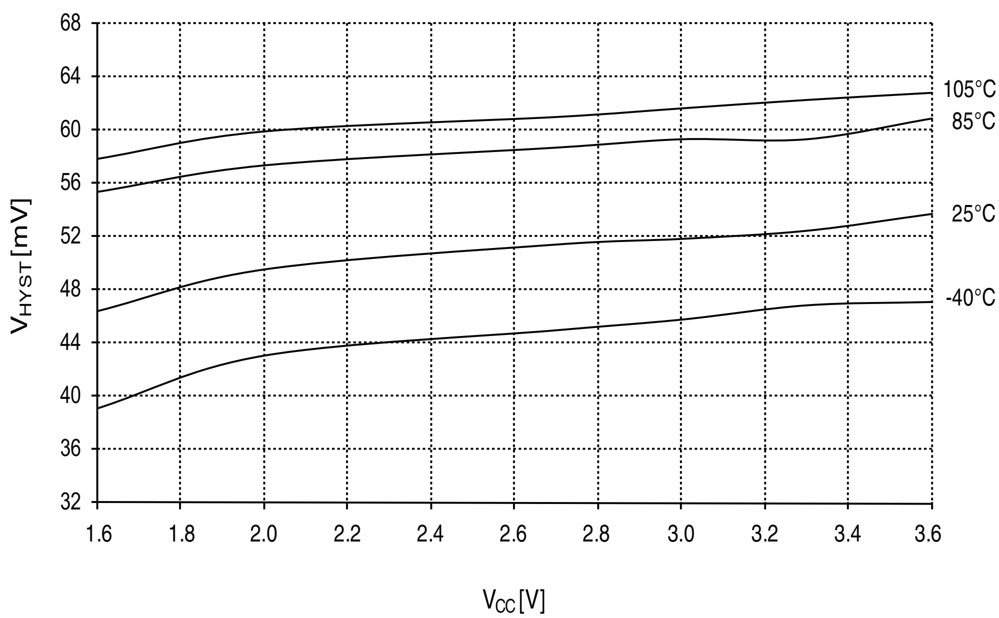


Figure 33-169. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 1MHz external clock

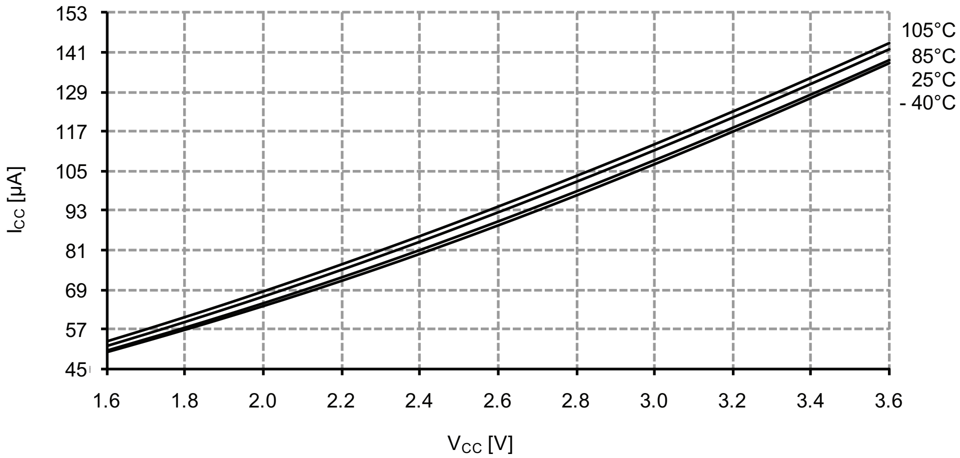


Figure 33-170. Idle Mode Supply Current vs. V_{CC}

f_{SYS} = 2MHz internal oscillator

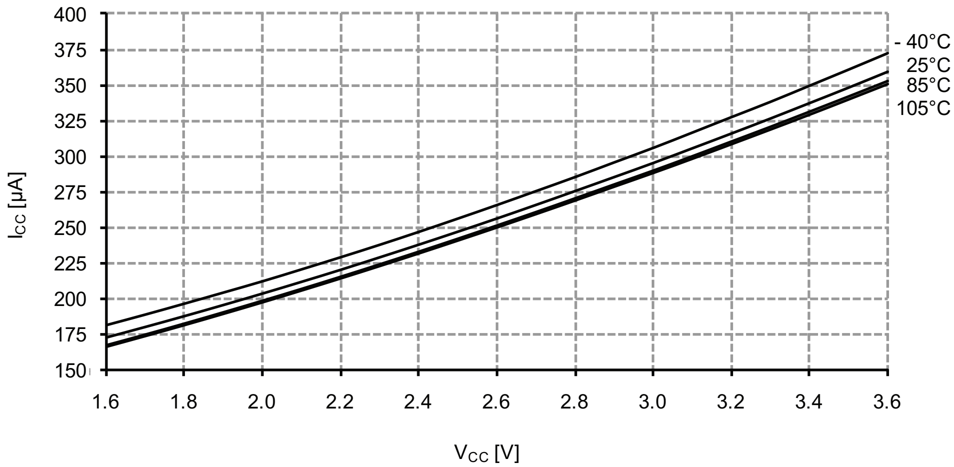


Figure 33-203. Gain Error vs. Temperature

V_{CC} = 2.7V, V_{REF} = external 1.0V

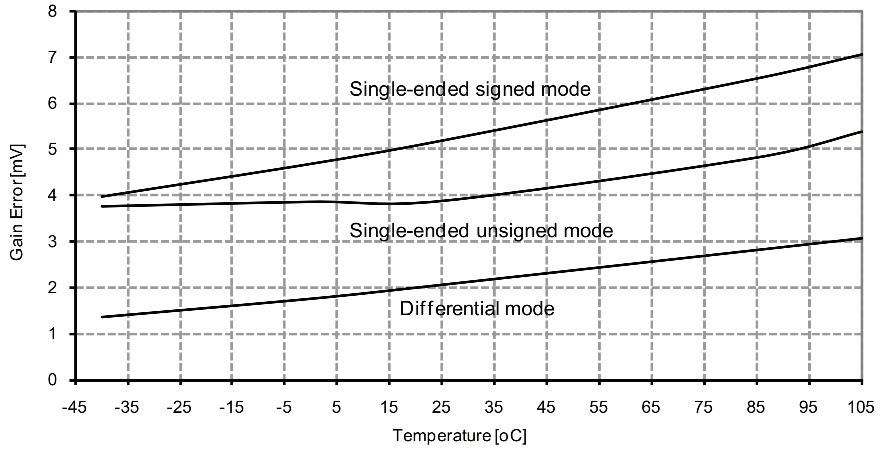


Figure 33-204. Offset Error vs. V_{CC}

T = 25°C, V_{REF} = external 1.0V, ADC sampling speed = 500ksps

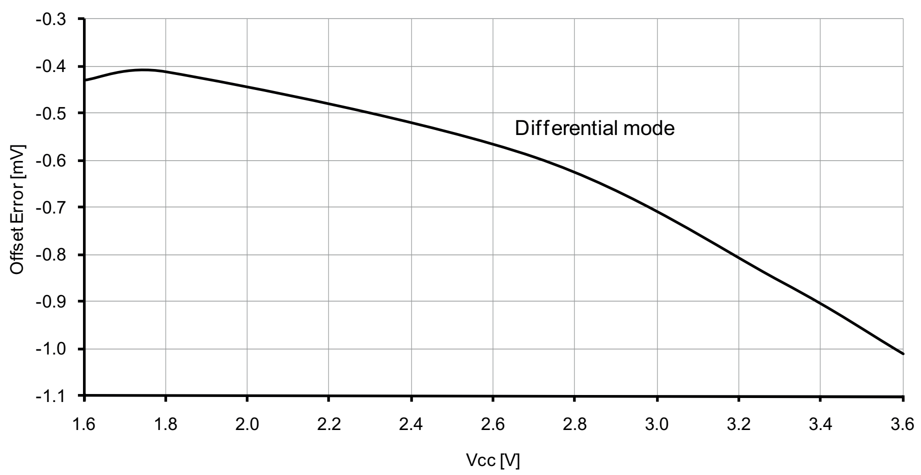
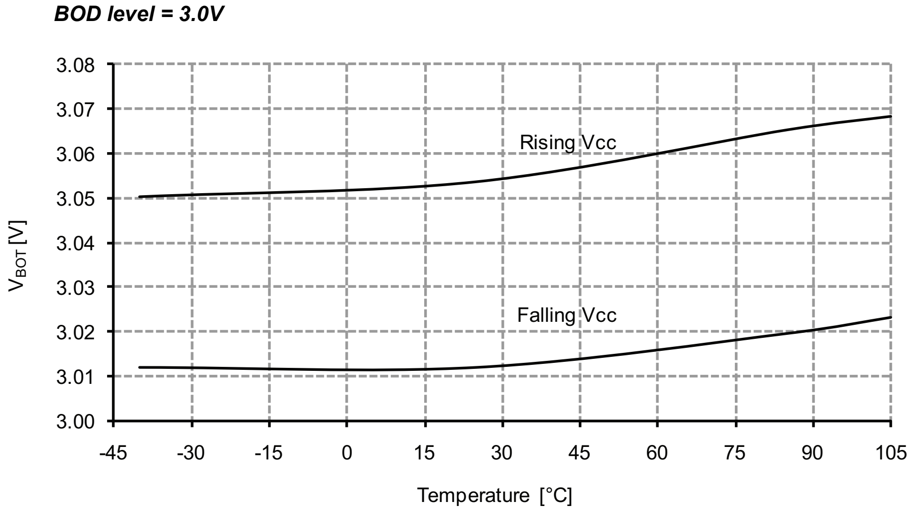
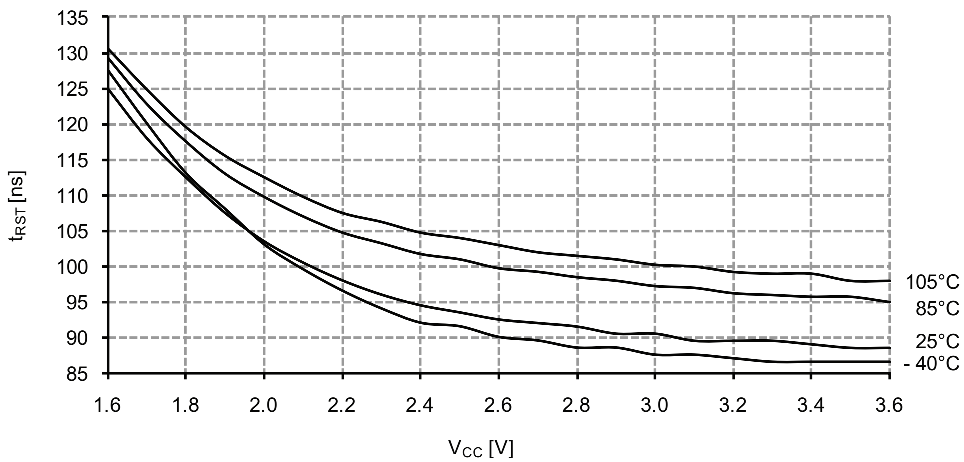


Figure 33-219. BOD Thresholds vs. Temperature



33.3.8 External Reset Characteristics

Figure 33-220. Minimum Reset Pin Pulse Width vs. V_{CC}



35. Datasheet Revision History

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

35.1 8135S – 09/2016

1.	Updated "Instruction Set Summary" on page 56. Removed "DES" instruction.
2.	Updated "Gain Stage Characteristics" : Table 32-11 on page 72, Table 32-39 on page 91Table 32-67 on page 110 and Table 32-96 on page 131. "Offset Error, input referred" is changed to "Offset Error, output referred.

35.2 8135R – 02/2015

1.	Updated Figure 25-1 on page 45
2.	Updated the "Packaging information" on page 61. Replaced "44M1" on page 62 by a correct package.
3.	Updated tables Table 32-8 on page 70and Table 32-36 on page 89 with information on fixed voltage offset.
4.	Updated use of capitals in heading, table headings and figure titles.

35.3 8135Q – 09/2014

1.	Updated the "Ordering Information" on page 2. Added ordering information for ATxmega16D4/32D4/64D4/128D4 @ 105°C.
2.	Updated the Application table section from 4K/4K/4K/4K to 8K/4K/4K/4K in the Figure 7-1 on page 13
3.	Updated Table 32-4 on page 66, Table 32-33 on page 86, Table 32-60 on page 104 and Table 32-89 on page 125. Added Icc Power-down power consumption for T=105°C for all functions disabled and for WDT and sampled BOD enabled
4.	Updated Table 32-17 on page 74, Table 32-45 on page 93, Table 32-73 on page 112 and Table 32-102 on page 133. Updated all tables to include values for T=85°C and T=105°C. Removed T=55°C
5.	Changed Vcc to AVcc in Figure 25-1 on page 45 and in the text in Section 25. "ADC – 12-bit Analog to Digital Converter" on page 44 and in Section 26. "AC – Analog Comparator" on page 46
6.	Changed unit parameter for $t_{SU;DAT}$ to ns in Table 32-28 on page 82, Table 32-56 on page 101, Table 32-85 on page 121 and Table 32-114 on page 142.
7.	Added ERRATA information on disabling of USART transmitter to Section 34.1 "ATxmega16D4 / ATxmega32D4" on page 308.
8.	Updated the typical characteristics of "ATxmega64D4" and "ATxmega128D4" with characterizations @105°C

35.4 8135P – 01/2014

1.	Updated the typical characteristics of "ATxmega16D4" and "ATxmega32D4" with characterizations @ 105°C

35.15 8135E – 02/10

1.	Updated the device pin-out Figure 2-1 on page 3. PDI_CLK and PDI_DATA renamed only PDI.
2.	Updated Table 7-3 on page 18. No of Pages for ATxmega32D4: 32
3.	Updated ”Alternate Port Functions” on page 29.
4.	Updated ”ADC - 12-bit Analog to Digital Converter” on page 39.
5.	Updated Figure 25-1 on page 50.
6.	Updated ”Alternate Pin Functions” on page 48.
7.	Updated ”Timer/Counter and AWEX functions” on page 46.
8.	Added Table 31-17 on page 65.
9.	Added Table 31-18 on page 66.
10.	Changed Internal Oscillator Speed to ”Oscillators and Wake-up Time” on page 85.
11.	Updated ”Errata” on page 90.

35.16 8135D – 12/09

1.	Added ATxmega128D4 device and updated the datasheet accordingly.
2.	Updated ”Electrical Characteristics” on page 58 with Max/Min numbers.
3.	Added ”Flash and EEPROM Memory Characteristics” on page 61.
4.	Updated Table 31-10 on page 64, Input hysteresis is in V and not in mV.
5.	Added ”Errata” on page 90.

35.17 8135C – 10/09

1.	Updated ”Features” on page 1 with Two Two-Wire Interfaces.
2.	Updated ”Block Diagram and QFN/TQFP pinout” on page 3.
3.	Updated ”Overview” on page 5.
4.	Updated ”XMEGA D4 Block Diagram” on page 7.
5.	Updated Table 13-1 on page 24.
6.	Updated ”Overview” on page 35.
7.	Updated Table 27-5 on page 49.
8.	Updated ”Peripheral Module Address Map” on page 50.

35.18 8135B – 09/09

1.	Added ”Electrical Characteristics” on page 58.
2.	Added ”Typical Characteristics” on page 67.

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