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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	60MHz
Connectivity	EBI/EMI, I ² C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	112
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 1.95V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2212fbd144-551

3.1 Ordering options

Table 2. Ordering options

Type number	Flash memory	RAM	Fast GPIO/ SSP/ Enhanced UART, ADC, Timer	Temperature range
LPC2212FBD144/01	128 kB	16 kB	yes	–40 °C to +85 °C
LPC2214FBD144/01	256 kB	16 kB	yes	–40 °C to +85 °C

4. Block diagram

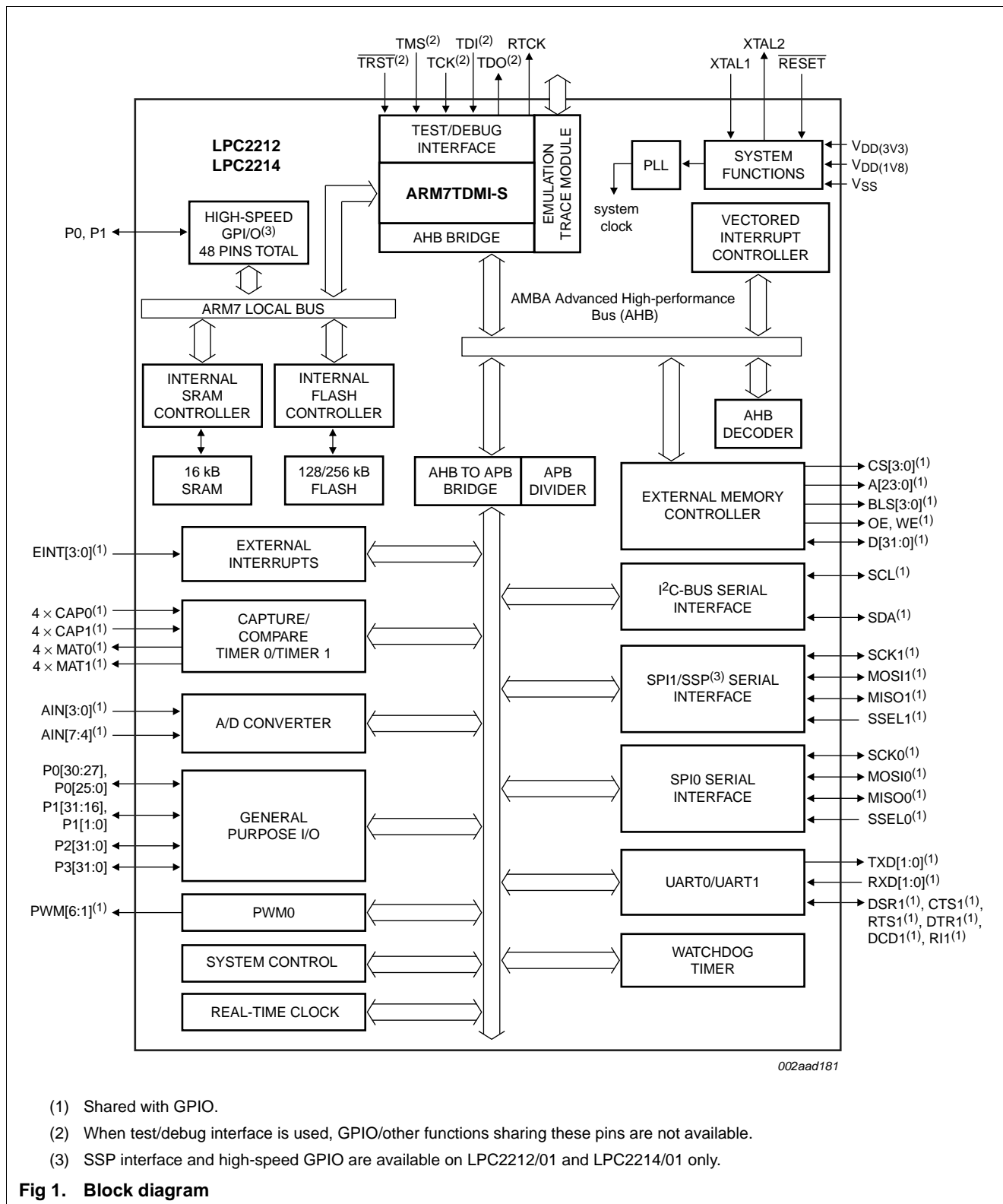


Fig 1. Block diagram

5.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
P0[0] to P0[31]		I/O	Port 0 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 0 pins depends upon the pin function selected via the Pin Connect Block. Pins 26 and 31 of port 0 are not available.
P0[0]/TXD0/PWM1	42	O	TXD0 — Transmitter output for UART0.
		O	PWM1 — Pulse Width Modulator output 1.
P0[1]/RXD0/PWM3/EINT0	49	I	RXD0 — Receiver input for UART0.
		O	PWM3 — Pulse Width Modulator output 3.
		I	EINT0 — External interrupt 0 input
P0[2]/SCL/CAP0[0]	50	I/O	SCL — I ² C-bus clock input/output. Open-drain output (for I ² C-bus compliance).
		I	CAP0[0] — Capture input for Timer 0, channel 0.
P0[3]/SDA/MAT0[0]/EINT1	58	I/O	SDA — I ² C-bus data input/output. Open-drain output (for I ² C-bus compliance).
		O	MAT0[0] — Match output for Timer 0, channel 0.
		I	EINT1 — External interrupt 1 input.
P0[4]/SCK0/CAP0[1]	59	I/O	SCK0 — Serial clock for SPI0. SPI clock output from master or input to slave.
		I	CAP0[1] — Capture input for Timer 0, channel 1.
P0[5]/MISO0/MAT0[1]	61	I/O	MISO0 — Master In Slave OUT for SPI0. Data input to SPI master or data output from SPI slave.
		O	MAT0[1] — Match output for Timer 0, channel 1.
P0[6]/MOSI0/CAP0[2]	68	I/O	MOSI0 — Master Out Slave In for SPI0. Data output from SPI master or data input to SPI slave.
		I	CAP0[2] — Capture input for Timer 0, channel 2.
		I	SSEL0 — Slave Select for SPI0. Selects the SPI interface as a slave.
P0[7]/SSEL0/PWM2/EINT2	69	O	PWM2 — Pulse Width Modulator output 2.
		I	EINT2 — External interrupt 2 input.
		I	SSEL0 — Slave Select for SPI0. Selects the SPI interface as a slave.
P0[8]/TXD1/PWM4	75	O	TXD1 — Transmitter output for UART1.
		O	PWM4 — Pulse Width Modulator output 4.
		I	RXD1 — Receiver input for UART1.
P0[9]/RXD1/PWM6/EINT3	76	O	PWM6 — Pulse Width Modulator output 6.
		I	EINT3 — External interrupt 3 input.
		I	RXD1 — Receiver input for UART1.
P0[10]/RTS1/CAP1[0]	78	O	RTS1 — Request to Send output for UART1.
		I	CAP1[0] — Capture input for Timer 1, channel 0.
P0[11]/CTS1/CAP1[1]	83	I	CTS1 — Clear to Send input for UART1.
		I	CAP1[1] — Capture input for Timer 1, channel 1.
P0[12]/DSR1/MAT1[0]	84	I	DSR1 — Data Set Ready input for UART1.
		O	MAT1[0] — Match output for Timer 1, channel 0.
P0[13]/DTR1/MAT1[1]	85	O	DTR1 — Data Terminal Ready output for UART1.
		O	MAT1[1] — Match output for Timer 1, channel 1.

Table 3. Pin description ...continued

Symbol	Pin	Type	Description
P0[30]/AIN3/EINT3/ CAP0[0]	33	I	AIN3 — ADC, input 3. This analog input is always connected to its pin.
		I	EINT3 — External interrupt 3 input.
		I	CAP0[0] — Capture input for Timer 0, channel 0.
P1[0] to P1[31]		I/O	Port 1 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 1 pins depends upon the pin function selected via the Pin Connect Block. Pins 2 through 15 of port 1 are not available.
P1[0]/CS0	91	O	LOW-active Chip Select 0 signal. (Bank 0 addresses range 0x8000 0000 to 0x80FF FFFF)
P1[1]/OE	90	O	LOW-active Output Enable signal.
P1[16]/TRACEPKT0	34	O	Trace Packet, bit 0. Standard I/O port with internal pull-up.
P1[17]/TRACEPKT1	24	O	Trace Packet, bit 1. Standard I/O port with internal pull-up.
P1[18]/TRACEPKT2	15	O	Trace Packet, bit 2. Standard I/O port with internal pull-up.
P1[19]/TRACEPKT3	7	O	Trace Packet, bit 3. Standard I/O port with internal pull-up.
P1[20]/TRACESYNC	102	O	Trace Synchronization; standard I/O port with internal pull-up. Note: LOW on this pin while $\overline{\text{RESET}}$ is LOW, enables pins P1[25:16] to operate as Trace port after reset.
P1[21]/PIPESTAT0	95	O	Pipeline Status, bit 0. Standard I/O port with internal pull-up.
P1[22]/PIPESTAT1	86	O	Pipeline Status, bit 1. Standard I/O port with internal pull-up.
P1[23]/PIPESTAT2	82	O	Pipeline Status, bit 2. Standard I/O port with internal pull-up.
P1[24]/TRACECLK	70	O	Trace Clock. Standard I/O port with internal pull-up.
P1[25]/EXTIN0	60	I	External Trigger Input. Standard I/O with internal pull-up.
P1[26]/RTCK	52	I/O	Returned Test Clock output. Extra signal added to the JTAG port. Assists debugger synchronization when processor frequency varies. Bidirectional pin with internal pull-up. Note: LOW on this pin while $\overline{\text{RESET}}$ is LOW, enables pins P1[31:26] to operate as Debug port after reset.
P1[27]/TDO	144	O	Test Data out for JTAG interface.
P1[28]/TDI	140	I	Test Data in for JTAG interface.
P1[29]/TCK	126	I	Test Clock for JTAG interface. This clock must be slower than $\frac{1}{6}$ of the CPU clock (CCLK) for the JTAG interface to operate.
P1[30]/TMS	113	I	Test Mode Select for JTAG interface.
P1[31]/ $\overline{\text{TRST}}$	43	I	Test Reset for JTAG interface.
P2[0] to P2[31]		I/O	Port 2 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 2 pins depends upon the pin function selected via the Pin Connect Block.
P2[0]/D0	98	I/O	External memory data line 0.
P2[1]/D1	105	I/O	External memory data line 1.
P2[2]/D2	106	I/O	External memory data line 2.
P2[3]/D3	108	I/O	External memory data line 3.
P2[4]/D4	109	I/O	External memory data line 4.
P2[5]/D5	114	I/O	External memory data line 5.
P2[6]/D6	115	I/O	External memory data line 6.

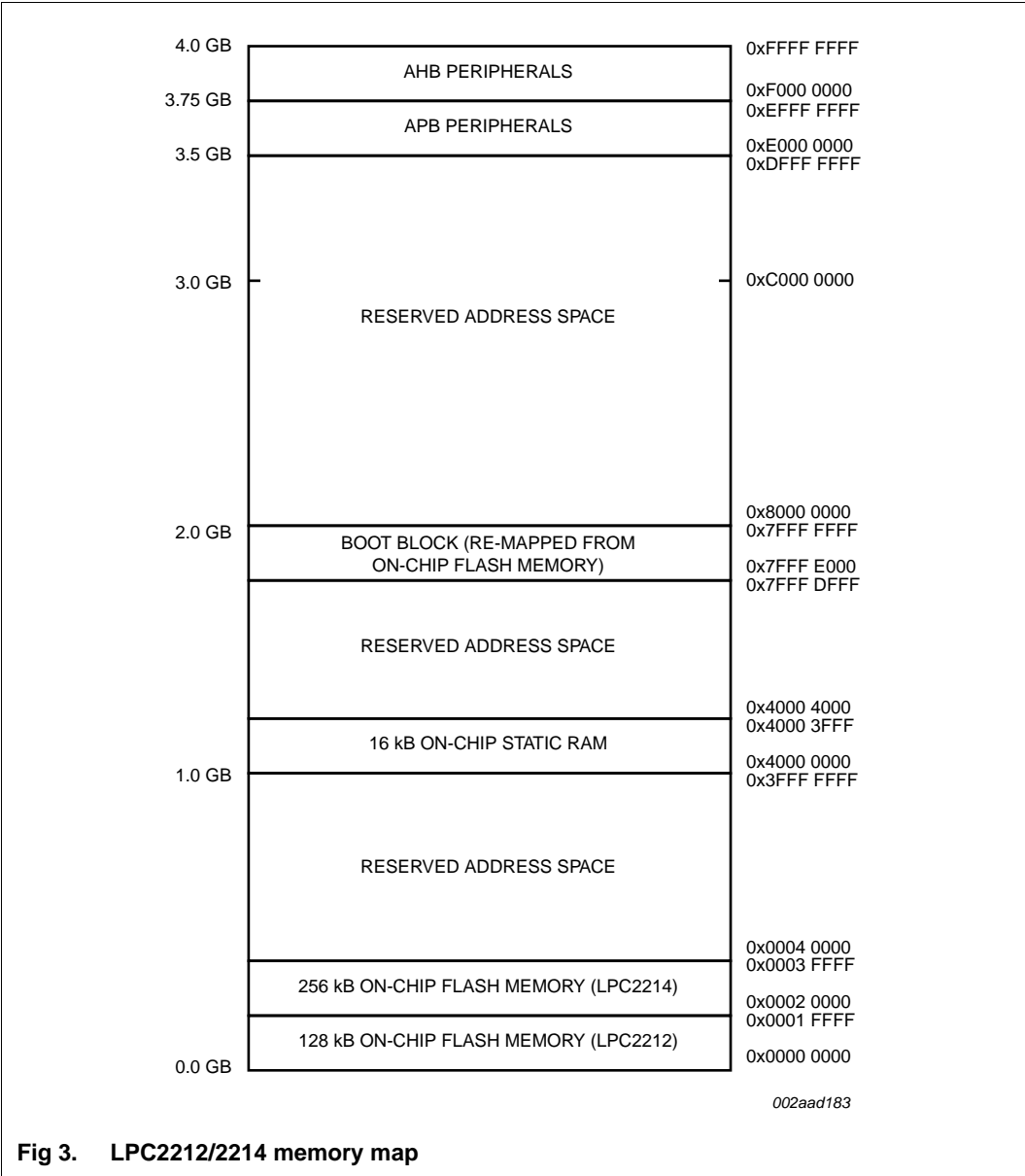


Fig 3. LPC2212/2214 memory map

6.5 Interrupt controller

The Vectored Interrupt Controller (VIC) accepts all of the interrupt request inputs and categorizes them as Fast Interrupt reQuest (FIQ), vectored Interrupt ReQuest (IRQ), and non-vectored IRQ as defined by programmable settings. The programmable assignment scheme means that priorities of interrupts from the various peripherals can be dynamically assigned and adjusted.

The FIQ has the highest priority. If more than one request is assigned to FIQ, the VIC combines the requests to produce the FIQ signal to the ARM processor. The fastest possible FIQ latency is achieved when only one request is classified as FIQ, because then the FIQ service routine can simply start dealing with that device. But if more than one request is assigned to the FIQ class, the FIQ service routine can read a word from the VIC that identifies which FIQ source(s) is (are) requesting an interrupt.

[1] SSP interface available on LPC2212/01 and LPC2214/01 only.

6.6 Pin connect block

The pin connect block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on chip peripherals. Peripherals should be connected to the appropriate pins prior to being activated, and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

6.7 External memory controller

The external Static Memory Controller (SMC) is a module which provides an interface between the system bus and external (off-chip) memory devices. It provides support for up to four independently configurable memory banks (16 MB each with byte lane enable control) simultaneously. Each memory bank is capable of supporting SRAM, ROM, flash EPROM, burst ROM memory, or some external I/O devices.

Each memory bank may be 8-bit, 16-bit, or 32-bit wide.

6.8 General purpose parallel I/O (GPIO) and Fast I/O

Device pins that are not connected to a specific peripheral function are controlled by the parallel I/O registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back, as well as the current state of the port pins.

6.8.1 Features

- Bit-level set and clear registers allow a single instruction set or clear of any number of bits in one port.
- Direction control of individual bits.
- Separate control of output set and clear.
- All I/O default to inputs after reset.

6.8.2 Features added with the Fast GPIO set of registers available on LPC2212/2214/01 only

- Fast GPIO registers are relocated to the ARM local bus for the fastest possible I/O timing, enabling port pin toggling up to 3.5 times faster than earlier LPC2000 devices.
- Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
- All Fast GPIO registers are byte addressable.
- Entire port value can be written in one instruction.
- Ports are accessible via either the legacy group of registers (GPIOs) or the group of registers providing accelerated port access (Fast GPIOs).

6.9 10-bit ADC

The LPC2212/2214 each contain a single 10-bit successive approximation ADC with four multiplexed channels.

6.9.1 Features

- Measurement range of 0 V to 3 V.
- Capable of performing more than 400 000 10-bit samples per second.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition on input pin or Timer Match signal.

6.9.2 ADC features available in LPC2212/2214/01 only

- Every analog input has a dedicated result register to reduce interrupt overhead.
- Every analog input can generate an interrupt once the conversion is completed.
- The ADC pads are 5 V tolerant when configured for digital I/O function(s).

6.10 UARTs

The LPC2212/2214 each contain two UARTs. In addition to standard transmit and receive data lines, the UART1 also provides a full modem control handshake interface.

6.10.1 Features

- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Transmission FIFO control enables implementation of software (XON/XOFF) flow control on both UARTs.
- UART1 is equipped with standard modem interface signals. This module also provides full support for hardware flow control (auto-CTS/RTS).

6.10.2 UART features available in LPC2212/2214/01 only

Compared to previous LPC2000 microcontrollers, UARTs in LPC2212/2214/01 introduce a fractional baud rate generator for both UARTs, enabling these microcontrollers to achieve standard baud rates such as 115200 Bd with any crystal frequency above 2 MHz. In addition, auto-CTS/RTS flow-control functions are fully implemented in hardware.

- Fractional baud rate generator enables standard baud rates such as 115200 Bd to be achieved with any crystal frequency above 2 MHz.
- Auto-bauding.
- Auto-CTS/RTS flow-control fully implemented in hardware.

- Toggle on match.
- Do nothing on match.

6.14.2 Features available in LPC2212/2214/01 only

The LPC2212/2214/01 can count external events on one of the capture inputs if the external pulse lasts at least one half of the period of the PCLK. In this configuration, unused capture lines can be selected as regular timer capture inputs, or used as external interrupts.

- Timer can count cycles of either the peripheral clock (PCLK) or an externally supplied clock.
- When counting cycles of an externally supplied clock, only one of the timer's capture inputs can be selected as the timer's clock. The rate of such a clock is limited to $PCLK / 4$. Duration of high/low levels on the selected CAP input cannot be shorter than $1 / (2PCLK)$.

6.15 Watchdog timer

The purpose of the Watchdog is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, the Watchdog will generate a system reset if the user program fails to 'feed' (or reload) the Watchdog within a predetermined amount of time.

6.15.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect/incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 32-bit timer with internal prescaler.
- Selectable time period from $(T_{cy(PCLK)} \times 256 \times 4)$ to $(T_{cy(PCLK)} \times 2^{32} \times 4)$ in multiples of $T_{cy(PCLK)} \times 4$.

6.16 Real-time clock

The RTC is designed to provide a set of counters to measure time when normal or idle operating mode is selected. The RTC has been designed to use little power, making it suitable for battery powered systems where the CPU is not running continuously (Idle mode).

6.16.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra low power design to support battery powered systems.

- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Programmable reference clock divider allows adjustment of the RTC to match various crystal frequencies.

6.17 Pulse width modulator

The PWM is based on the standard Timer block and inherits all of its features, although only the PWM function is pinned out on the LPC2212/2214. The Timer is designed to count cycles of the peripheral clock (PCLK) and optionally generate interrupts or perform other actions when specified timer values occur, based on seven match registers. The PWM function is also based on match register events.

The ability to separately control rising and falling edge locations allows the PWM to be used for more applications. For instance, multi-phase motor control typically requires three non-overlapping PWM outputs with individual control of all three pulse widths and positions.

Two match registers can be used to provide a single edge controlled PWM output. One match register (MR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. Additional single edge controlled PWM outputs require only one match register each, since the repetition rate is the same for all PWM outputs. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when an MR0 match occurs.

Three match registers can be used to provide a PWM output with both edges controlled. Again, the MR0 match register controls the PWM cycle rate. The other match registers control the two PWM edge positions. Additional double edge controlled PWM outputs require only two match registers each, since the repetition rate is the same for all PWM outputs.

With double edge controlled PWM outputs, specific match registers control the rising and falling edge of the output. This allows both positive going PWM pulses (when the rising edge occurs prior to the falling edge), and negative going PWM pulses (when the falling edge occurs prior to the rising edge).

6.17.1 Features

- Seven match registers allow up to six single edge controlled or three double edge controlled PWM outputs, or a mix of both types.
- The match registers also allow:
 - Continuous operation with optional interrupt generation on match.
 - Stop timer on match with optional interrupt generation.
 - Reset timer on match with optional interrupt generation.
- Supports single edge controlled and/or double edge controlled PWM outputs. Single edge controlled PWM outputs all go HIGH at the beginning of each cycle unless the output is a constant LOW. Double edge controlled PWM outputs can have either edge occur at any position within a cycle. This allows for both positive going and negative going pulses.

7. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).^[1]

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DD(1V8)}	supply voltage (1.8 V)		[2] -0.5	+2.5	V
V _{DD(3V3)}	supply voltage (3.3 V)		[3] -0.5	+3.6	V
V _{DDA(3V3)}	analog supply voltage (3.3 V)		-0.5	+4.6	V
V _{IA}	analog input voltage		-0.5	+5.1	V
V _I	input voltage	5 V tolerant I/O pins	[4][5] -0.5	+6.0	V
		other I/O pins	[4][6] -0.5	V _{DD(3V3)} + 0.5	V
I _{DD}	supply current		[7][8] -	100	mA
I _{SS}	ground current		[8][9] -	100	mA
T _j	junction temperature		-	150	°C
T _{stg}	storage temperature		[10] -65	+150	°C
P _{tot(pack)}	total power dissipation (per package)	based on package heat transfer, not device power consumption	-	1.5	W
V _{esd}	electrostatic discharge voltage	human body model	[11]		
		all pins	-2000	+2000	V
		machine model	[12]		
		all pins	-200	+200	V

[1] The following applies to Table 5:

- a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.
- b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Internal rail.

[3] External rail.

[4] Including voltage on outputs in 3-state mode.

[5] Only valid when the V_{DD(3V3)} supply voltage is present.

[6] Not to exceed 4.6 V.

[7] Per supply pin.

[8] The peak current is limited to 25 times the corresponding maximum current.

[9] Per ground pin.

[10] Dependent on package type.

[11] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[12] Machine model: equivalent to discharging a 200 pF capacitor through a 0.75 μH coil and a 10 Ω series resistor.

Table 6. Static characteristics ...continued $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
Power consumption LPC2212, LPC2212/00, LPC2214, LPC2214/00						
I _{DD(act)}	active mode supply current	V _{DD(1V8)} = 1.8 V; CCLK = 60 MHz; T _{amb} = 25 °C; code while(1){} executed from flash; all peripherals enabled via PCONP ^[11] register but not configured to run	-	60	-	mA
I _{DD(pd)}	Power-down mode supply current	V _{DD(1V8)} = 1.8 V; T _{amb} = 25 °C	-	10	-	μA
		V _{DD(1V8)} = 1.8 V; T _{amb} = 85 °C	-	110	500	μA
Power consumption LPC2212/01 and LPC2214/01						
I _{DD(act)}	active mode supply current	V _{DD(1V8)} = 1.8 V; CCLK = 60 MHz; T _{amb} = 25 °C; code while(1){} executed from flash; all peripherals enabled via PCONP ^[11] register but not configured to run	-	41	-	mA
I _{DD(idle)}	Idle mode supply current	V _{DD(1V8)} = 1.8 V; CCLK = 60 MHz; T _{amb} = 25 °C; executed from flash; all peripherals enabled via PCONP ^[11] register but not configured to run	-	6.5	-	mA
I _{DD(pd)}	Power-down mode supply current	V _{DD(1V8)} = 1.8 V; T _{amb} = 25 °C	-	10	-	μA
		V _{DD(1V8)} = 1.8 V; T _{amb} = 85 °C	-	110	500	μA
I ² C-bus pins						
V _{IH}	HIGH-level input voltage		0.7V _{DD(3V3)}	-	-	V
V _{IL}	LOW-level input voltage		-	-	0.3V _{DD(3V3)}	V
V _{hys}	hysteresis voltage		-	0.05V _{DD(3V3)}	-	V
V _{OL}	LOW-level output voltage	I _{OLS} = 3 mA	^[7] -	-	0.4	V
I _{LI}	input leakage current	V _I = V _{DD(3V3)}	^[12] -	2	4	μA
		V _I = 5 V	-	10	22	μA

Table 7. ADC static characteristics

$V_{DDA} = 2.5\text{ V}$ to 3.6 V unless otherwise specified; $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ unless otherwise specified. ADC frequency 4.5 MHz .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IA}	analog input voltage		0	-	V_{DDA}	V
C_{ia}	analog input capacitance		-	-	1	pF
E_D	differential linearity error	[1][2][3]	-	-	± 1	LSB
$E_{L(adj)}$	integral non-linearity	[1][4]	-	-	± 2	LSB
E_O	offset error	[1][5]	-	-	± 3	LSB
E_G	gain error	[1][6]	-	-	± 0.5	%
E_T	absolute error	[1][7]	-	-	± 4	LSB

[1] Conditions: $V_{SSA} = 0\text{ V}$, $V_{DDA} = 3.3\text{ V}$.

[2] The ADC is monotonic, there are no missing codes.

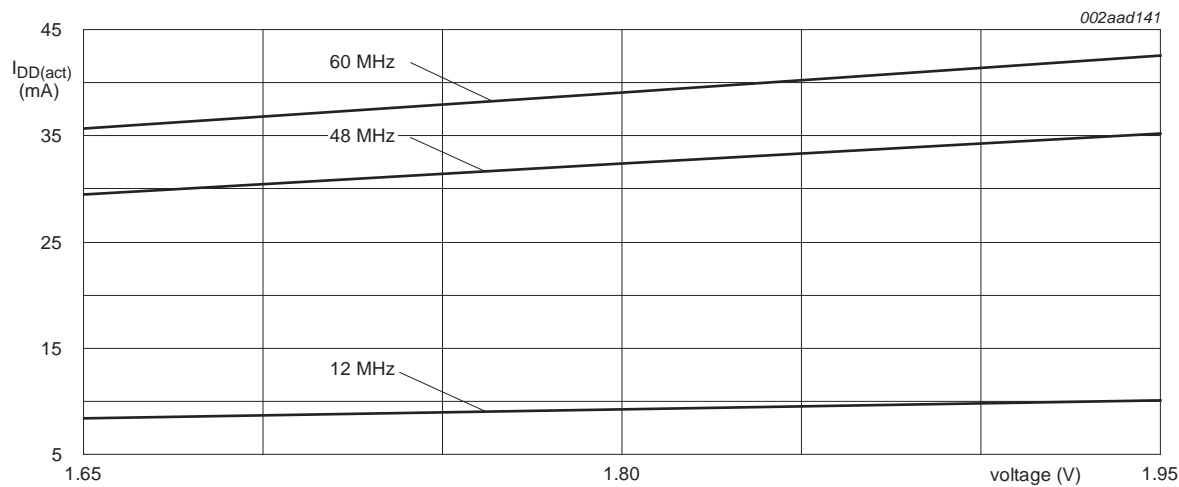
[3] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See [Figure 4](#).

[4] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See [Figure 4](#).

[5] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See [Figure 4](#).

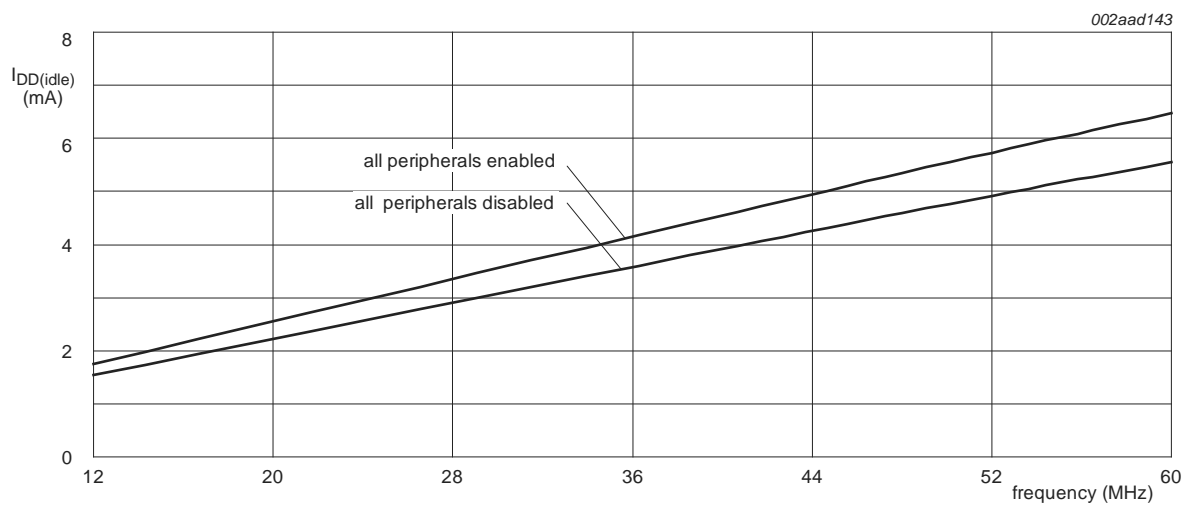
[6] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See [Figure 4](#).

[7] The absolute voltage error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See [Figure 4](#).



Test conditions: Active mode entered executing code from on-chip flash; $PCLK = CCLK/4$;
Temp = 25 °C; core voltage 1.8 V; all peripherals disabled.

Fig 7. Typical LPC2212/01 and LPC2214/01 $I_{DD(act)}$ measured at different voltages



Test conditions: Idle mode entered executing code from on-chip flash; $PCLK = CCLK/4$;
 $T_{amb} = 25\text{ °C}$; core voltage 1.8 V.

Fig 8. Typical LPC2212/01 and LPC2214/01 $I_{DD(idle)}$ measured at different frequencies

9. Dynamic characteristics

Table 9. Dynamic characteristics

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ for industrial applications; $V_{DD(1V8)}$, $V_{DD(3V3)}$ over specified ranges ^[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
External clock						
f_{osc}	oscillator frequency	supplied by an external oscillator (signal generator)	1	-	50	MHz
		external clock frequency supplied by an external crystal oscillator	1	-	30	MHz
		external clock frequency if on-chip PLL is used	10	-	25	MHz
		external clock frequency if on-chip bootloader is used for initial code download	10	-	25	MHz
$T_{cy(clk)}$	clock cycle time		20	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns
Port pins (except P0[2] and P0[3])						
t_r	rise time		-	10	-	ns
t_f	fall time		-	10	-	ns
I²C-bus pins (P0[2] and P0[3])						
t_f	fall time	V_{IH} to V_{IL}	^[2] $20 + 0.1 \times C_b$	-	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Bus capacitance C_b in pF, from 10 pF to 400 pF.

9.1 Timing

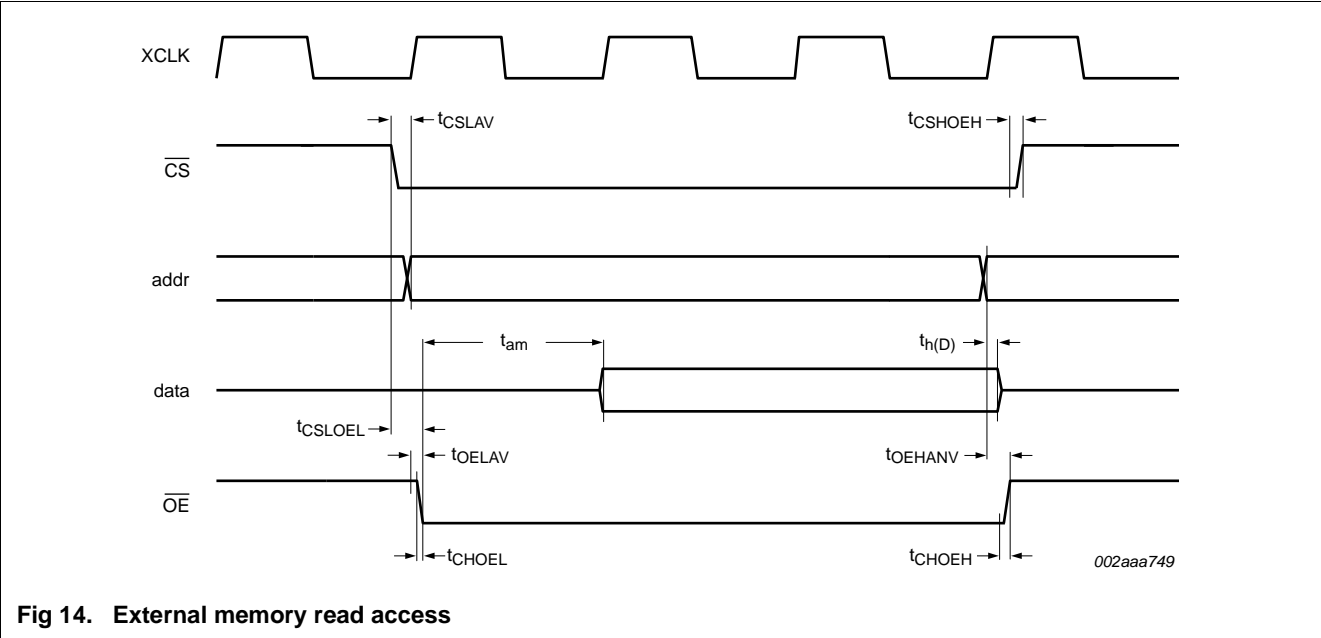


Fig 14. External memory read access

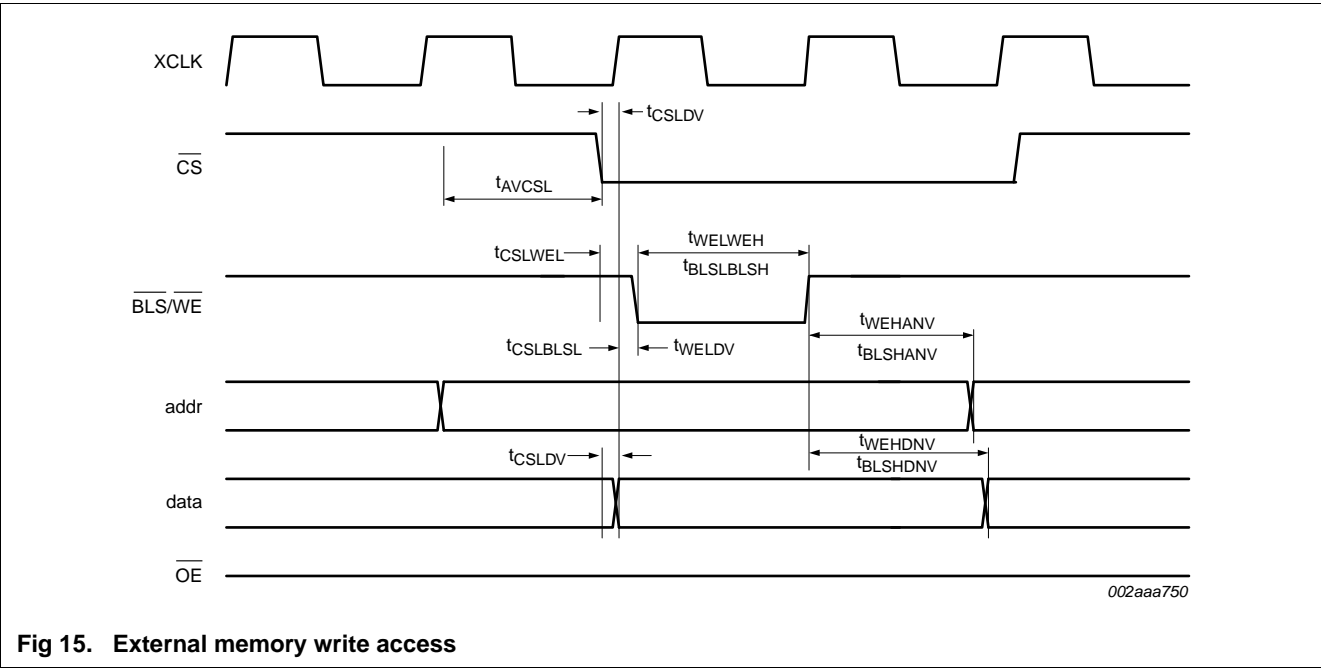
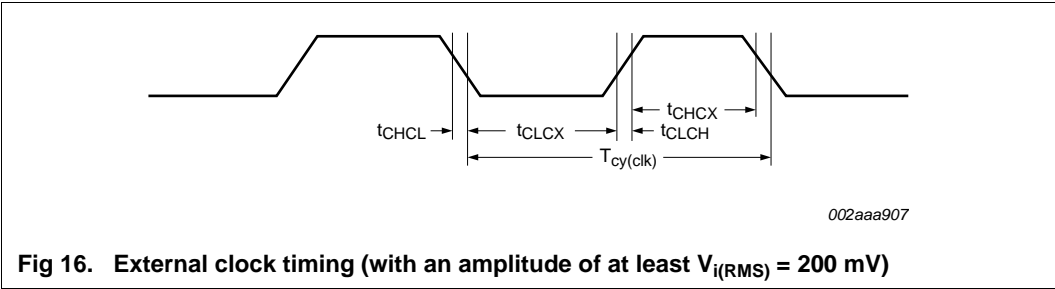


Fig 15. External memory write access



10. Package outline

LQFP144: plastic low profile quad flat package; 144 leads; body 20 x 20 x 1.4 mm

SOT486-1

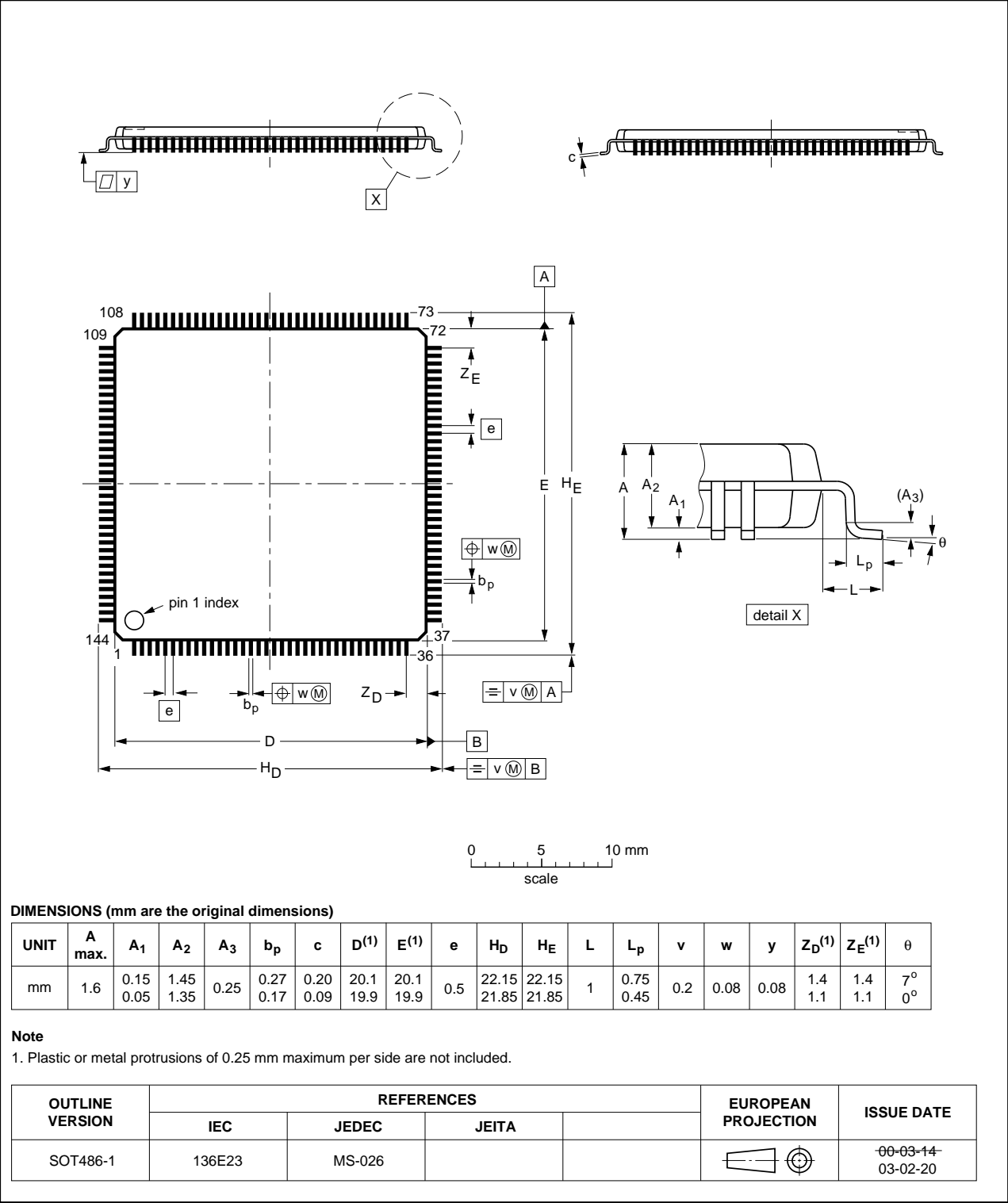


Fig 17. Package outline SOT486-1 (LQFP144)

11. Abbreviations

Table 12. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
CPU	Central Processing Unit
DCC	Debug Communications Channel
EMC	External Memory Controller
FIFO	First In, First Out
GPIO	General Purpose Input/Output
JTAG	Joint Test Action Group
PLL	Phase-Locked Loop
POR	Power-On Reset
PWM	Pulse Width Modulator
RAM	Random Access Memory
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SSI	Synchronous Serial Interface
SSP	Synchronous Serial Port
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter

13. Legal information

13.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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