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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	60MHz
Connectivity	EBI/EMI, FIFO, I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	PWM, WDT
Number of I/O	112
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 1.95V, 3V ~ 3.6V
Data Converters	A/D 8x10b SAR
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2214fbd144-01-5

3.1 Ordering options

Table 2. Ordering options

Type number	Flash memory	RAM	Fast GPIO/ SSP/ Enhanced UART, ADC, Timer	Temperature range
LPC2212FBD144/01	128 kB	16 kB	yes	−40 °C to +85 °C
LPC2214FBD144/01	256 kB	16 kB	yes	−40 °C to +85 °C

5.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
P0[0] to P0[31]		I/O	Port 0 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 0 pins depends upon the pin function selected via the Pin Connect Block. Pins 26 and 31 of port 0 are not available.
P0[0]/TXD0/PWM1	42	O	**TXD0 —** Transmitter output for UART0.
		O	**PWM1 —** Pulse Width Modulator output 1.
P0[1]/RXD0/PWM3/ EINT0	49	I	**RXD0 —** Receiver input for UART0.
		O	**PWM3 —** Pulse Width Modulator output 3.
		I	**EINT0 —** External interrupt 0 input
P0[2]/SCL/CAP0[0]	50	I/O	**SCL —** I^2C-bus clock input/output. Open-drain output (for I^2C-bus compliance).
		I	**CAP0[0] —** Capture input for Timer 0, channel 0.
P0[3]/SDA/MAT0[0]/ EINT1	58	I/O	**SDA —** I^2C-bus data input/output. Open-drain output (for I^2C-bus compliance).
		O	**MAT0[0] —** Match output for Timer 0, channel 0.
		I	**EINT1 —** External interrupt 1 input.
P0[4]/SCK0/CAP0[1]	59	I/O	**SCK0 —** Serial clock for SPI0. SPI clock output from master or input to slave.
		I	**CAP0[1] —** Capture input for Timer 0, channel 1.
P0[5]/MISO0/MAT0[1]	61	I/O	**MISO0 —** Master In Slave OUT for SPI0. Data input to SPI master or data output from SPI slave.
		O	**MAT0[1] —** Match output for Timer 0, channel 1.
P0[6]/MOSI0/CAP0[2]	68	I/O	**MOSI0 —** Master Out Slave In for SPI0. Data output from SPI master or data input to SPI slave.
		I	**CAP0[2] —** Capture input for Timer 0, channel 2.
P0[7]/SSEL0/PWM2/ EINT2	69	I	**SSEL0 —** Slave Select for SPI0. Selects the SPI interface as a slave.
		O	**PWM2 —** Pulse Width Modulator output 2.
		I	**EINT2 —** External interrupt 2 input.
P0[8]/TXD1/PWM4	75	O	**TXD1 —** Transmitter output for UART1.
		O	**PWM4 —** Pulse Width Modulator output 4.
P0[9]/RXD1/PWM6/ EINT3	76	I	**RXD1 —** Receiver input for UART1.
		O	**PWM6 —** Pulse Width Modulator output 6.
		I	**EINT3 —** External interrupt 3 input.
P0[10]/RTS1/CAP1[0]	78	O	**RTS1 —** Request to Send output for UART1.
		I	**CAP1[0] —** Capture input for Timer 1, channel 0.
P0[11]/CTS1/CAP1[1]	83	I	**CTS1 —** Clear to Send input for UART1.
		I	**CAP1[1] —** Capture input for Timer 1, channel 1.
P0[12]/DSR1/MAT1[0]	84	I	**DSR1 —** Data Set Ready input for UART1.
		O	**MAT1[0] —** Match output for Timer 1, channel 0.
P0[13]/DTR1/MAT1[1]	85	O	**DTR1 —** Data Terminal Ready output for UART1.
		O	**MAT1[1] —** Match output for Timer 1, channel 1.

Table 3. Pin description *…continued*

Symbol	Pin	Type	Description
P0[14]/DCD1/EINT1	92	I	**DCD1 —** Data Carrier Detect input for UART1.
		I	**EINT1 —** External interrupt 1 input. Note: LOW on this pin while $\overline{\text{RESET}}$ is LOW forces on-chip bootloader to take over control of the part after reset.
P0[15]/RI1/EINT2	99	I	**RI1 —** Ring Indicator input for UART1.
		I	**EINT2 —** External interrupt 2 input.
P0[16]/EINT0/MAT0[2]/ CAP0[2]	100	I	**EINT0 —** External interrupt 0 input.
		O	**MAT0[2] —** Match output for Timer 0, channel 2.
		I	**CAP0[2] —** Capture input for Timer 0, channel 2.
P0[17]/CAP1[2]/SCK1/ MAT1[2]	101	I	**CAP1[2] —** Capture input for Timer 1, channel 2.
		I/O	**SCK1 —** Serial Clock for SPI1/SSP[1]. SPI clock output from master or input to slave.
		O	**MAT1[2] —** Match output for Timer 1, channel 2.
P0[18]/CAP1[3]/MISO1/ MAT1[3]	121	I	**CAP1[3] —** Capture input for Timer 1, channel 3.
		I/O	**MISO1 —** Master In Slave Out for SPI1/SSP[1]. Data input to SPI master or data output from SPI slave.
		O	**MAT1[3] —** Match output for Timer 1, channel 3.
P0[19]/MAT1[2]/MOSI1/ CAP1[2]	122	O	**MAT1[2] —** Match output for Timer 1, channel 2.
		I/O	**MOSI1 —** Master Out Slave In for SPI1/SSP[1]. Data output from SPI master or data input to SPI slave.
		I	**CAP1[2] —** Capture input for Timer 1, channel 2.
P0[20]/MAT1[3]/SSEL1/ EINT3	123	O	**MAT1[3] —** Match output for Timer 1, channel 3.
		I	**SSEL1 —** Slave Select for SPI1/SSP[1]. Selects the SPI interface as a slave.
		I	**EINT3 —** External interrupt 3 input.
P0[21]/PWM5/CAP1[3]	4	O	**PWM5 —** Pulse Width Modulator output 5.
		I	**CAP1[3] —** Capture input for Timer 1, channel 3.
P0[22]/CAP0[0]/MAT0[0]	5	I	**CAP0[0] —** Capture input for Timer 0, channel 0.
		O	**MAT0[0] —** Match output for Timer 0, channel 0.
P0[23]	6	I/O	General purpose bidirectional digital port only.
P0[24]	8	I/O	General purpose bidirectional digital port only.
P0[25]	21	I/O	General purpose bidirectional digital port only.
P0[27]/AIN0/CAP0[1]/ MAT0[1]	23	I	**AIN0 —** ADC, input 0. This analog input is always connected to its pin.
		I	**CAP0[1] —** Capture input for Timer 0, channel 1.
		O	**MAT0[1] —** Match output for Timer 0, channel 1.
P0[28]/AIN1/CAP0[2]/ MAT0[2]	25	I	**AIN1 —** ADC, input 1. This analog input is always connected to its pin.
		I	**CAP0[2] —** Capture input for Timer 0, channel 2.
		O	**MAT0[2] —** Match output for Timer 0, channel 2.
P0[29]/AIN2/CAP0[3]/ MAT0[3]	32	I	**AIN2 —** ADC, input 2. This analog input is always connected to its pin.
		I	**CAP0[3] —** Capture input for Timer 0, Channel 3.
		O	**MAT0[3] —** Match output for Timer 0, channel 3.

6. Functional description

Details of the LPC2212/2214 systems and peripheral functions are described in the following sections.

6.1 Architectural overview

The ARM7TDMI-S is a general purpose 32-bit microprocessor, which offers high performance and very low power consumption. The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed Complex Instruction Set Computers. This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM7TDMI-S processor also employs a unique architectural strategy known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions, or applications where code density is an issue.

The key idea behind Thumb is that of a super-reduced instruction set. Essentially, the ARM7TDMI-S processor has two instruction sets:

- The standard 32-bit ARM set.
- A 16-bit Thumb set.

The Thumb set's 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARM's performance advantage over a traditional 16-bit processor using 16-bit registers. This is possible because Thumb code operates on the same 32-bit register set as ARM code.

Thumb code is able to provide up to 65 % of the code size of ARM, and 160 % of the performance of an equivalent ARM processor connected to a 16-bit memory system.

6.2 On-chip flash program memory

The LPC2212/2214 incorporate a 128 kB and 256 kB flash memory system respectively. This memory may be used for both code and data storage. Programming of the flash memory may be accomplished in several ways. It may be programmed In System via the serial port. The application program may also erase and/or program the flash while the application is running, allowing a great degree of flexibility for data storage field firmware upgrades, etc. When on-chip bootloader is used, 120/248 kB of flash memory is available for user code.

The LPC2212/2214 flash memory provides a minimum of 100000 erase/write cycles and 20 years of data retention.

On-chip bootloader (as of revision 1.60) provides Code Read Protection (CRP) for the LPC2212/2214 on-chip flash memory. When the CRP is enabled, the JTAG debug port, external memory boot and ISP commands accessing either the on-chip RAM or flash memory are disabled. However, the ISP flash erase command can be executed at any

time (no matter whether the CRP is on or off). Removal of CRP is achieved by erasure of full on-chip user flash. With the CRP off, full access to the chip via the JTAG and/or ISP is restored.

6.3 On-chip static RAM

On-chip static RAM may be used for code and/or data storage. The SRAM may be accessed as 8 bit, 16 bit, and 32 bit. The LPC2212/2214 provide 16 kB of static RAM.

6.4 Memory map

The LPC2212/2214 memory maps incorporate several distinct regions, as shown in the following figures.

In addition, the CPU interrupt vectors may be re-mapped to allow them to reside in either flash memory (the default) or on-chip static RAM. This is described in Section 6.18 “System control”.

6.11 I²C-bus serial I/O controller

The I²C-bus is a bidirectional bus for inter-IC control using only two wires: a serial clock line (SCL), and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g. an LCD driver or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I²C-bus is a multi-master bus; it can be controlled by more than one bus master connected to it.

The I²C-bus implemented in LPC2212/2214 supports a bit rate up to 400 kbit/s (Fast I²C-bus).

6.11.1 Features

- Standard I²C-bus compliant interface.
- Easy to configure as Master, Slave, or Master/Slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I²C-bus may be used for test and diagnostic purposes.

6.12 SPI serial I/O controller

The LPC2212/2214 each contain two SPIs. The SPI is a full duplex serial interface, designed to be able to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends a byte of data to the slave, and the slave always sends a byte of data to the master.

6.12.1 Features

- Compliant with Serial Peripheral Interface (SPI) specification.
- Synchronous, Serial, Full Duplex communication.
- Combined SPI master and slave.
- Maximum data bit rate of $1/8$ of the input clock rate.

6.12.2 Features available in LPC2212/2214/01 only

- Eight to 16 bits per frame.

- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Programmable reference clock divider allows adjustment of the RTC to match various crystal frequencies.

6.17 Pulse width modulator

The PWM is based on the standard Timer block and inherits all of its features, although only the PWM function is pinned out on the LPC2212/2214. The Timer is designed to count cycles of the peripheral clock (PCLK) and optionally generate interrupts or perform other actions when specified timer values occur, based on seven match registers. The PWM function is also based on match register events.

The ability to separately control rising and falling edge locations allows the PWM to be used for more applications. For instance, multi-phase motor control typically requires three non-overlapping PWM outputs with individual control of all three pulse widths and positions.

Two match registers can be used to provide a single edge controlled PWM output. One match register (MR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. Additional single edge controlled PWM outputs require only one match register each, since the repetition rate is the same for all PWM outputs. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when an MR0 match occurs.

Three match registers can be used to provide a PWM output with both edges controlled. Again, the MR0 match register controls the PWM cycle rate. The other match registers control the two PWM edge positions. Additional double edge controlled PWM outputs require only two match registers each, since the repetition rate is the same for all PWM outputs.

With double edge controlled PWM outputs, specific match registers control the rising and falling edge of the output. This allows both positive going PWM pulses (when the rising edge occurs prior to the falling edge), and negative going PWM pulses (when the falling edge occurs prior to the rising edge).

6.17.1 Features

- Seven match registers allow up to six single edge controlled or three double edge controlled PWM outputs, or a mix of both types.
- The match registers also allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Supports single edge controlled and/or double edge controlled PWM outputs. Single edge controlled PWM outputs all go HIGH at the beginning of each cycle unless the output is a constant LOW. Double edge controlled PWM outputs can have either edge occur at any position within a cycle. This allows for both positive going and negative going pulses.

- Pulse period and width can be any number of timer counts. This allows complete flexibility in the trade-off between resolution and repetition rate. All PWM outputs will occur at the same repetition rate.
- Double edge controlled PWM outputs can be programmed to be either positive going or negative going pulses.
- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must 'release' new match values before they can become effective.
- May be used as a standard timer if the PWM mode is not enabled.
- A 32-bit Timer/Counter with a programmable 32-bit Prescaler.

6.18 System control

6.18.1 Crystal oscillator

The oscillator supports crystals in the range of 1 MHz to 30 MHz. The oscillator output frequency is called f_{osc} and the ARM processor clock frequency is referred to as CCLK for purposes of rate equations, etc. f_{osc} and CCLK are the same value unless the PLL is running and connected. Refer to Section 6.18.2 "PLL" for additional information.

6.18.2 PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up into the range of 10 MHz to 60 MHz with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32 (in practice, the multiplier value cannot be higher than 6 on this family of microcontrollers due to the upper frequency limit of the CPU). The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip Reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to Lock, then connect to the PLL as a clock source. The PLL settling time is 100 μs.

6.18.3 Reset and wake-up timer

Reset has two sources on the LPC2212/2214: the $\overline{\text{RESET}}$ pin and Watchdog Reset. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin with an additional glitch filter. Assertion of chip Reset by any source starts the Wake-up Timer (see Wake-up Timer description below), causing the internal chip reset to remain asserted until the external Reset is de-asserted, the oscillator is running, a fixed number of clocks have passed, and the on-chip flash controller has completed its initialization.

When the internal Reset is removed, the processor begins executing at address 0, which is the Reset vector. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

The Wake-up Timer ensures that the oscillator and other analog functions required for chip operation are fully functional before the processor is allowed to execute instructions. This is important at power on, all types of Reset, and whenever any of the aforementioned

The ARM core has a Debug Communication Channel function built-in. The debug communication channel allows a program running on the target to communicate with the host debugger or another separate host without stopping the program flow or even entering the debug state. The debug communication channel is accessed as a co-processor 14 by the program running on the ARM7TDMI-S core. The debug communication channel allows the JTAG port to be used for sending and receiving data without affecting the normal program flow. The debug communication channel data and control registers are mapped in to addresses in the EmbeddedICE logic.

The JTAG clock (TCK) must be slower than $\frac{1}{6}$ of the CPU clock (CCLK) for the JTAG interface to operate.

6.19.2 Embedded trace macrocell

Since the LPC2212/2214 have significant amounts of on-chip memory, it is not possible to determine how the processor core is operating simply by observing the external pins. The Embedded Trace Macrocell (ETM) provides real-time trace capability for deeply embedded processor cores. It outputs information about processor execution to the trace port.

The ETM is connected directly to the ARM core and not to the main AMBA system bus. It compresses the trace information and exports it through a narrow trace port. An external trace port analyzer must capture the trace information under software debugger control. Instruction trace (or PC trace) shows the flow of execution of the processor and provides a list of all the instructions that were executed. Instruction trace is significantly compressed by only broadcasting branch addresses as well as a set of status signals that indicate the pipeline status on a cycle by cycle basis. Trace information generation can be controlled by selecting the trigger resource. Trigger resources include address comparators, counters and sequencers. Since trace information is compressed the software debugger requires a static image of the code being executed. Self-modifying code can not be traced because of this restriction.

6.19.3 RealMonitor

RealMonitor is a configurable software module, developed by ARM Inc., which enables real time debug. It is a lightweight debug monitor that runs in the background while users debug their foreground application. It communicates with the host using the DCC (Debug Communications Channel), which is present in the EmbeddedICE logic. The LPC2212/2214 contain a specific configuration of RealMonitor software programmed into the on-chip flash memory.

7. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(1V8)}$	supply voltage (1.8 V)		[2]	−0.5	+2.5	V
$V_{DD(3V3)}$	supply voltage (3.3 V)		[3]	−0.5	+3.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)			−0.5	+4.6	V
V_{IA}	analog input voltage			−0.5	+5.1	V
V_I	input voltage	5 V tolerant I/O pins	[4][5]	−0.5	+6.0	V
		other I/O pins	[4][6]	−0.5	$V_{DD(3V3)}$ + 0.5	V
I_{DD}	supply current		[7][8]	-	100	mA
I_{SS}	ground current		[8][9]	-	100	mA
T_j	junction temperature			-	150	°C
T_{stg}	storage temperature		[10]	−65	+150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{esd}	electrostatic discharge voltage	human body model	[11]			
		all pins		−2000	+2000	V
		machine model	[12]			
		all pins		−200	+200	V

[1] The following applies to Table 5:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Internal rail.

[3] External rail.

[4] Including voltage on outputs in 3-state mode.

[5] Only valid when the $V_{DD(3V3)}$ supply voltage is present.

[6] Not to exceed 4.6 V.

[7] Per supply pin.

[8] The peak current is limited to 25 times the corresponding maximum current.

[9] Per ground pin.

[10] Dependent on package type.

[11] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[12] Machine model: equivalent to discharging a 200 pF capacitor through a 0.75 μH coil and a 10 Ω series resistor.

Table 6. Static characteristics *…continued*

T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
Oscillator pins						
$V_{i(XTAL1)}$	input voltage on pin XTAL1		0	-	1.8	V
$V_{o(XTAL2)}$	output voltage on pin XTAL2		0	-	1.8	V

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] Internal rail.

[3] External rail.

[4] Including voltage on outputs in 3-state mode.

[5] $V_{DD(3V3)}$ supply voltages must be present.

[6] 3-state outputs go into 3-state mode when $V_{DD(3V3)}$ is grounded.

[7] Accounts for 100 mV voltage drop in all supply lines.

[8] Only allowed for a short time period.

[9] Minimum condition for V_I = 4.5 V, maximum condition for V_I = 5.5 V.

[10] Applies to P1[25:16].

[11] See the *LPC2114/2124/2212/2214 User Manual*.

[12] To V_{SS}.

Table 7. ADC static characteristics

V_{DDA} = 2.5 V to 3.6 V unless otherwise specified; T_{amb} = −40 °C to +85 °C unless otherwise specified. ADC frequency 4.5 MHz.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IA}	analog input voltage			0	-	V_{DDA}	V
C_{ia}	analog input capacitance			-	-	1	pF
E_D	differential linearity error		[1][2][3]	-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity		[1][4]	-	-	±2	LSB
E_O	offset error		[1][5]	-	-	±3	LSB
E_G	gain error		[1][6]	-	-	±0.5	%
E_T	absolute error		[1][7]	-	-	±4	LSB

[1] Conditions: V_{SSA} = 0 V, V_{DDA} = 3.3 V.

[2] The ADC is monotonic, there are no missing codes.

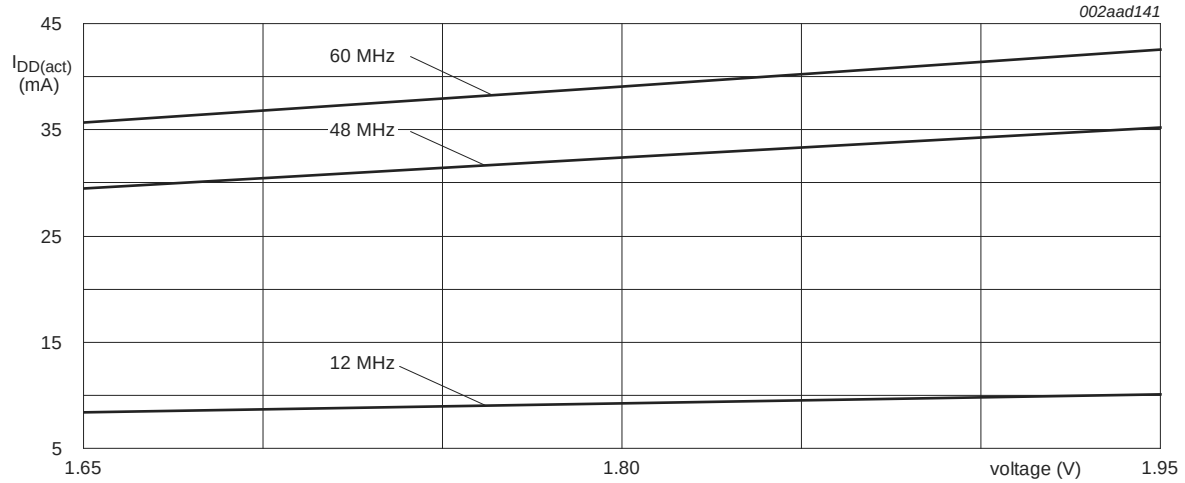
[3] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 4.

[4] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 4.

[5] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 4.

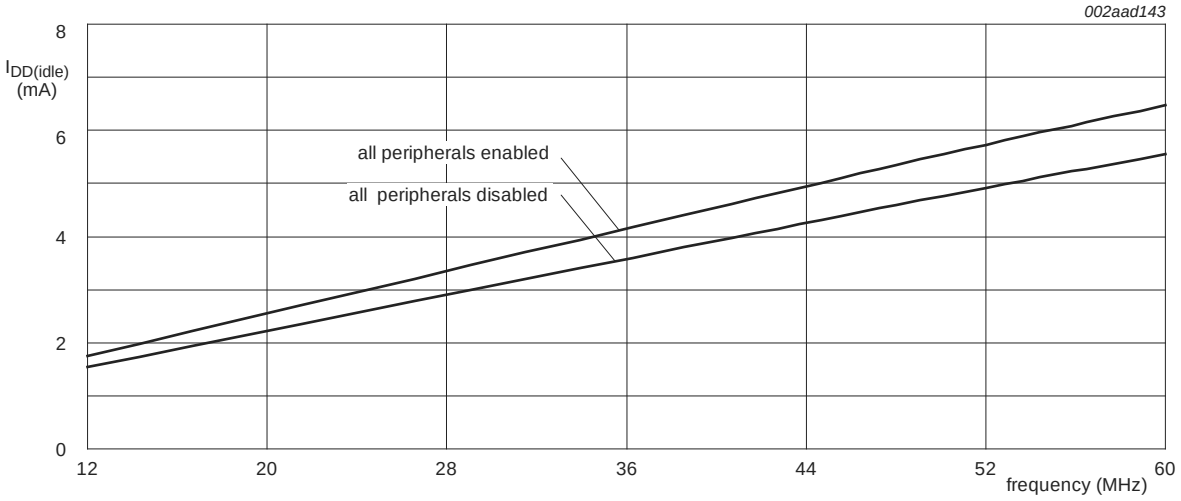
[6] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 4.

[7] The absolute voltage error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 4.



Test conditions: Active mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$;
Temp = 25 °C; core voltage 1.8 V; all peripherals disabled.

Fig 7. Typical LPC2212/01 and LPC2214/01 $I_{DD(act)}$ measured at different voltages



Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$;
T_{amb} = 25 °C; core voltage 1.8 V.

Fig 8. Typical LPC2212/01 and LPC2214/01 $I_{DD(idle)}$ measured at different frequencies

9. Dynamic characteristics

Table 9. Dynamic characteristics

T_{amb} = −40 °C to +85 °C for industrial applications; $V_{DD(1V8)}$, $V_{DD(3V3)}$ over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
External clock						
f_{osc}	oscillator frequency	supplied by an external oscillator (signal generator)	1	-	50	MHz
		external clock frequency supplied by an external crystal oscillator	1	-	30	MHz
		external clock frequency if on-chip PLL is used	10	-	25	MHz
		external clock frequency if on-chip bootloader is used for initial code download	10	-	25	MHz
$T_{cy(clk)}$	clock cycle time		20	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns
Port pins (except P0[2] and P0[3])						
t_r	rise time		-	10	-	ns
t_f	fall time		-	10	-	ns
I^2C-bus pins (P0[2] and P0[3])						
t_f	fall time	V_{IH} to V_{IL}	[2] $20 + 0.1 \times C_b$	-	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Bus capacitance C_b in pF, from 10 pF to 400 pF.

9.1 Timing

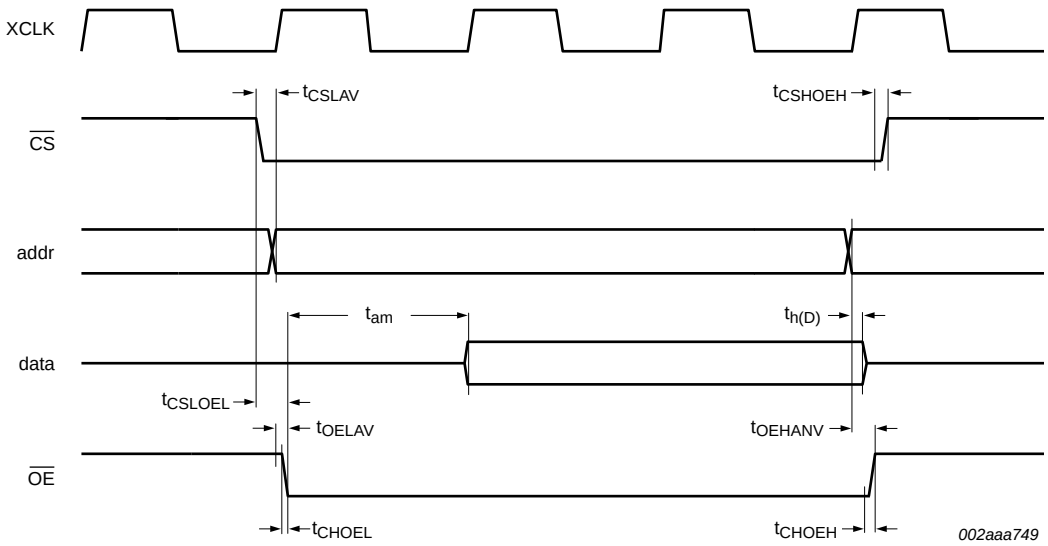


Fig 14. External memory read access

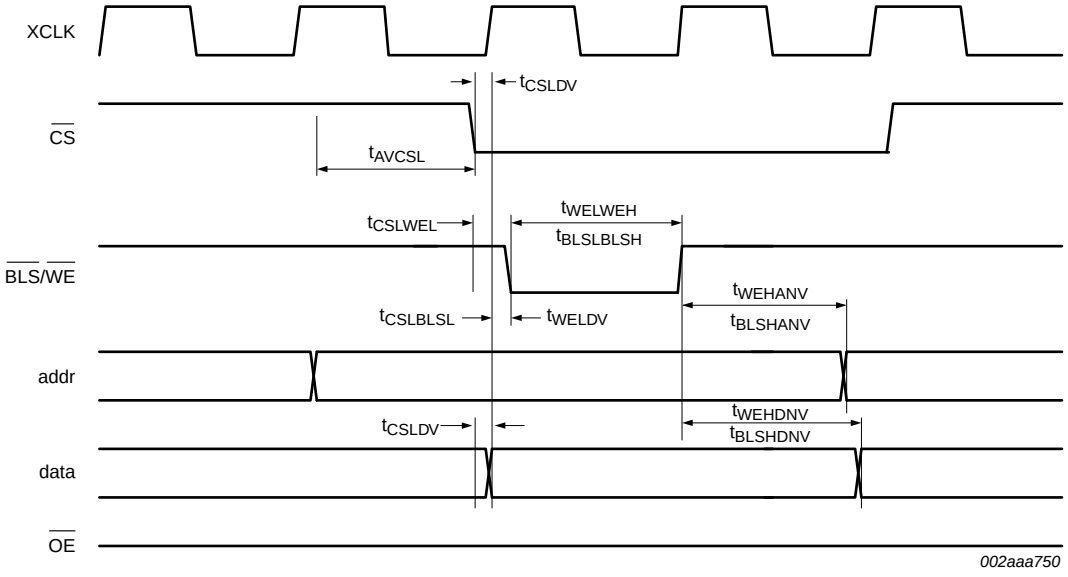


Fig 15. External memory write access

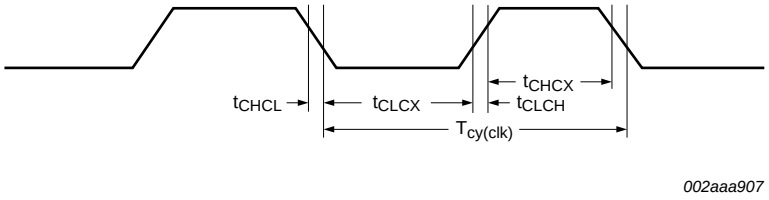


Fig 16. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

11. Abbreviations

Table 12. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
CPU	Central Processing Unit
DCC	Debug Communications Channel
EMC	External Memory Controller
FIFO	First In, First Out
GPIO	General Purpose Input/Output
JTAG	Joint Test Action Group
PLL	Phase-Locked Loop
POR	Power-On Reset
PWM	Pulse Width Modulator
RAM	Random Access Memory
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SSI	Synchronous Serial Interface
SSP	Synchronous Serial Port
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter

12. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC2212_2214 v.5	20110614	Product data sheet	201004021F	LPC2212_2214 v.4
Modifications:	• Table 6 “Static characteristics”; Changed /01 Power-down mode supply current ($I_{DD(pd)}$) from 180 μA to 500 μA for industrial temperature range. • Table 6 “Static characteristics”; Moved V_{hys} voltage from typical to minimum. • Table 6 “Static characteristics”; Changed I^2C pad hysteresis from $0.5V_{DD(3V3)}$ to $0.05V_{DD(3V3)}$.			
LPC2212_2214 v.4	20080103	Product data sheet	-	LPC2212_2214 v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Type number LPC2212FBD144/01 has been added. • Type number LPC2214FBD144/01 has been added. • Details introduced with /01 devices on new peripherals/features (Fast I/O Ports, SSP, CRP) and enhancements to existing ones (UART0/1, Timers, ADC, and SPI) added. • Power consumption measurements for LPC2212/01 and LPC2214/01 added. • Description of JTAG pin TCK has been updated.			
LPC2212_2214 v.3	20060719	Product data sheet	-	LPC2212_2214 v.2
LPC2212_2214 v.2	20041223	Product data	-	LPC2212_2214 v.1
LPC2212_2214 v.1	20040202	Preliminary data	-	-

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13.4 Trademarks

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14. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

15. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

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