Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	60MHz
Connectivity	EBI/EMI, I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	112
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 1.95V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2214fbd144-551

- 16 kB on-chip static RAM and 128/256 kB on-chip flash program memory. 128-bit wide interface/accelerator enables high speed 60 MHz operation.
- In-System Programming (ISP) and In-Application Programming (IAP) via on-chip bootloader software. Flash programming takes 1 ms per 512 B line. Single sector or full chip erase takes 400 ms.
- EmbeddedICE-RT and Embedded Trace interfaces offer real-time debugging with the on-chip RealMonitor software as well as high speed real-time tracing of instruction execution.
- Eight-channel 10-bit ADC with conversion time as low as 2.44 μs.
- Two 32-bit timers (with four capture and four compare channels), PWM unit (six outputs), Real-Time Clock and Watchdog.
- Multiple serial interfaces including two UARTs (16C550), Fast I^2C-bus (400 kbit/s) and two SPIs.
- Vectored Interrupt Controller with configurable priorities and vector addresses.
- Configurable external memory interface with up to four banks, each up to 16 MB and 8/16/32-bit data width.
- Up to 112 general purpose I/O pins (5 V tolerant). Up to nine edge or level sensitive external interrupt pins available.
- 60 MHz maximum CPU clock available from programmable on-chip Phase-Locked Loop with settling time of 100 μs.
- On-chip crystal oscillator with an operating range of 1 MHz to 30 MHz.
- Two low power modes, Idle and Power-down.
- Processor wake-up from Power-down mode via external interrupt.
- Individual enable/disable of peripheral functions for power optimization.
- Dual power supply:
  - CPU operating voltage range of 1.65 V to 1.95 V (1.8 V ± 0.15 V).
  - I/O power supply range of 3.0 V to 3.6 V (3.3 V ± 10 %) with 5 V tolerant I/O pads.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC2212FBD144/01	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC2214FBD144/01	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1

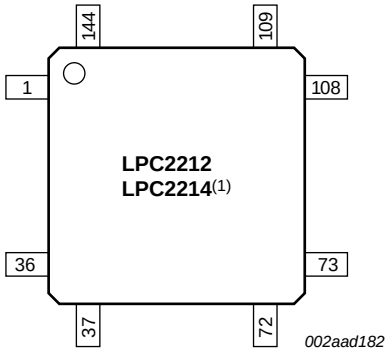
3.1 Ordering options

Table 2. Ordering options

Type number	Flash memory	RAM	Fast GPIO/ SSP/ Enhanced UART, ADC, Timer	Temperature range
LPC2212FBD144/01	128 kB	16 kB	yes	−40 °C to +85 °C
LPC2214FBD144/01	256 kB	16 kB	yes	−40 °C to +85 °C

5. Pinning information

5.1 Pinning



(1) Pin configuration is identical for devices with and without /00 and /01 suffixes.

Fig 2. Pin configuration (LQFP144)

5.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
P0[0] to P0[31]		I/O	Port 0 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 0 pins depends upon the pin function selected via the Pin Connect Block. Pins 26 and 31 of port 0 are not available.
P0[0]/TXD0/PWM1	42	O	**TXD0 —** Transmitter output for UART0.
		O	**PWM1 —** Pulse Width Modulator output 1.
P0[1]/RXD0/PWM3/ EINT0	49	I	**RXD0 —** Receiver input for UART0.
		O	**PWM3 —** Pulse Width Modulator output 3.
		I	**EINT0 —** External interrupt 0 input
P0[2]/SCL/CAP0[0]	50	I/O	**SCL —** I^2C-bus clock input/output. Open-drain output (for I^2C-bus compliance).
		I	**CAP0[0] —** Capture input for Timer 0, channel 0.
P0[3]/SDA/MAT0[0]/ EINT1	58	I/O	**SDA —** I^2C-bus data input/output. Open-drain output (for I^2C-bus compliance).
		O	**MAT0[0] —** Match output for Timer 0, channel 0.
		I	**EINT1 —** External interrupt 1 input.
P0[4]/SCK0/CAP0[1]	59	I/O	**SCK0 —** Serial clock for SPI0. SPI clock output from master or input to slave.
		I	**CAP0[1] —** Capture input for Timer 0, channel 1.
P0[5]/MISO0/MAT0[1]	61	I/O	**MISO0 —** Master In Slave OUT for SPI0. Data input to SPI master or data output from SPI slave.
		O	**MAT0[1] —** Match output for Timer 0, channel 1.
P0[6]/MOSI0/CAP0[2]	68	I/O	**MOSI0 —** Master Out Slave In for SPI0. Data output from SPI master or data input to SPI slave.
		I	**CAP0[2] —** Capture input for Timer 0, channel 2.
P0[7]/SSEL0/PWM2/ EINT2	69	I	**SSEL0 —** Slave Select for SPI0. Selects the SPI interface as a slave.
		O	**PWM2 —** Pulse Width Modulator output 2.
		I	**EINT2 —** External interrupt 2 input.
P0[8]/TXD1/PWM4	75	O	**TXD1 —** Transmitter output for UART1.
		O	**PWM4 —** Pulse Width Modulator output 4.
P0[9]/RXD1/PWM6/ EINT3	76	I	**RXD1 —** Receiver input for UART1.
		O	**PWM6 —** Pulse Width Modulator output 6.
		I	**EINT3 —** External interrupt 3 input.
P0[10]/RTS1/CAP1[0]	78	O	**RTS1 —** Request to Send output for UART1.
		I	**CAP1[0] —** Capture input for Timer 1, channel 0.
P0[11]/CTS1/CAP1[1]	83	I	**CTS1 —** Clear to Send input for UART1.
		I	**CAP1[1] —** Capture input for Timer 1, channel 1.
P0[12]/DSR1/MAT1[0]	84	I	**DSR1 —** Data Set Ready input for UART1.
		O	**MAT1[0] —** Match output for Timer 1, channel 0.
P0[13]/DTR1/MAT1[1]	85	O	**DTR1 —** Data Terminal Ready output for UART1.
		O	**MAT1[1] —** Match output for Timer 1, channel 1.

Table 3. Pin description *…continued*

Symbol	Pin	Type	Description
P0[30]/AIN3/EINT3/ CAP0[0]	33	I	**AIN3 —** ADC, input 3. This analog input is always connected to its pin.
		I	**EINT3 —** External interrupt 3 input.
		I	**CAP0[0] —** Capture input for Timer 0, channel 0.
P1[0] to P1[31]		I/O	Port 1 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 1 pins depends upon the pin function selected via the Pin Connect Block. Pins 2 through 15 of port 1 are not available.
P1[0]/CS0	91	O	LOW-active Chip Select 0 signal. (Bank 0 addresses range 0x8000 0000 to 0x80FF FFFF)
P1[1]/OE	90	O	LOW-active Output Enable signal.
P1[16]/TRACEPKT0	34	O	Trace Packet, bit 0. Standard I/O port with internal pull-up.
P1[17]/TRACEPKT1	24	O	Trace Packet, bit 1. Standard I/O port with internal pull-up.
P1[18]/TRACEPKT2	15	O	Trace Packet, bit 2. Standard I/O port with internal pull-up.
P1[19]/TRACEPKT3	7	O	Trace Packet, bit 3. Standard I/O port with internal pull-up.
P1[20]/TRACESYNC	102	O	Trace Synchronization; standard I/O port with internal pull-up. Note: LOW on this pin while $\overline{\text{RESET}}$ is LOW, enables pins P1[25:16] to operate as Trace port after reset.
P1[21]/PIPESTAT0	95	O	Pipeline Status, bit 0. Standard I/O port with internal pull-up.
P1[22]/PIPESTAT1	86	O	Pipeline Status, bit 1. Standard I/O port with internal pull-up.
P1[23]/PIPESTAT2	82	O	Pipeline Status, bit 2. Standard I/O port with internal pull-up.
P1[24]/TRACECLK	70	O	Trace Clock. Standard I/O port with internal pull-up.
P1[25]/EXTIN0	60	I	External Trigger Input. Standard I/O with internal pull-up.
P1[26]/RTCK	52	I/O	Returned Test Clock output. Extra signal added to the JTAG port. Assists debugger synchronization when processor frequency varies. Bidirectional pin with internal pull-up. Note: LOW on this pin while $\overline{\text{RESET}}$ is LOW, enables pins P1[31:26] to operate as Debug port after reset.
P1[27]/TDO	144	O	Test Data out for JTAG interface.
P1[28]/TDI	140	I	Test Data in for JTAG interface.
P1[29]/TCK	126	I	Test Clock for JTAG interface. This clock must be slower than $\frac{1}{6}$ of the CPU clock (CCLK) for the JTAG interface to operate.
P1[30]/TMS	113	I	Test Mode Select for JTAG interface.
P1[31]/$\overline{\text{TRST}}$	43	I	Test Reset for JTAG interface.
P2[0] to P2[31]		I/O	Port 2 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 2 pins depends upon the pin function selected via the Pin Connect Block.
P2[0]/D0	98	I/O	External memory data line 0.
P2[1]/D1	105	I/O	External memory data line 1.
P2[2]/D2	106	I/O	External memory data line 2.
P2[3]/D3	108	I/O	External memory data line 3.
P2[4]/D4	109	I/O	External memory data line 4.
P2[5]/D5	114	I/O	External memory data line 5.
P2[6]/D6	115	I/O	External memory data line 6.

Table 3. Pin description *…continued*

Symbol	Pin	Type	Description
P3[3]/A3	81	O	External memory address line 3.
P3[4]/A4	80	O	External memory address line 4.
P3[5]/A5	74	O	External memory address line 5.
P3[6]/A6	73	O	External memory address line 6.
P3[7]/A7	72	O	External memory address line 7.
P3[8]/A8	71	O	External memory address line 8.
P3[9]/A9	66	O	External memory address line 9.
P3[10]/A10	65	O	External memory address line 10.
P3[11]/A11	64	O	External memory address line 11.
P3[12]/A12	63	O	External memory address line 12.
P3[13]/A13	62	O	External memory address line 13.
P3[14]/A14	56	O	External memory address line 14.
P3[15]/A15	55	O	External memory address line 15.
P3[16]/A16	53	O	External memory address line 16.
P3[17]/A17	48	O	External memory address line 17.
P3[18]/A18	47	O	External memory address line 18.
P3[19]/A19	46	O	External memory address line 19.
P3[20]/A20	45	O	External memory address line 20.
P3[21]/A21	44	O	External memory address line 21.
P3[22]/A22	41	O	External memory address line 22.
P3[23]/A23/XCLK	40	O	**A23 —** External memory address line 23.
		O	**XCLK —** Clock output.
P3[24]/CS3	36	O	LOW-active Chip Select 3 signal. (Bank 3 addresses range 0x8300 0000 to 0x83FF FFFF)
P3[25]/CS2	35	O	LOW-active Chip Select 2 signal. (Bank 2 addresses range 0x8200 0000 to 0x82FF FFFF)
P3[26]/CS1	30	O	LOW-active Chip Select 1 signal. (Bank 1 addresses range 0x8100 0000 to 0x81FF FFFF)
P3[27]/WE	29	O	LOW-active Write enable signal.
P3[28]/BLS3/AIN7	28	O	**BLS3 —** LOW-active Byte Lane Select signal (Bank 3).
		I	**AIN7 —** ADC, input 7. This analog input is always connected to its pin.
P3[29]/BLS2/AIN6	27	O	**BLS2 —** LOW-active Byte Lane Select signal (Bank 2).
		I	**AIN6 —** ADC, input 6. This analog input is always connected to its pin.
P3[30]/BLS1	97	O	LOW-active Byte Lane Select signal (Bank 1).
P3[31]/BLS0	96	O	LOW-active Byte Lane Select signal (Bank 0).
n.c.	22		Pin not connected.
$\overline{\text{RESET}}$	135	I	external reset input; a LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. TTL with hysteresis, 5 V tolerant.
XTAL1	142	I	input to the oscillator circuit and internal clock generator circuits.
XTAL2	141	O	output from the oscillator amplifier.

6. Functional description

Details of the LPC2212/2214 systems and peripheral functions are described in the following sections.

6.1 Architectural overview

The ARM7TDMI-S is a general purpose 32-bit microprocessor, which offers high performance and very low power consumption. The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed Complex Instruction Set Computers. This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM7TDMI-S processor also employs a unique architectural strategy known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions, or applications where code density is an issue.

The key idea behind Thumb is that of a super-reduced instruction set. Essentially, the ARM7TDMI-S processor has two instruction sets:

- The standard 32-bit ARM set.
- A 16-bit Thumb set.

The Thumb set's 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARM's performance advantage over a traditional 16-bit processor using 16-bit registers. This is possible because Thumb code operates on the same 32-bit register set as ARM code.

Thumb code is able to provide up to 65 % of the code size of ARM, and 160 % of the performance of an equivalent ARM processor connected to a 16-bit memory system.

6.2 On-chip flash program memory

The LPC2212/2214 incorporate a 128 kB and 256 kB flash memory system respectively. This memory may be used for both code and data storage. Programming of the flash memory may be accomplished in several ways. It may be programmed In System via the serial port. The application program may also erase and/or program the flash while the application is running, allowing a great degree of flexibility for data storage field firmware upgrades, etc. When on-chip bootloader is used, 120/248 kB of flash memory is available for user code.

The LPC2212/2214 flash memory provides a minimum of 100000 erase/write cycles and 20 years of data retention.

On-chip bootloader (as of revision 1.60) provides Code Read Protection (CRP) for the LPC2212/2214 on-chip flash memory. When the CRP is enabled, the JTAG debug port, external memory boot and ISP commands accessing either the on-chip RAM or flash memory are disabled. However, the ISP flash erase command can be executed at any

time (no matter whether the CRP is on or off). Removal of CRP is achieved by erasure of full on-chip user flash. With the CRP off, full access to the chip via the JTAG and/or ISP is restored.

6.3 On-chip static RAM

On-chip static RAM may be used for code and/or data storage. The SRAM may be accessed as 8 bit, 16 bit, and 32 bit. The LPC2212/2214 provide 16 kB of static RAM.

6.4 Memory map

The LPC2212/2214 memory maps incorporate several distinct regions, as shown in the following figures.

In addition, the CPU interrupt vectors may be re-mapped to allow them to reside in either flash memory (the default) or on-chip static RAM. This is described in Section 6.18 “System control”.

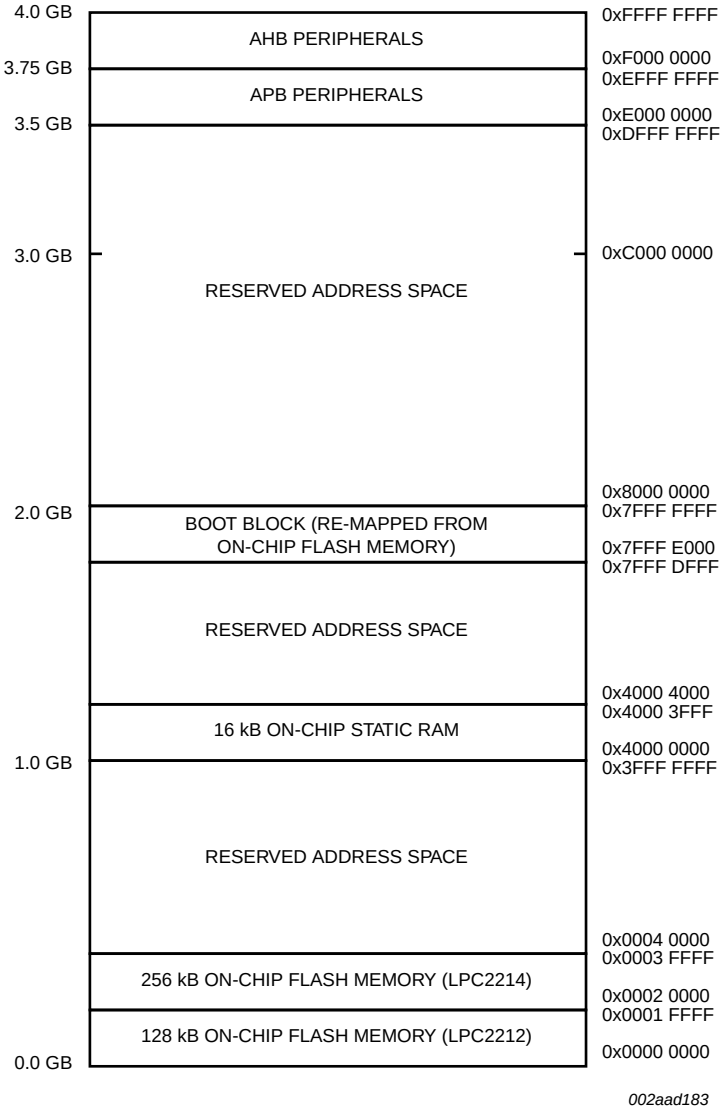


Fig 3. LPC2212/2214 memory map

6.5 Interrupt controller

The Vectored Interrupt Controller (VIC) accepts all of the interrupt request inputs and categorizes them as Fast Interrupt reQuest (FIQ), vectored Interrupt ReQuest (IRQ), and non-vectored IRQ as defined by programmable settings. The programmable assignment scheme means that priorities of interrupts from the various peripherals can be dynamically assigned and adjusted.

The FIQ has the highest priority. If more than one request is assigned to FIQ, the VIC combines the requests to produce the FIQ signal to the ARM processor. The fastest possible FIQ latency is achieved when only one request is classified as FIQ, because then the FIQ service routine can simply start dealing with that device. But if more than one request is assigned to the FIQ class, the FIQ service routine can read a word from the VIC that identifies which FIQ source(s) is (are) requesting an interrupt.

Vectored IRQs have the middle priority. Sixteen of the interrupt requests can be assigned to this category. Any of the interrupt requests can be assigned to any of the 16 vectored IRQ slots, among which slot 0 has the highest priority and slot 15 has the lowest.

Non-vectored IRQs have the lowest priority.

The VIC combines the requests from all the vectored and non-vectored IRQs to produce the IRQ signal to the ARM processor. The IRQ service routine can start by reading a register from the VIC and jumping there. If any of the vectored IRQs are requesting, the VIC provides the address of the highest-priority requesting IRQs service routine, otherwise it provides the address of a default routine that is shared by all the non-vectored IRQs. The default routine can read another VIC register to see what IRQs are active.

6.5.1 Interrupt sources

Table 4 lists the interrupt sources for each peripheral function. Each peripheral device has one interrupt line connected to the Vectored Interrupt Controller, but may have several internal interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Table 4. Interrupt sources

Block	Flag(s)	VIC channel #
WDT	Watchdog Interrupt (WDINT)	0
-	Reserved for software interrupts only	1
ARM Core	EmbeddedICE, DbgCommRx	2
ARM Core	EmbeddedICE, DbgCommTx	3
Timer 0	Match 0 to 3 (MR0, MR1, MR2, MR3)	4
Timer 1	Match 0 to 3 (MR0, MR1, MR2, MR3)	5
UART0	Rx Line Status (RLS) Transmit Holding Register empty (THRE) Rx Data Available (RDA) Character Time-out Indicator (CTI)	6
UART1	Rx Line Status (RLS) Transmit Holding Register empty (THRE) Rx Data Available (RDA) Character Time-out Indicator (CTI) Modem Status Interrupt (MSI)	7
PWM0	Match 0 to 6 (MR0, MR1, MR2, MR3, MR4, MR5, MR6)	8
I^2C-bus	SI (state change)	9
SPI0	SPIF, MODF	10
SPI1 and SSP[1]	SPIF, MODF and TXRIS, RXRIS, RTRIS, RORRIS	11
PLL	PLL Lock (PLOCK)	12
RTC	RTCCIF (Counter Increment), RTCALF (Alarm)	13
System Control	External Interrupt 0 (EINT0)	14
	External Interrupt 1 (EINT1)	15
	External Interrupt 2 (EINT2)	16
	External Interrupt 3 (EINT3)	17
ADC	ADC	18

- Toggle on match.
- Do nothing on match.

6.14.2 Features available in LPC2212/2214/01 only

The LPC2212/2214/01 can count external events on one of the capture inputs if the external pulse lasts at least one half of the period of the PCLK. In this configuration, unused capture lines can be selected as regular timer capture inputs, or used as external interrupts.

- Timer can count cycles of either the peripheral clock (PCLK) or an externally supplied clock.
- When counting cycles of an externally supplied clock, only one of the timer's capture inputs can be selected as the timer's clock. The rate of such a clock is limited to PCLK / 4. Duration of high/low levels on the selected CAP input cannot be shorter than 1 / (2PCLK).

6.15 Watchdog timer

The purpose of the Watchdog is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, the Watchdog will generate a system reset if the user program fails to 'feed' (or reload) the Watchdog within a predetermined amount of time.

6.15.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect/incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 32-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(PCLK)} \times 256 \times 4$) to ($T_{cy(PCLK)} \times 2^{32} \times 4$) in multiples of $T_{cy(PCLK)} \times 4$.

6.16 Real-time clock

The RTC is designed to provide a set of counters to measure time when normal or idle operating mode is selected. The RTC has been designed to use little power, making it suitable for battery powered systems where the CPU is not running continuously (Idle mode).

6.16.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra low power design to support battery powered systems.

6.18.6 Memory mapping control

The Memory Mapping Control alters the mapping of the interrupt vectors that appear beginning at address 0x0000 0000. Vectors may be mapped to the bottom of the on-chip flash memory, or to the on-chip static RAM. This allows code running in different memory spaces to have control of the interrupts.

6.18.7 Power control

The LPC2212/2214 support two reduced power modes: Idle mode and Power-down mode. In Idle mode, execution of instructions is suspended until either a Reset or interrupt occurs. Peripheral functions continue operation during Idle mode and may generate interrupts to cause the processor to resume execution. Idle mode eliminates power used by the processor itself, memory systems and related controllers, and internal buses.

In Power-down mode, the oscillator is shut down and the chip receives no internal clocks. The processor state and registers, peripheral registers, and internal SRAM values are preserved throughout Power-down mode and the logic levels of chip output pins remain static. The Power-down mode can be terminated and normal operation resumed by either a Reset or certain specific interrupts that are able to function without clocks. Since all dynamic operation of the chip is suspended, Power-down mode reduces chip power consumption to nearly zero.

A Power Control for Peripherals feature allows individual peripherals to be turned off if they are not needed in the application, resulting in additional power savings.

6.18.8 APB

The APB divider determines the relationship between the processor clock (CCLK) and the clock used by peripheral devices (PCLK). The APB divider serves two purposes. The first is to provide peripherals with the desired PCLK via APB so that they can operate at the speed chosen for the ARM processor. In order to achieve this, the APB may be slowed down to $\frac{1}{2}$ to $\frac{1}{4}$ of the processor clock rate. Because the APB bus must work properly at power-up (and its timing cannot be altered if it does not work since the APB divider control registers reside on the APB), the default condition at reset is for the APB to run at $\frac{1}{4}$ of the processor clock rate. The second purpose of the APB divider is to allow power savings when an application does not require any peripherals to run at the full processor rate. Because the APB divider is connected to the PLL output, the PLL remains active (if it was running) during Idle mode.

6.19 Emulation and debugging

The LPC2212/2214 support emulation and debugging via a JTAG serial port. A trace port allows tracing program execution. Debugging and trace functions are multiplexed only with GPIOs on Port 1. This means that all communication, timer and interface peripherals residing on Port 0 are available during the development and debugging phase as they are when the application is run in the embedded system itself.

6.19.1 EmbeddedICE

Standard ARM EmbeddedICE logic provides on-chip debug support. The debugging of the target system requires a host computer running the debugger software and an EmbeddedICE protocol convertor. EmbeddedICE protocol convertor converts the Remote Debug Protocol commands to the JTAG data needed to access the ARM core.

8. Static characteristics

Table 6. Static characteristics

T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$V_{DD(1V8)}$	supply voltage (1.8 V)		[2]	1.65	1.8	1.95	V
$V_{DD(3V3)}$	supply voltage (3.3 V)		[3]	3.0	3.3	3.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)			2.5	3.3	3.6	V
Standard port pins, $\overline{\text{RESET}}$, RTCK							
I_{IL}	LOW-level input current	V_I = 0 V; no pull-up		-	-	3	μA
I_{IH}	HIGH-level input current	$V_I = V_{DD(3V3)}$; no pull-down		-	-	3	μA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD(3V3)}$; no pull-up/down		-	-	3	μA
I_{latch}	I/O latch-up current	$-(0.5V_{DD(3V3)}) < V_I < (1.5V_{DD(3V3)})$; T_j < 125 °C		100	-	-	mA
V_I	input voltage		[4][5][6]	0	-	5.5	V
V_O	output voltage	output active		0	-	$V_{DD(3V3)}$	V
V_{IH}	HIGH-level input voltage			2.0	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.8	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA	[7]	$V_{DD(3V3)} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	[7]	-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(3V3)} - 0.4$ V	[7]	−4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	[7]	4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[8]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD(3V3)}$	[8]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	[9]	10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V	[10]	−15	−50	−85	μA
		$V_{DD(3V3)} < V_I$ < 5 V	[9]	0	0	0	μA

Table 6. Static characteristics *…continued*

T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Power consumption LPC2212, LPC2212/00, LPC2214, LPC2214/00							
$I_{DD(act)}$	active mode supply current	$V_{DD(1V8)}$ = 1.8 V; CCLK = 60 MHz; T_{amb} = 25 °C; code `while(1){}` executed from flash; all peripherals enabled via PCONP[11] register but not configured to run		-	60	-	mA
$I_{DD(pd)}$	Power-down mode supply current	$V_{DD(1V8)}$ = 1.8 V; T_{amb} = 25 °C		-	10	-	μA
		$V_{DD(1V8)}$ = 1.8 V; T_{amb} = 85 °C		-	110	500	μA
Power consumption LPC2212/01 and LPC2214/01							
$I_{DD(act)}$	active mode supply current	$V_{DD(1V8)}$ = 1.8 V; CCLK = 60 MHz; T_{amb} = 25 °C; code `while(1){}` executed from flash; all peripherals enabled via PCONP[11] register but not configured to run		-	41	-	mA
$I_{DD(idle)}$	Idle mode supply current	$V_{DD(1V8)}$ = 1.8 V; CCLK = 60 MHz; T_{amb} = 25 °C; executed from flash; all peripherals enabled via PCONP[11] register but not configured to run		-	6.5	-	mA
$I_{DD(pd)}$	Power-down mode supply current	$V_{DD(1V8)}$ = 1.8 V; T_{amb} = 25 °C		-	10	-	μA
		$V_{DD(1V8)}$ = 1.8 V; T_{amb} = 85 °C		-	110	500	μA
I^2C-bus pins							
V_{IH}	HIGH-level input voltage			$0.7V_{DD(3V3)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(3V3)}$	V
V_{hys}	hysteresis voltage			-	$0.05V_{DD(3V3)}$	-	V
V_{OL}	LOW-level output voltage	I_{OLS} = 3 mA	[7]	-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{DD(3V3)}$	[12]	-	2	4	μA
		V_I = 5 V		-	10	22	μA

Table 6. Static characteristics *…continued*

T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
Oscillator pins						
$V_{i(XTAL1)}$	input voltage on pin XTAL1		0	-	1.8	V
$V_{o(XTAL2)}$	output voltage on pin XTAL2		0	-	1.8	V

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] Internal rail.

[3] External rail.

[4] Including voltage on outputs in 3-state mode.

[5] $V_{DD(3V3)}$ supply voltages must be present.

[6] 3-state outputs go into 3-state mode when $V_{DD(3V3)}$ is grounded.

[7] Accounts for 100 mV voltage drop in all supply lines.

[8] Only allowed for a short time period.

[9] Minimum condition for V_I = 4.5 V, maximum condition for V_I = 5.5 V.

[10] Applies to P1[25:16].

[11] See the *LPC2114/2124/2212/2214 User Manual*.

[12] To V_{SS}.

9. Dynamic characteristics

Table 9. Dynamic characteristics

T_{amb} = −40 °C to +85 °C for industrial applications; $V_{DD(1V8)}$, $V_{DD(3V3)}$ over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
External clock						
f_{osc}	oscillator frequency	supplied by an external oscillator (signal generator)	1	-	50	MHz
		external clock frequency supplied by an external crystal oscillator	1	-	30	MHz
		external clock frequency if on-chip PLL is used	10	-	25	MHz
		external clock frequency if on-chip bootloader is used for initial code download	10	-	25	MHz
$T_{cy(clk)}$	clock cycle time		20	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns
Port pins (except P0[2] and P0[3])						
t_r	rise time		-	10	-	ns
t_f	fall time		-	10	-	ns
I^2C-bus pins (P0[2] and P0[3])						
t_f	fall time	V_{IH} to V_{IL}	[2] $20 + 0.1 \times C_b$	-	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Bus capacitance C_b in pF, from 10 pF to 400 pF.

Table 10. External memory interface dynamic characteristics *…continued*
C_L = 25 pF; T_{amb} = 40 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{BLSHDNV}$	BLS HIGH to data invalid time		[2]	$(2 \times T_{cy(CCLK)}) - 5$	-	$(2 \times T_{cy(CCLK)}) + 5$	ns
t_{CHDV}	XCLK HIGH to data valid time			-	-	10	ns
t_{CHWEL}	XCLK HIGH to WE LOW time			-	-	10	ns
t_{CHBLSL}	XCLK HIGH to BLS LOW time			-	-	10	ns
t_{CHWEH}	XCLK HIGH to WE HIGH time			-	-	10	ns
t_{CHBLSH}	XCLK HIGH to BLS HIGH time			-	-	10	ns
t_{CHDNV}	XCLK HIGH to data invalid time			-	-	10	ns

[1] Except on initial access, in which case the address is set up $T_{cy(CCLK)}$ earlier.

[2] $T_{cy(CCLK)} = 1/CCLK$.

[3] Latest of address valid, CS LOW, OE LOW to data valid.

[4] Address valid to data valid.

[5] Earliest of CS HIGH, OE HIGH, address change to data invalid.

Table 11. Standard read access specifications

Access cycle	Max frequency	WST[1] setting WST ≥ 0; round up to integer	Memory access time requirement
standard read	$f_{MAX} \leq \frac{2 + WST1}{t_{RAM} + 20\ ns}$	$WST1 \geq \frac{t_{RAM} + 20\ ns}{t_{cy(CCLK)}} - 2$	$t_{RAM} \leq t_{cy(CCLK)} \times (2 + WST1) - 20\ ns$
standard write	$f_{MAX} \leq \frac{1 + WST2}{t_{WRITE} + 5\ ns}$	$WST2 \geq \frac{t_{WRITE} - t_{CYC} + 5}{t_{cy(CCLK)}}$	$t_{WRITE} \leq t_{cy(CCLK)} \times (1 + WST2) - 5\ ns$
burst read - initial	$f_{MAX} \leq \frac{2 + WST1}{t_{INIT} + 20\ ns}$	$WST1 \geq \frac{t_{INIT} + 20\ ns}{t_{cy(CCLK)}} - 2$	$t_{INIT} \leq t_{cy(CCLK)} \times (2 + WST1) - 20\ ns$
burst read - subsequent 3×	$f_{MAX} \leq \frac{1}{t_{ROM} + 20\ ns}$	N/A	$t_{ROM} \leq t_{cy(CCLK)} - 20\ ns$

[1] See the *LPC2114/2124/2212/2214 User Manual* for a description of the WSTn bits.

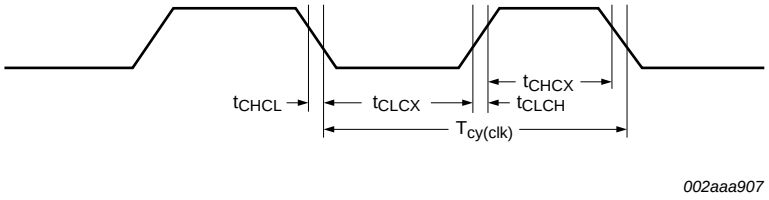


Fig 16. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

11. Abbreviations

Table 12. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
CPU	Central Processing Unit
DCC	Debug Communications Channel
EMC	External Memory Controller
FIFO	First In, First Out
GPIO	General Purpose Input/Output
JTAG	Joint Test Action Group
PLL	Phase-Locked Loop
POR	Power-On Reset
PWM	Pulse Width Modulator
RAM	Random Access Memory
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SSI	Synchronous Serial Interface
SSP	Synchronous Serial Port
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter

12. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC2212_2214 v.5	20110614	Product data sheet	201004021F	LPC2212_2214 v.4
Modifications:	• Table 6 “Static characteristics”; Changed /01 Power-down mode supply current ($I_{DD(pd)}$) from 180 μA to 500 μA for industrial temperature range. • Table 6 “Static characteristics”; Moved V_{hys} voltage from typical to minimum. • Table 6 “Static characteristics”; Changed I^2C pad hysteresis from $0.5V_{DD(3V3)}$ to $0.05V_{DD(3V3)}$.			
LPC2212_2214 v.4	20080103	Product data sheet	-	LPC2212_2214 v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Type number LPC2212FBD144/01 has been added. • Type number LPC2214FBD144/01 has been added. • Details introduced with /01 devices on new peripherals/features (Fast I/O Ports, SSP, CRP) and enhancements to existing ones (UART0/1, Timers, ADC, and SPI) added. • Power consumption measurements for LPC2212/01 and LPC2214/01 added. • Description of JTAG pin TCK has been updated.			
LPC2212_2214 v.3	20060719	Product data sheet	-	LPC2212_2214 v.2
LPC2212_2214 v.2	20041223	Product data	-	LPC2212_2214 v.1
LPC2212_2214 v.1	20040202	Preliminary data	-	-