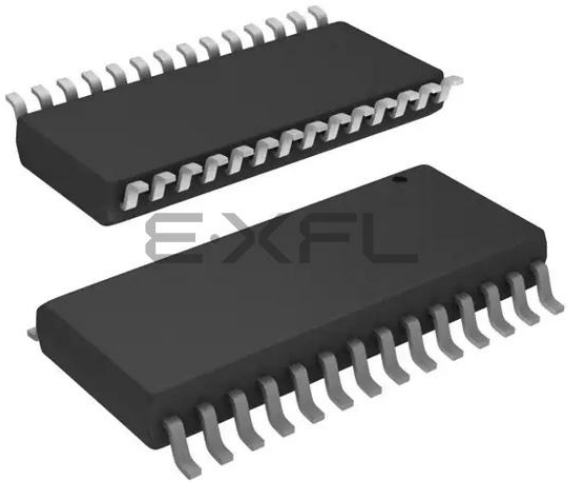

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 24x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f18855-e-so

TABLE 1-3: PIC16F18875 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RB2/ANB2/SDA2(3,4)/SDI2(1)/ CWG3IN(1)/IOCB2	RB2	TTL/ST	CMOS/OD	General purpose I/O.
	ANB2	AN	—	ADC Channel B2 input.
	SDA2(3,4)	I^2C/SMBus	OD	MSSP2 I^2C serial data input/output.
	SDI2(1)	TTL/ST	—	MSSP2 SPI serial data input.
	CWG3IN(1)	TTL/ST	—	Complementary Waveform Generator 3 input.
	IOCB2	TTL/ST	—	Interrupt-on-change input.
RB3/ANB3/C1IN2-/C2IN2-/IOCB3	RB3	TTL/ST	CMOS/OD	General purpose I/O.
	ANB3	AN	—	ADC Channel B3 input.
	C1IN2-	AN	—	Comparator negative input.
	C2IN2-	AN	—	Comparator negative input.
	IOCB3	TTL/ST	—	Interrupt-on-change input.
RB4/ANB4/ADCACT(1)/T5G(1)/ SMTWIN2(1)/IOCB4	RB4	TTL/ST	CMOS/OD	General purpose I/O.
	ANB4	AN	—	ADC Channel B4 input.
	ADCACT(1)	TTL/ST	—	ADC Auto-Conversion Trigger input.
	T5G(1)	TTL/ST	—	Timer5 gate input.
	SMTWIN2(1)	TTL/ST	—	Signal Measurement Timer2 (SMT2) window input.
	IOCB4	TTL/ST	—	Interrupt-on-change input.
RB5/ANB5/T1G(1)/SMTSIG2(1)/ CCP3(1)/IOCB5	RB5	TTL/ST	CMOS/OD	General purpose I/O.
	ANB5	AN	—	ADC Channel B5 input.
	T1G(1)	TTL/ST	—	Timer1 gate input.
	SMTSIG2(1)	TTL/ST	—	Signal Measurement Timer2 (SMT2) signal input.
	CCP3(1)	TTL/ST	CMOS/OD	Capture/compare/PWM3 (default input location for capture function).
	IOCB5	TTL/ST	—	Interrupt-on-change input.
RB6/ANB6/CLCIN2(1)/IOCB6/ ICSPCLK	RB6	TTL/ST	CMOS/OD	General purpose I/O.
	ANB6	AN	—	ADC Channel B6 input.
	CLCIN2(1)	TTL/ST	—	Configurable Logic Cell source input.
	IOCB6	TTL/ST	—	Interrupt-on-change input.
	ICSPCLK	ST	—	In-Circuit Serial Programming™ and debugging clock input.
RB7/ANB7/DAC1OUT2/T6IN(1)/ CLCIN3(1)/IOCB7/ICSPDAT	RB7	TTL/ST	CMOS/OD	General purpose I/O.
	ANB7	AN	—	ADC Channel B7 input.
	DAC1OUT2	—	AN	Digital-to-Analog Converter output.
	T6IN(1)	TTL/ST	—	Timer6 external digital clock input.
	CLCIN3(1)	TTL/ST	—	Configurable Logic Cell source input.
	IOCB7	TTL/ST	—	Interrupt-on-change input.
	ICSPDAT	ST	CMOS	In-Circuit Serial Programming™ and debugging data input/ output.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2CHV= High Voltage XTAL= Crystal levels

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 13-1 for details on which PORT pins may be used for this signal.

2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 13-3.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I^2C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.

TABLE 3-13: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-31

Address	Name	PIC16(L)F18855	PIC16(L)F18875	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Bank 0													
CPU CORE REGISTERS; see Table 3-2 for specifics													
00Ch	PORTA			RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	xxxx xxxx	xxxx xxxx
00Dh	PORTB			RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	xxxx xxxx
00Eh	PORTC			RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	xxxx xxxx
00Fh	PORTD	X	—	Unimplemented								---- ----	---- ----
		—	X	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx xxxx	xxxx xxxx
010h	PORTE	X	—	—	—	—	—	RE3	—	—	—	---- x---	---- x---
		—	X	—	—	—	—	RE3	RE2	RE1	RE0	---- xxxx	---- xxxx
011h	TRISA			TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1111 1111	1111 1111
012h	TRISB			TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111	1111 1111
013h	TRISC			TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	1111 1111	1111 1111
014h	TRISD	X	—	Unimplemented								---- ----	---- ----
		—	X	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	1111 1111	1111 1111
015h	TRISE	X	—	Unimplemented								---- ----	---- ----
		—	X	—	—	—	—	—	TRISE2	TRISE1	TRISE0	---- -111	---- -111
016h	LATA			LATA7	LATA6	LATA5	LATA4	LATA3	LATA2	LATA1	LATA0	xxxx xxxx	uuuu uuuu
017h	LATB			LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	xxxx xxxx	uuuu uuuu
018h	LATC			LATC7	LATC6	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0	xxxx xxxx	uuuu uuuu
019h	LATD	X	—	Unimplemented								---- ----	---- ----
		—	X	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	xxxx xxxx	uuuu uuuu
01Ah	LATE	X	-	Unimplemented								---- ----	---- ----
		—	X	—	—	—	—	—	LATE2	LATE1	LATE0	---- -xxx	---- -uuu

Legend: x = unknown, u = unchanged, q =depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Register present on PIC16F18855/75 devices only.

2: Unimplemented, read as '1'.

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6.3 Clock Switching

The system clock source can be switched between external and internal clock sources via software using the New Oscillator Source (NOSC) and New Divider selection request (NDIV) bits of the OSCCON1 register. The following clock sources can be selected using the following:

- External oscillator
- Internal Oscillator Block (INTOSC)

6.3.1 NEW OSCILLATOR SOURCE (NOSC) AND NEW DIVIDER SELECTION REQUEST (NDIV) BITS

The New Oscillator Source (NOSC) and New Divider selection request (NDIV) bits of the OSCCON1 register select the system clock source that is used for the CPU and peripherals.

When new values of NOSC and NDIV are written to OSCCON1, the current oscillator selection will continue to operate while waiting for the new clock source to indicate that it is stable and ready. In some cases, the newly requested source may already be in use, and is ready immediately. In the case of a divider-only change, the new and old sources are the same, so the old source will be ready immediately. The device may enter Sleep while waiting for the switch as described in Section 6.3.3, Clock Switch and Sleep.

When the new oscillator is ready, the New Oscillator is Ready (NOSCR) bit of OSCCON3 and the Clock Switch Interrupt Flag (CSWIF) bit of PIR1 become set (CSWIF = 1). If Clock Switch Interrupts are enabled (CLKSIE = 1), an interrupt will be generated at that time. The Oscillator Ready (ORDY) bit of OSCCON3 can also be polled to determine when the oscillator is ready in lieu of an interrupt.

If the Clock Switch Hold (CSWHOLD) bit of OSCCON3 is clear, the oscillator switch will occur when the New Oscillator is ready bit (NOSCR) is set, and the interrupt (if enabled) will be serviced at the new oscillator setting.

If CSWHOLD is set, the oscillator switch is suspended, while execution continues using the current (old) clock source. When the NOSCR bit is set, software should:

- Set CSWHOLD = 0 so the switch can complete, or
- Copy COSC into NOSC to abandon the switch.

If DOZE is in effect, the switch occurs on the next clock cycle, whether or not the CPU is operating during that cycle.

Changing the clock post-divider without changing the clock source (i.e., changing FOSC from 1 MHz to 2 MHz) is handled in the same manner as a clock source change, as described previously. The clock source will already be active, so the switch is relatively quick. CSWHOLD must be clear (CSWHOLD = 0) for the switch to complete.

The current COSC and CDIV are indicated in the OSCCON2 register up to the moment when the switch actually occurs, at which time OSCCON2 is updated and ORDY is set. NOSCR is cleared by hardware to indicate that the switch is complete.

6.3.2 PLL INPUT SWITCH

Switching between the PLL and any non-PLL source is managed as described above. The input to the PLL is established when NOSC selects the PLL, and maintained by the COSC setting.

When NOSC and COSC select the PLL with different input sources, the system continues to run using the COSC setting, and the new source is enabled per NOSC. When the new oscillator is ready (and CSWHOLD = 0), system operation is suspended while the PLL input is switched and the PLL acquires lock.

Note:	If the PLL fails to lock, the FSCM will trigger.

6.3.3 CLOCK SWITCH AND SLEEP

If OSCCON1 is written with a new value and the device is put to Sleep before the switch completes, the switch will not take place and the device will enter Sleep mode.

When the device wakes from Sleep and the CSWHOLD bit is clear, the device will wake with the ‘new’ clock active, and the clock switch interrupt flag bit (CSWIF) will be set.

When the device wakes from Sleep and the CSWHOLD bit is set, the device will wake with the ‘old’ clock active and the new clock will be requested again.

7.0 INTERRUPTS

The interrupt feature allows certain events to preempt normal program flow. Firmware is used to determine the source of the interrupt and act accordingly. Some interrupts can be configured to wake the MCU from Sleep mode.

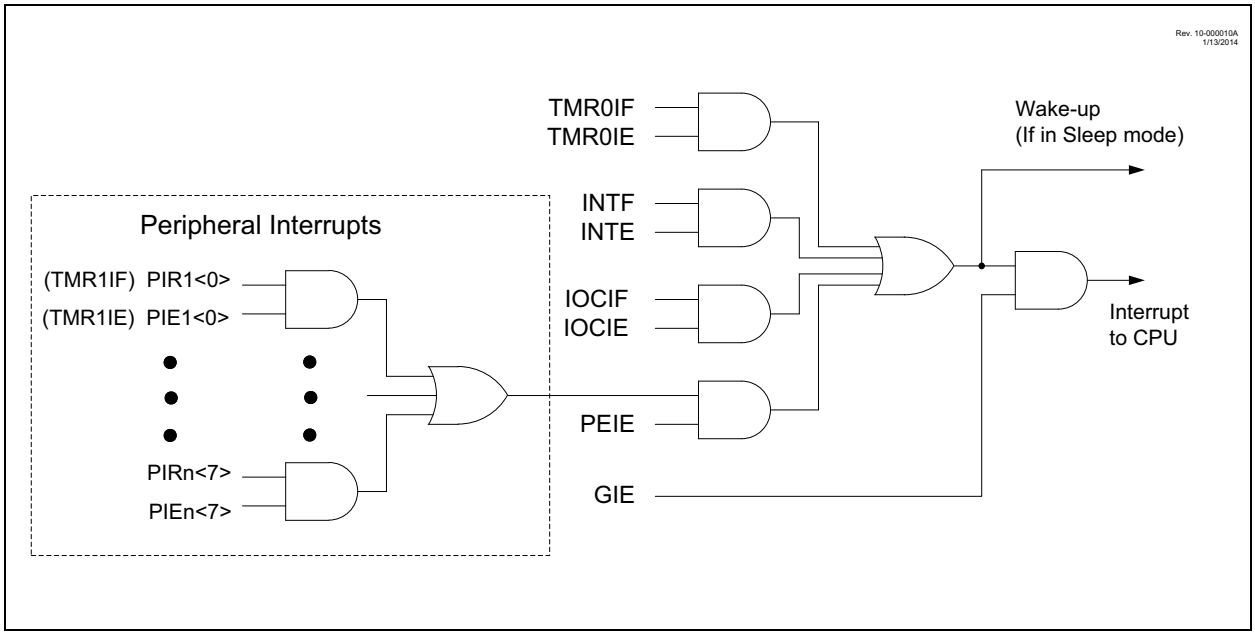
This chapter contains the following information for Interrupts:

- Operation
- Interrupt Latency
- Interrupts During Sleep
- INT Pin
- Automatic Context Saving

Many peripherals produce interrupts. Refer to the corresponding chapters for details.

A block diagram of the interrupt logic is shown in Figure 7-1.

FIGURE 7-1: INTERRUPT LOGIC



10.4.3 NVMREG WRITE TO EEPROM

Writing to the EEPROM is accomplished by the following steps:

1. Set the NVMREGS and WREN bits of the NVMCON1 register.
2. Write the desired address (address + F000h) into the NVMADRH:NVMADRL register pair (Table 10-2).
3. Perform the unlock sequence as described in **Section 10.4.2 "NVM Unlock Sequence"**.

A single EEPROM word is written with NVMDATA. The operation includes an implicit erase cycle for that word (it is not necessary to set the FREE bit), and requires many instruction cycles to finish. CPU execution continues in parallel and, when complete, WR is cleared by hardware, NVMIF is set, and an interrupt will occur if NVMIE is also set. Software must poll the WR bit to determine when writing is complete, or wait for the interrupt to occur. WREN will remain unchanged.

Once the EEPROM write operation begins, clearing the WR bit will have no effect; the operation will continue to run to completion.

10.4.4 NVMREG ERASE OF PFM

Before writing to PFM, the word(s) to be written must be erased or previously unwritten. PFM can only be erased one row at a time. No automatic erase occurs upon the initiation of the write to PFM.

To erase a PFM row:

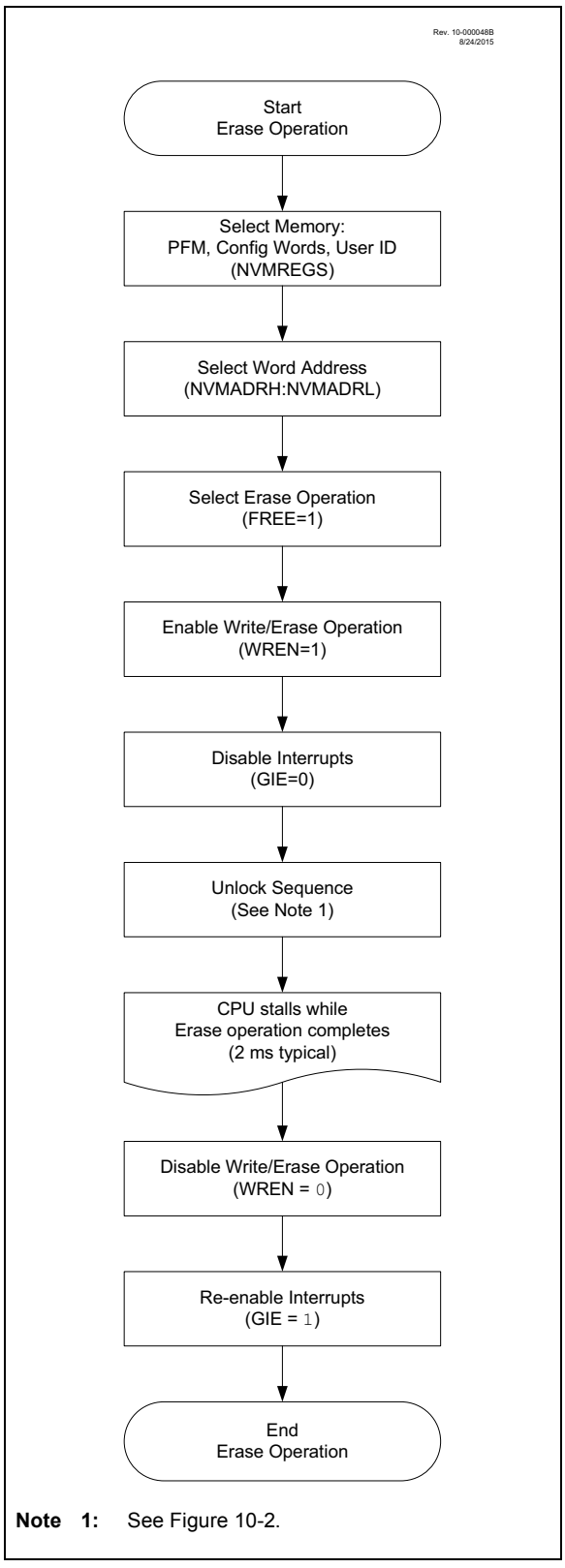
1. Clear the NVMREGS bit of the NVMCON1 register to erase PFM locations, or set the NMVREGS bit to erase User ID locations.
2. Write the desired address into the NVMADRH:NVMADRL register pair (Table 10-2).
3. Set the FREE and WREN bits of the NVMCON1 register.
4. Perform the unlock sequence as described in **Section 10.4.2 "NVM Unlock Sequence"**.

If the PFM address is write-protected, the WR bit will be cleared and the erase operation will not take place.

While erasing PFM, CPU operation is suspended, and resumes when the operation is complete. Upon completion, the NVMIF is set, and an interrupt will occur if the NVMIE bit is also set.

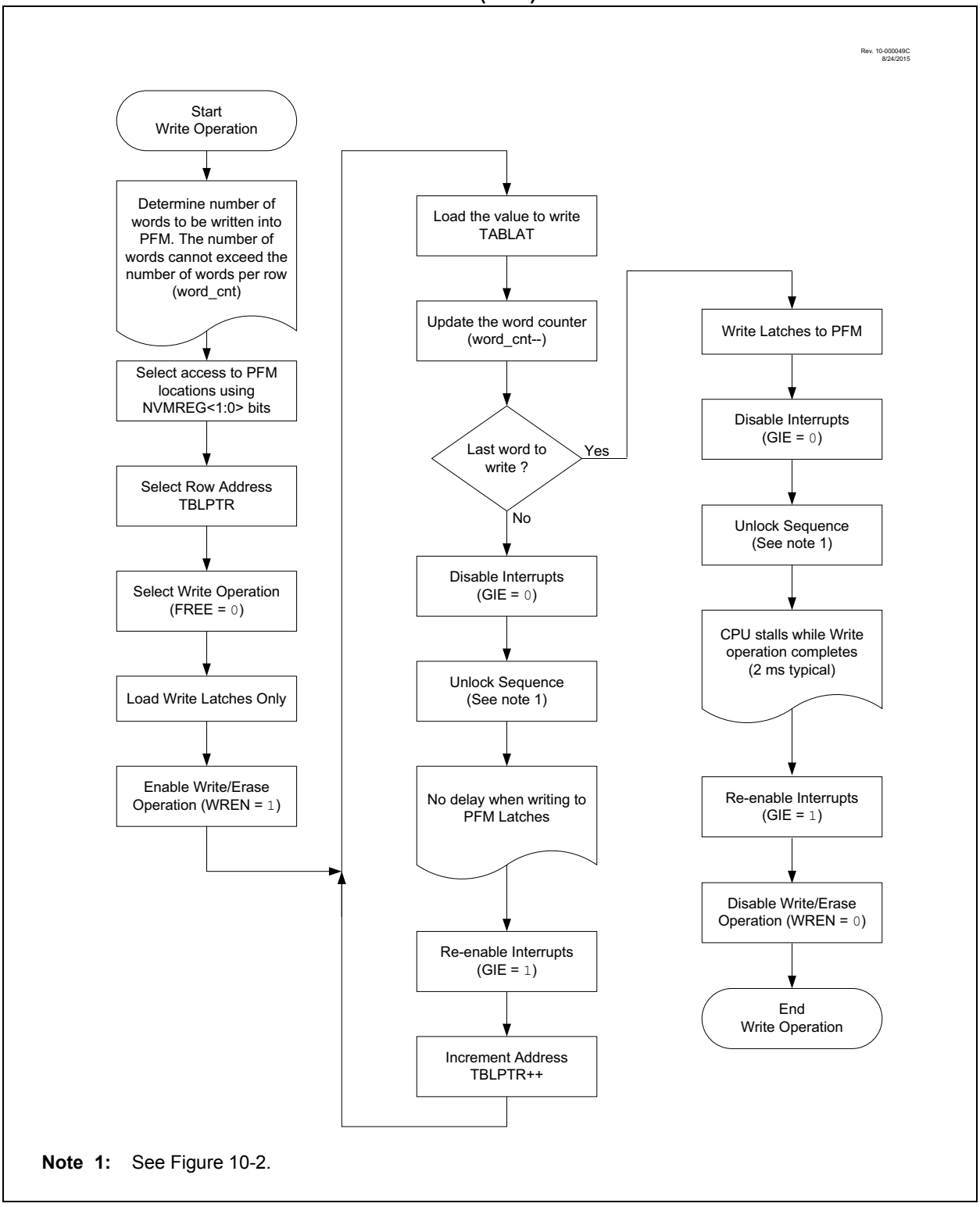
Write latch data is not affected by erase operations, and WREN will remain unchanged.

FIGURE 10-3: NVM ERASE FLOWCHART



Note 1: See Figure 10-2.

FIGURE 10-5: PROGRAM FLASH MEMORY (PFM) WRITE FLOWCHART



Note 1: See Figure 10-2.

REGISTER 12-16: WPUB: WEAK PULL-UP PORTB REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
WPUB7	WPUB6	WPUB5	WPUB4	WPUB3	WPUB2	WPUB1	WPUB0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **WPUB<7:0>**: Weak Pull-up Register bits(1)
1 = Pull-up enabled
0 = Pull-up disabled

Note 1: The weak pull-up device is automatically disabled if the pin is configured as an output.

REGISTER 12-17: ODCONB: PORTB OPEN-DRAIN CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
ODCB7	ODCB6	ODCB5	ODCB4	ODCB3	ODCB2	ODCB1	ODCB0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **ODCB<7:0>:** PORTB Open-Drain Enable bits
For RB<7:0> pins, respectively
1 = Port pin operates as open-drain drive (sink current only)
0 = Port pin operates as standard push-pull drive (source and sink current)

REGISTER 12-27: ODCONC: PORTC OPEN-DRAIN CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
ODCC7	ODCC6	ODCC5	ODCC4	ODCC3	ODCC2	ODCC1	ODCC0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **ODCC<7:0>:** PORTC Open-Drain Enable bits
For RC<7:0> pins, respectively
1 = Port pin operates as open-drain drive (sink current only)
0 = Port pin operates as standard push-pull drive (source and sink current)

REGISTER 12-28: SLRCONC: PORTC SLEW RATE CONTROL REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
SLRC7	SLRC6	SLRC5	SLRC4	SLRC3	SLRC2	SLRC1	SLRC0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **SLRC<7:0>:** PORTC Slew Rate Enable bits
For RC<7:0> pins, respectively
1 = Port pin slew rate is limited
0 = Port pin slews at maximum rate

REGISTER 12-29: INLVLC: PORTC INPUT LEVEL CONTROL REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
INLVLC7	INLVLC6	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **INLVLC<7:0>:** PORTC Input Level Select bits
For RC<7:0> pins, respectively
1 = ST input used for PORT reads and interrupt-on-change
0 = TTL input used for PORT reads and interrupt-on-change

12.11 Register Definitions: PORTD

REGISTER 12-32: PORTD: PORTD REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **RD<7:0>**: PORTD I/O Value bits(1)
1 = Port pin is ≥ VIH
0 = Port pin is ≤ VIL

Note 1: Writes to PORTD are actually written to corresponding LATD register. Reads from PORTD register is return of actual I/O pin values.

REGISTER 12-33: TRISD: PORTD TRI-STATE REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **TRISD<7:0>**: TRISD I/O Value bits
1 = Port pin is ≥ VIH
0 = Port pin is ≤ VIL

TABLE 13-4: SUMMARY OF REGISTERS ASSOCIATED WITH THE PPS MODULE (CONTINUED)

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
RA4PPS	—	—	RA4PPS<5:0>						250
RA5PPS	—	—	RA5PPS<5:0>						250
RA6PPS	—	—	RA6PPS<5:0>						250
RA7PPS	—	—	RA7PPS<5:0>						250
RB0PPS	—	—	RB0PPS<5:0>						250
RB1PPS	—	—	RB1PPS<5:0>						250
RB2PPS	—	—	RB2PPS<5:0>						250
RB3PPS	—	—	RB3PPS<5:0>						250
RB4PPS	—	—	RB4PPS<5:0>						250
RB5PPS	—	—	RB5PPS<5:0>						250
RB6PPS	—	—	RB6PPS<5:0>						250
RB7PPS	—	—	RB7PPS<5:0>						250
RC0PPS	—	—	RC0PPS<5:0>						250
RC1PPS	—	—	RC1PPS<5:0>						250
RC2PPS	—	—	RC2PPS<5:0>						250
RC3PPS	—	—	RC3PPS<5:0>						250
RC4PPS	—	—	RC4PPS<5:0>						250
RC5PPS	—	—	RC5PPS<5:0>						250
RC6PPS	—	—	RC6PPS<5:0>						250
RC7PPS	—	—	RC7PPS<5:0>						250
RD0PPS(1)	—	—	RD0PPS<5:0>						250
RD1PPS(1)	—	—	RD1PPS<5:0>						250
RD2PPS(1)	—	—	RD2PPS<5:0>						250
RD3PPS(1)	—	—	RD3PPS<5:0>						250
RD4PPS(1)	—	—	RD4PPS<5:0>						250
RD5PPS(1)	—	—	RD5PPS<5:0>						250
RD6PPS(1)	—	—	RD6PPS<5:0>						250
RD7PPS(1)	—	—	RD7PPS<5:0>						250
RE0PPS(1)	—	—	RE0PPS<5:0>						250
RE1PPS(1)	—	—	RE1PPS<5:0>						250
RE2PPS(1)	—	—	RE2PPS<5:0>						250

Legend: — = unimplemented, read as '0'. Shaded cells are unused by the PPS module.
Note 1: PIC16F18875 only.

FIGURE 20-1: SIMPLIFIED CWG BLOCK DIAGRAM (HALF-BRIDGE MODE)

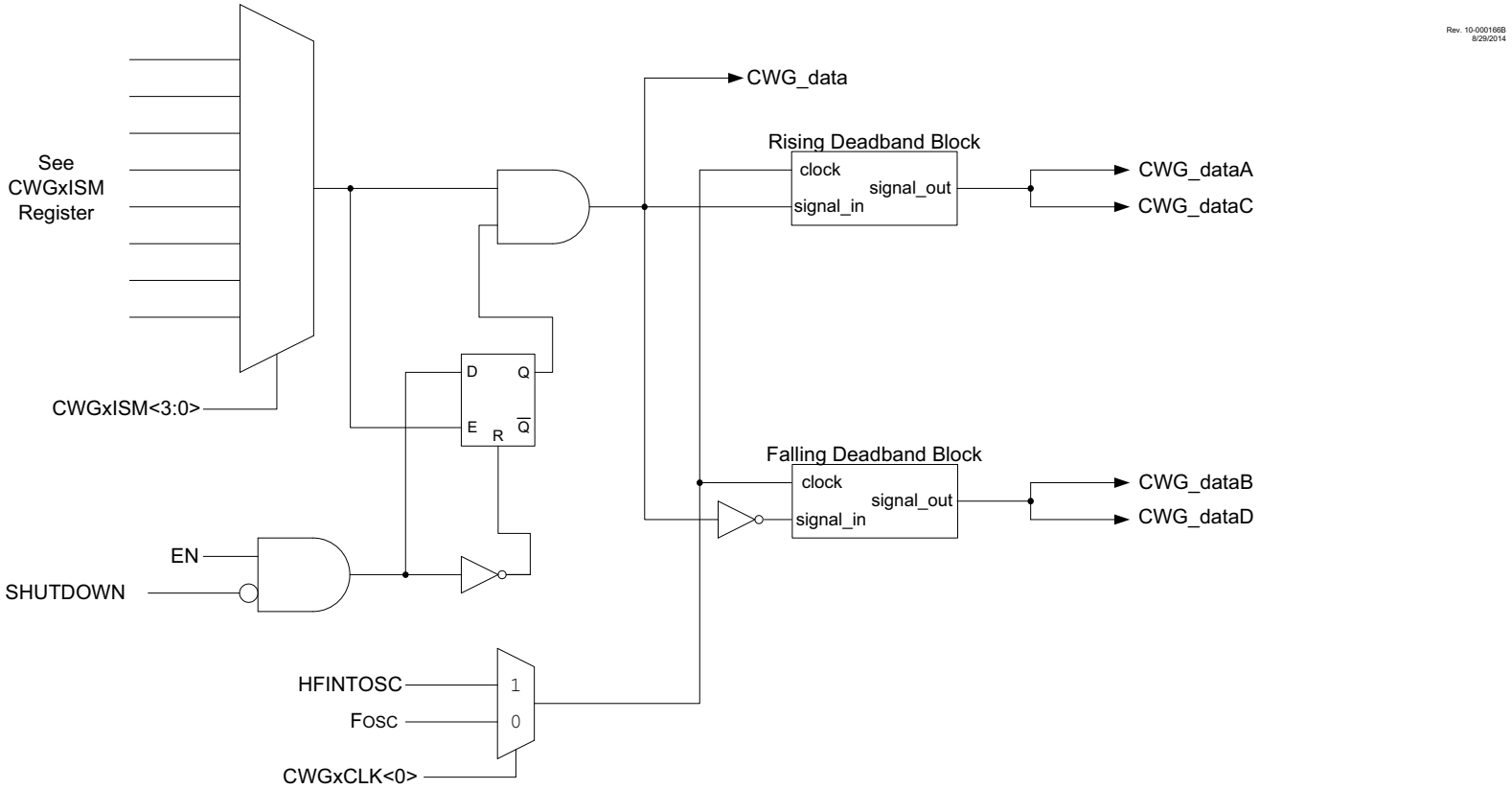


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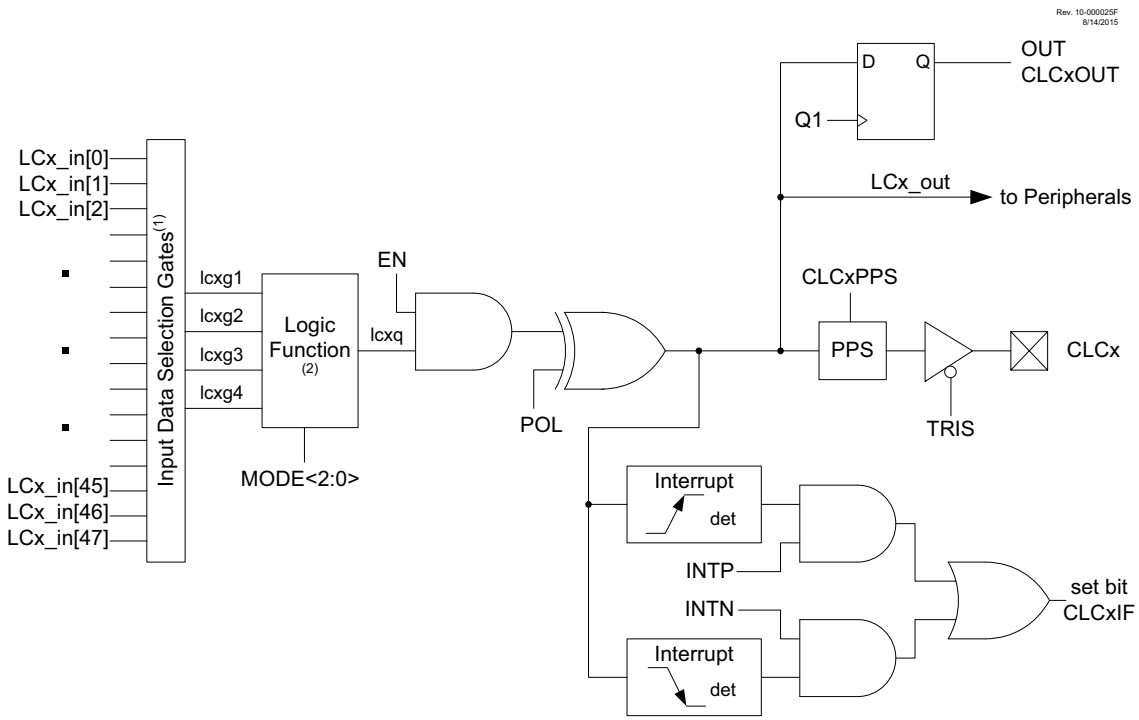
FIGURE 22-1: CLCx SIMPLIFIED BLOCK DIAGRAM



Note 1: See Figure 22-2: Input Data Selection and Gating

2: See Figure 22-3: Programmable Logic Functions.

24.1 NCO OPERATION

The NCO operates by repeatedly adding a fixed value to an accumulator. Additions occur at the input clock rate. The accumulator will overflow with a carry periodically, which is the raw NCO output (NCO_overflow). This effectively reduces the input clock by the ratio of the addition value to the maximum accumulator value. See Equation 24-1.

The NCO output can be further modified by stretching the pulse or toggling a flip-flop. The modified NCO output is then distributed internally to other peripherals and can be optionally output to a pin. The accumulator overflow also generates an interrupt (NCO_overflow).

The NCO period changes in discrete steps to create an average frequency. This output depends on the ability of the receiving circuit (i.e., CWG or external resonant converter circuitry) to average the NCO output to reduce uncertainty.

EQUATION 24-1: NCO OVERFLOW FREQUENCY

$$F_{OVERFLOW} = \frac{NCO\ Clock\ Frequency \times Increment\ Value}{2^{20}}$$

24.1.1 NCO CLOCK SOURCES

Clock sources available to the NCO include:

- HFINTOSC
- FOSC
- LC1_out
- LC2_out
- LC3_out
- LC4_out

The NCO clock source is selected by configuring the N1CKS<2:0> bits in the NCO1CLK register.

24.1.2 ACCUMULATOR

The accumulator is a 20-bit register. Read and write access to the accumulator is available through three registers:

- NCO1ACCL
- NCO1ACCH
- NCO1ACCU

24.1.3 ADDER

The NCO Adder is a full adder, which operates independently from the source clock. The addition of the previous result and the increment value replaces the accumulator value on the rising edge of each input clock.

24.1.4 INCREMENT REGISTERS

The increment value is stored in three registers making up a 20-bit incrementer. In order of LSB to MSB they are:

- NCO1INCL
- NCO1INCH
- NCO1INCU

When the NCO module is enabled, the NCO1INCU and NCO1INCH registers should be written first, then the NCO1INCL register. Writing to the NCO1INCL register initiates the increment buffer registers to be loaded simultaneously on the second rising edge of the NCO_clk signal.

The registers are readable and writable. The increment registers are double-buffered to allow value changes to be made without first disabling the NCO module.

When the NCO module is disabled, the increment buffers are loaded immediately after a write to the increment registers.

Note: The increment buffer registers are not user-accessible.

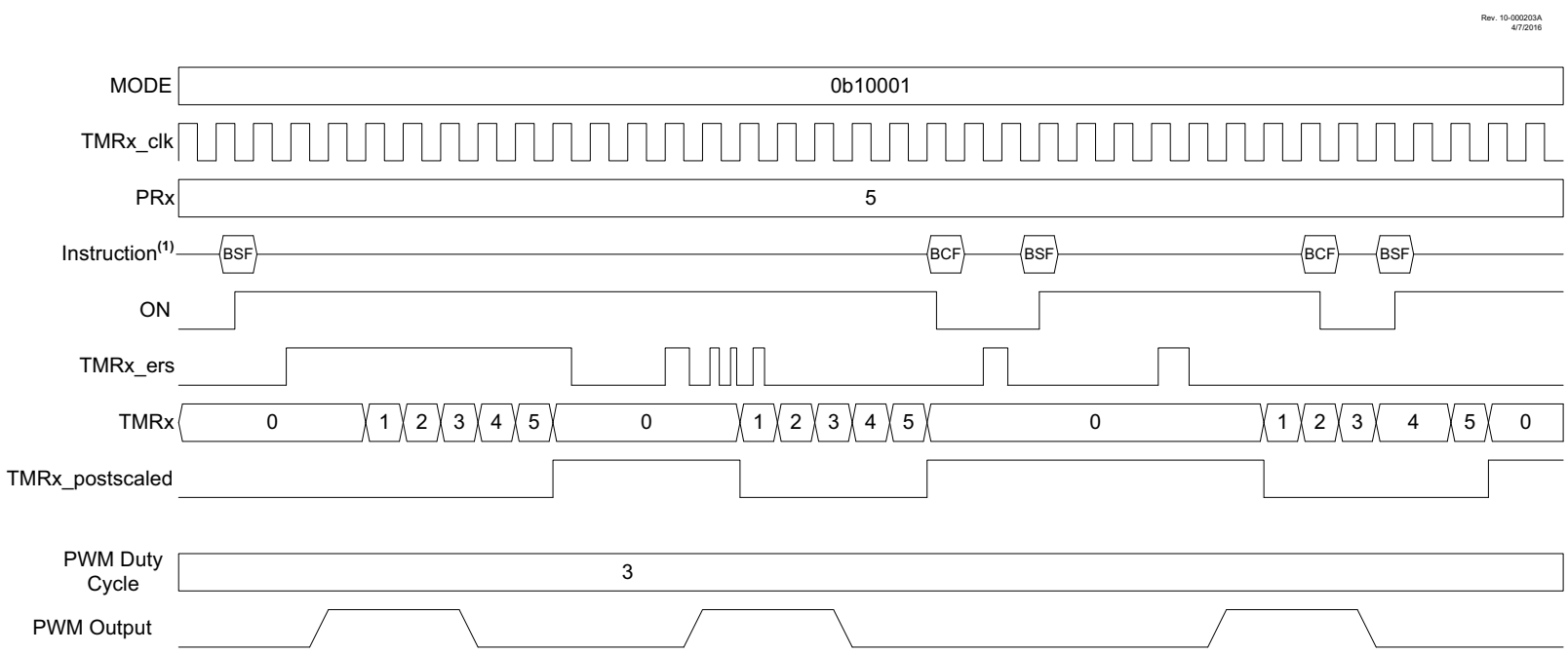
29.5.9 EDGE-TRIGGERED MONOSTABLE MODES

The Edge-Triggered Monostable modes start the timer on an edge from the external Reset signal input, after the ON bit is set, and stop incrementing the timer when the timer matches the PRx period value. The following edges will start the timer:

- Rising edge (MODE<4:0> = 10001)
- Falling edge (MODE<4:0> = 10010)
- Rising or Falling edge (MODE<4:0> = 10011)

When an Edge-Triggered Monostable mode is used in conjunction with the CCP PWM operation the PWM drive goes active with the external Reset signal edge that starts the timer, but will not go active when the timer matches the PRx value. While the timer is incrementing, additional edges on the external Reset signal will not affect the CCP PWM.

FIGURE 29-12: RISING EDGE-TRIGGERED MONOSTABLE MODE TIMING DIAGRAM (MODE = 10001)



Note 1: BSF and BCF represent Bit-Set File and Bit-Clear File instructions executed by the CPU to set or clear the ON bit of TxCON. CPU execution is asynchronous to the timer clock input.

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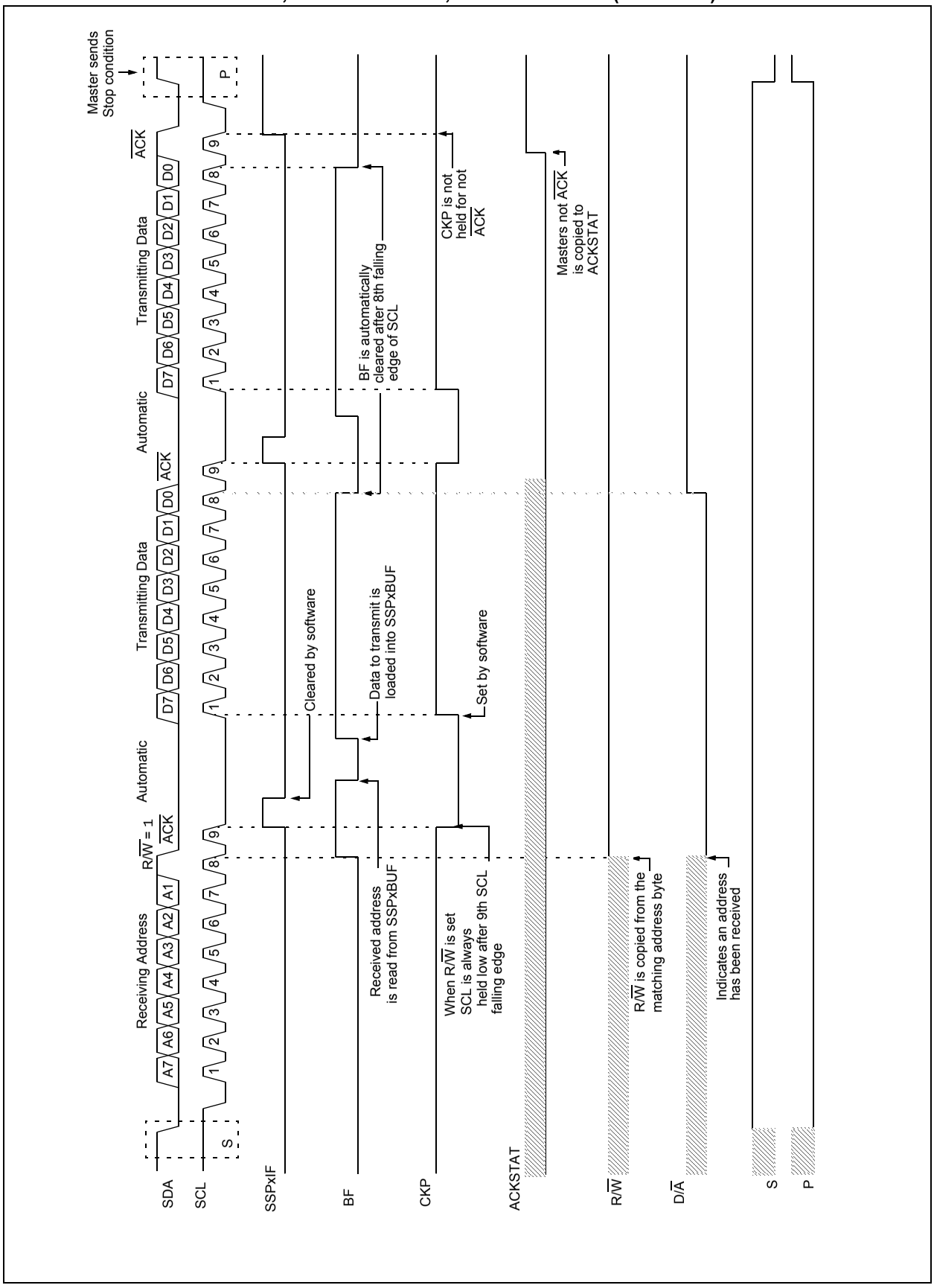
FIGURE 31-18: I²C SLAVE, 7-BIT ADDRESS, TRANSMISSION (AHEN = 0)



32.1 SMT Operation

The core of the module is the 24-bit counter, SMTxTMR combined with a complex data acquisition front-end. Depending on the mode of operation selected, the SMT can perform a variety of measurements summarized in Table 32-1.

32.1.1 CLOCK SOURCES

Clock sources available to the SMT include:

- FOSC
- FOSC/4
- HFINTOSC (16 MHz)
- LFINTOSC
- MFINTOSC/16 (31.25 kHz)

The SMT clock source is selected by configuring the CSEL<2:0> bits in the SMTxCLK register. The clock source can also be prescaled using the PS<1:0> bits of the SMTxCON0 register. The prescaled clock source is used to clock both the counter and any synchronization logic used by the module.

32.1.2 PERIOD MATCH INTERRUPT

Similar to other timers, the SMT triggers an interrupt when SMTxTMR rolls over to '0'. This happens when SMTxTMR = SMTxPR, regardless of mode. Hence, in any mode that relies on an external signal or a window to reset the timer, proper operation requires that SMTxPR be set to a period larger than that of the expected signal or window.

32.2 Basic Timer Function Registers

The SMTxTMR time base and the SMTxCPW/SMTxPR/SMTxCPR buffer registers serve several functions and can be manually updated using software.

32.2.1 TIME BASE

The SMTxTMR is the 24-bit counter that is the center of the SMT. It is used as the basic counter/timer for measurement in each of the modes of the SMT. It can be reset to a value of 24'h00_0000 by setting the RST bit of the SMTxSTAT register. It can be written to and read from software, but it is not guarded for atomic access, therefore reads and writes to the SMTxTMR should only be made when the GO = 0, or the software should have other measures to ensure integrity of SMTxTMR reads/writes.

32.2.2 PULSE WIDTH LATCH REGISTERS

The SMTxCPW registers are the 24-bit SMT pulse width latch. They are used to latch in the value of the SMTxTMR when triggered by various signals, which are determined by the mode the SMT is currently in. The SMTxCPW registers can also be updated with the current value of the SMTxTMR value by setting the CPWUP bit of the SMTxSTAT register.

32.2.3 PERIOD LATCH REGISTERS

The SMTxCPR registers are the 24-bit SMT period latch. They are used to latch in other values of the SMTxTMR when triggered by various other signals, which are determined by the mode the SMT is currently in.

The SMTxCPR registers can also be updated with the current value of the SMTxTMR value by setting the CPRU bit in the SMTxSTAT register.

32.3 Halt Operation

The counter can be prevented from rolling-over using the STP bit in the SMTxCON0 register. When halting is enabled, the period match interrupt persists until the SMTxTMR is reset (either by a manual reset, **Section 32.2.1 "Time Base"**) or by clearing the SMTxGO bit of the SMTxCON1 register and writing the SMTxTMR values in software.

32.4 Polarity Control

The three input signals for the SMT have polarity control to determine whether or not they are active high/positive edge or active low/negative edge signals.

The following bits apply to Polarity Control:

- WSEL bit (Window Polarity)
- SSEL bit (Signal Polarity)
- CSEL bit (Clock Polarity)

These bits are located in the SMTxCON0 register.

32.5 Status Information

The SMT provides input status information for the user without requiring the need to deal with the polarity of the incoming signals.

32.5.1 WINDOW STATUS

Window status is determined by the WS bit of the SMTxSTAT register. This bit is only used in Windowed Measure, Gated Counter and Gated Window Measure modes, and is only valid when TS = 1, and will be delayed in time by synchronizer delays in non-Counter modes.

32.5.2 SIGNAL STATUS

Signal status is determined by the AS bit of the SMTxSTAT register. This bit is used in all modes except Window Measure, Time of Flight and Capture modes, and is only valid when TS = 1, and will be delayed in time by synchronizer delays in non-Counter modes.

REGISTER 32-3: SMTxSTAT: SMT STATUS REGISTER

R/W/HC-0/0	R/W/HC-0/0	R/W/HC-0/0	U-0	U-0	R-0/0	R-0/0	R-0/0
CPRUP	CPWUP	RST	—	—	TS	WS	AS
bit 7							bit 0

Legend:		
HC = Bit is cleared by hardware		HS = Bit is set by hardware
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7 **CPRUP:** SMT Manual Period Buffer Update bit
1 = Request update to SMTxPRx registers
0 = SMTxPRx registers update is complete

bit 6 **CPWUP:** SMT Manual Pulse Width Buffer Update bit
1 = Request update to SMTxCPW registers
0 = SMTxCPW registers update is complete

bit 5 **RST:** SMT Manual Timer Reset bit
1 = Request Reset to SMTxTMR registers
0 = SMTxTMR registers update is complete

bit 4-3 **Unimplemented**: Read as ‘0’

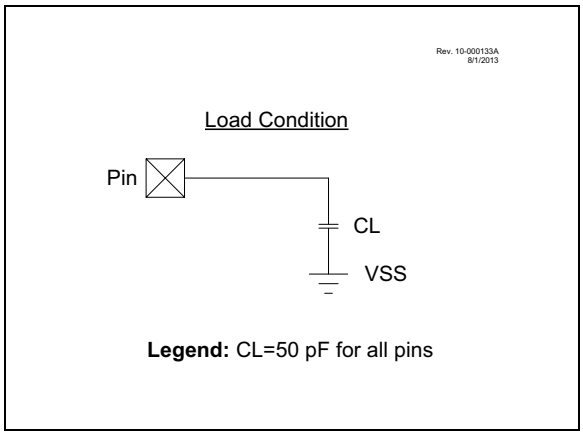
bit 2 **TS:** SMT GO Value Status bit
1 = SMT timer is incrementing
0 = SMT timer is not incrementing

bit 1 **WS:** SMTxWIN Value Status bit
1 = SMT window is open
0 = SMT window is closed

bit 0 **AS:** SMT_signal Value Status bit
1 = SMT acquisition is in progress
0 = SMT acquisition is not in progress

37.4 AC Characteristics

FIGURE 37-4: LOAD CONDITIONS



Note: Unless otherwise noted, VIN = 5V, FOSC = 300 kHz, CIN = 0.1 µF, TA = 25°C.

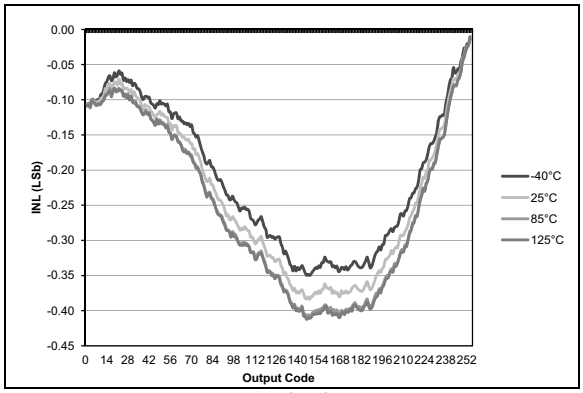


FIGURE 38-73: *Typical DAC INL Error, VDD = 5.0V, VREF = External 5V, PIC16F18855/75 Only.*

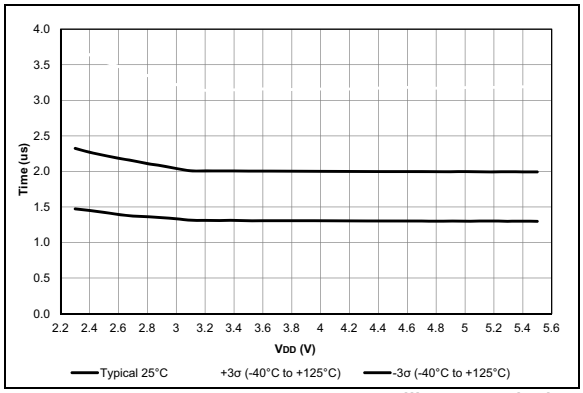


FIGURE 38-76: *ADC RC Oscillator Period, PIC16F18855/75 Only.*

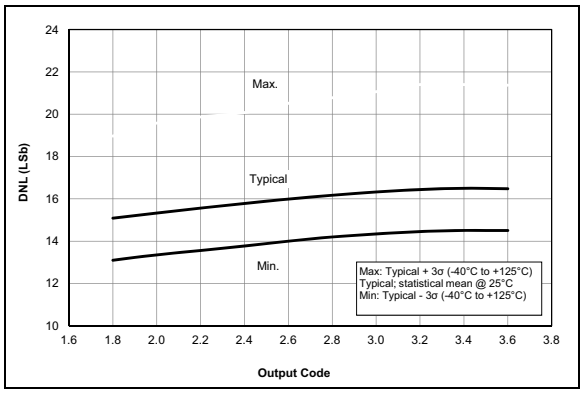


FIGURE 38-74: *DAC INL Error, VDD = 3.0V, PIC16LF18855/75 Only.*

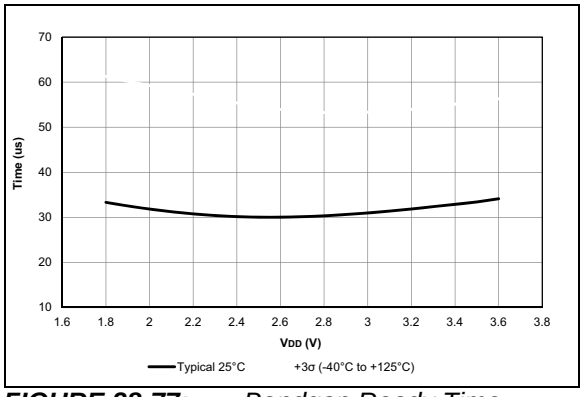


FIGURE 38-77: *Bandgap Ready Time, PIC16LF18855/75 Only.*

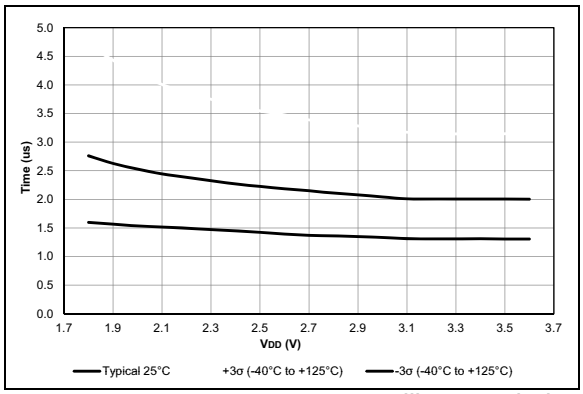


FIGURE 38-75: *ADC RC Oscillator Period, PIC16LF18855/75 Only.*

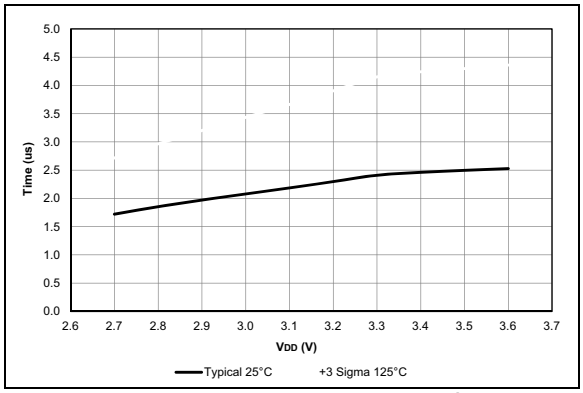
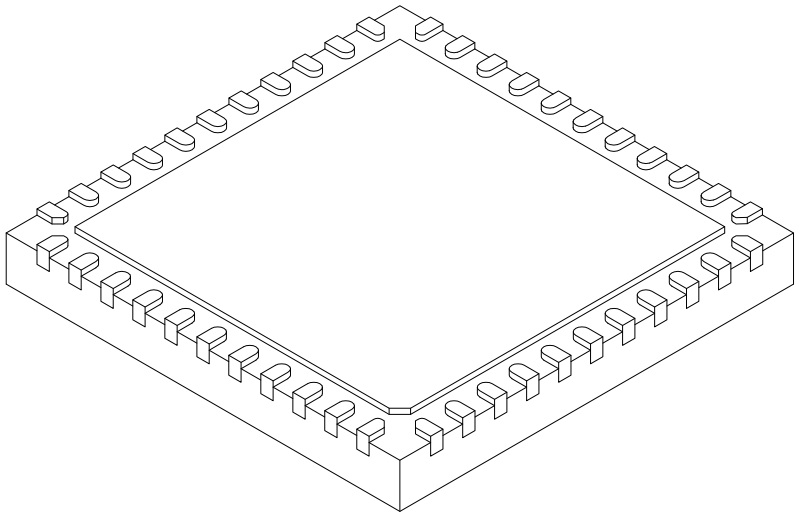


FIGURE 38-78: *BOR Response Time, PIC16LF18855/75 Only.*

44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		44	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Width	E		8.00 BSC	
Exposed Pad Width	E2	6.25	6.45	6.60
Overall Length	D		8.00 BSC	
Exposed Pad Length	D2	6.25	6.45	6.60
Terminal Width	b	0.20	0.30	0.35
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-103C Sheet 2 of 2

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