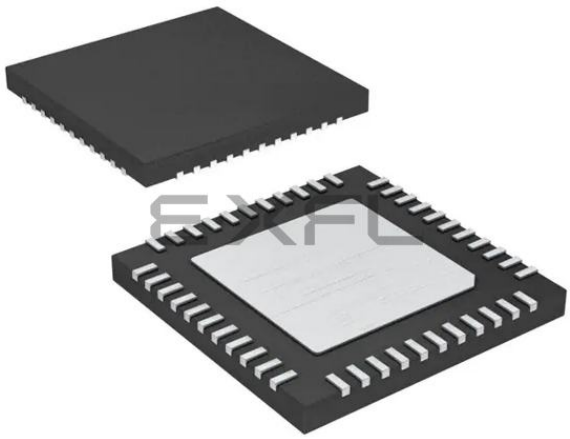

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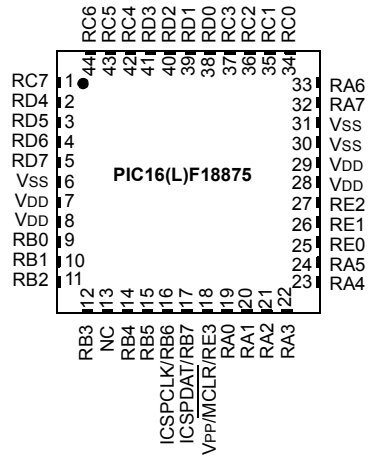
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 35x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f18875-i-ml

44-pin QFN (8x8)



Note 1: See Table 3 for location of all peripheral functions.

2: All VDD and all VSS pins must be connected at the circuit board level. Allowing one or more VSS or VDD pins to float may result in degraded electrical performance or non-functionality.

3: The bottom pad of the QFN/UQFN package should be connected to VSS at the circuit board level.

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TABLE 1-2: PIC16F18855 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RB2/ANB2/SDA2(3,4)/SDI2(1)/ CWG3IN(1)/IOCB2	RB2	TTL/ST	CMOS/OD	General purpose I/O.
	ANB2	AN	—	ADC Channel B2 input.
	SDA2(3,4)	I2C/ SMBus	OD	MSSP2 I2C serial data input/output.
	SDI2(1)	TTL/ST	—	MSSP2 SPI serial data input.
	CWG3IN(1)	TTL/ST	—	Complementary Waveform Generator 3 input.
	IOCB2	TTL/ST	—	Interrupt-on-change input.
RB3/ANB3/C1IN2-/C2IN2-/IOCB3	RB3	TTL/ST	CMOS/OD	General purpose I/O.
	ANB3	AN	—	ADC Channel B3 input.
	C1IN2-	AN	—	Comparator negative input.
	C2IN2-	AN	—	Comparator negative input.
	IOCB3	TTL/ST	—	Interrupt-on-change input.
RB4/ANB4/ADCACT(1)/T5G(1)/ SMTWIN2(1)/IOCB4	RB4	TTL/ST	CMOS/OD	General purpose I/O.
	ANB4	AN	—	ADC Channel B4 input.
	ADCACT(1)	TTL/ST	—	ADC Auto-Conversion Trigger input.
	T5G(1)	TTL/ST	—	Timer5 gate input.
	SMTWIN2(1)	TTL/ST	—	Signal Measurement Timer 2 (SMT2) window input.
	IOCB4	TTL/ST	—	Interrupt-on-change input.
RB5/ANB5/T1G(1)/SMTSIG2(1)/ CCP3(1)/IOCB5	RB5	TTL/ST	CMOS/OD	General purpose I/O.
	ANB5	AN	—	ADC Channel B5 input.
	T1G(1)	TTL/ST	—	Timer1 gate input.
	SMTSIG2(1)	TTL/ST	—	Signal Measurement Timer 2 (SMT2) signal input.
	CCP3(1)	TTL/ST	CMOS/OD	Capture/compare/PWM3 (default input location for capture function).
	IOCB5	TTL/ST	—	Interrupt-on-change input.
RB6/ANB6/CLCIN2(1)/IOCB6/ICSPCLK	RB6	TTL/ST	CMOS/OD	General purpose I/O.
	ANB6	AN	—	ADC Channel B6 input.
	CLCIN2(1)	TTL/ST	—	Configurable Logic Cell source input.
	IOCB6	TTL/ST	—	Interrupt-on-change input.
	ICSPCLK	ST	—	In-Circuit Serial Programming™ and debugging clock input.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I2C = Schmitt Trigger input with I2C
HV = High Voltage XTAL = Crystal levels

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 13-1 for details on which PORT pins may be used for this signal.

2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 13-3.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I2C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I2C specific or SMBus input buffer thresholds.

TABLE 3-13: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-31 (CONTINUED)

Address	Name	PIC16(L)F18855	PIC16(L)F18875	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Bank 8													
CPU CORE REGISTERS; see Table 3-2 for specifics													
40Ch	SCANLADRL			LADR<7:0>								0000 0000	0000 0000
40Dh	SCANLADRH			LADR<15:8>								0000 0000	0000 0000
40Eh	SCANHADRL			HADR<7:0>								1111 1111	1111 1111
40Fh	SCANHADRH			HADR<15:8>								1111 1111	1111 1111
410h	SCANCON0			EN	SCANGO	BUSY	INVALID	INTM	—	MODE<1:0>		0000 0-00	0000 0-00
411h	SCANTRIG			—	—	—	—	TSEL<3:0>				---- 0000	---- 0000
412h	—	—		Unimplemented								—	—
413h	—	—		Unimplemented								—	—
414h	—	—		Unimplemented								—	—
415h	—	—		Unimplemented								—	—
416h	CRCDATL			DATA<7:0>								xxxx xxxx	xxxx xxxx
417h	CRCDATH			DATA<15:8>								xxxx xxxx	xxxx xxxx
418h	CRCACCL			ACC<7:0>								0000 0000	0000 0000
419h	CRCACCH			ACC<15:8>								0000 0000	0000 0000
41Ah	CRCSHIFTL			SHIFT<7:0>								0000 0000	0000 0000
41Bh	CRCSHIFTH			SHIFT<15:8>								0000 0000	0000 0000
41Ch	CRCXORL			X<7:1>							—	xxxx xxx-	xxxx xxx-
41Dh	CRCXORH			X<15:8>								xxxx xxxx	xxxx xxxx
41Eh	CRCCON0			EN	CRCGO	BUSY	ACCM	—	—	SHIFTM	FULL	0000 --00	0000 --00
41Fh	CRCCON1			DLEN<3:0>				PLEN<3:0>				0000 0000	0000 0000

Legend: x = unknown, u = unchanged, q =depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Register present on PIC16F18855/75 devices only.

2: Unimplemented, read as '1'.

TABLE 3-13: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-31 (CONTINUED)

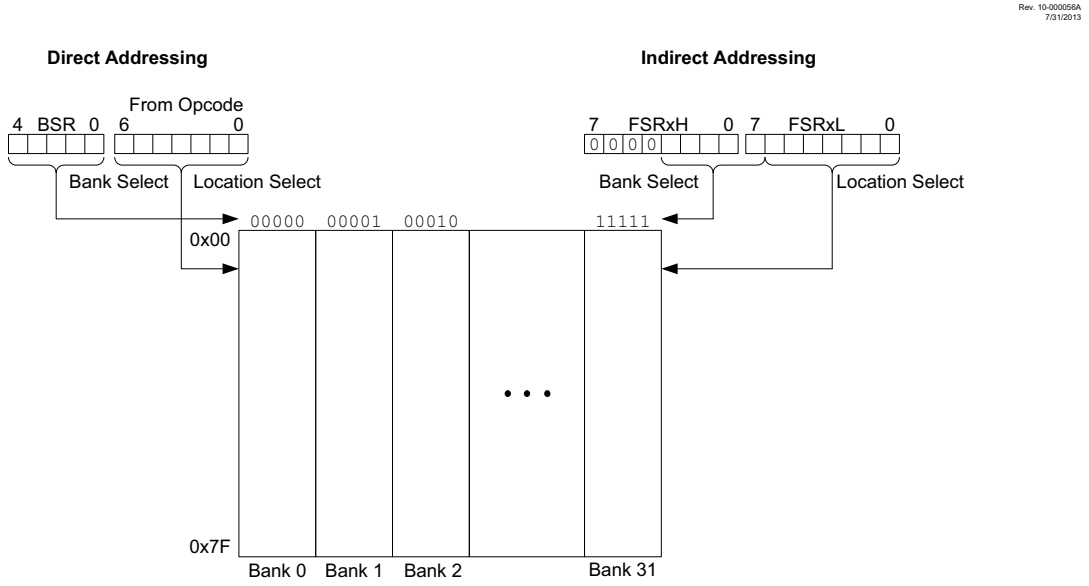
Address	Name	PIC16(L)F18855	PIC16(L)F18875	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Bank 11													
CPU CORE REGISTERS; see Table 3-2 for specifics													
58Ch	NCO1ACCL			NCO1ACC<7:0>								0000 0000	0000 0000
58Dh	NCO1ACCH			NCO1ACC<15:8>								0000 0000	0000 0000
58Eh	NCO1ACCU			—	—	—	—	NCO1ACC<19:16>				---- 0000	---- 0000
58Fh	NCO1INCL			NCO1INC<7:0>								0000 0001	0000 0001
590h	NCO1INCH			NCO1INC<15:8>								0000 0000	0000 0000
591h	NCO1INCU			—	—	—	—	NCO1INC<19:16>				---- 0000	---- 0000
592h	NCO1CON			N1EN	—	N1OUT	N1POL	—	—	—	N1PFM	0-00 ---0	0-00 ---0
593h	NCO1CLK			N1PWS<2:0>			—	—	N1CKS<2:0>			000- -000	000- -000
594h	—	—		Unimplemented								—	—
595h	—	—		Unimplemented								—	—
596h	—	—		Unimplemented								—	—
597h	—	—		Unimplemented								—	—
598h	—	—		Unimplemented								—	—
599h	—	—		Unimplemented								—	—
59Ah	—	—		Unimplemented								—	—
59Bh	—	—		Unimplemented								—	—
59Ch	—	—		Unimplemented								—	—
59Dh	—	—		Unimplemented								—	—
59Eh	—	—		Unimplemented								—	—
59Fh	—	—		Unimplemented								—	—

Legend: x = unknown, u = unchanged, q =depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Register present on PIC16F18855/75 devices only.

2: Unimplemented, read as '1'.

FIGURE 3-9: TRADITIONAL DATA MEMORY MAP



4.3 Code Protection

Code protection allows the device to be protected from unauthorized access. Program memory protection and data memory are controlled independently. Internal access to the program memory is unaffected by any code protection setting.

4.3.1 PROGRAM MEMORY PROTECTION

The entire program memory space is protected from external reads and writes by the $\overline{CP}$ bit in Configuration Words. When $\overline{CP}$ = 0, external reads and writes of program memory are inhibited and a read will return all '0's. The CPU can continue to read program memory, regardless of the protection bit settings. Self-writing the program memory is dependent upon the write protection setting. See **Section 4.4 "Write Protection"** for more information.

4.3.2 DATA MEMORY PROTECTION

The entire data EEPROM memory space is protected from external reads and writes by the $\overline{CPD}$ bit in the Configuration Words. When $\overline{CPD}$ = 0, external reads and writes of EEPROM memory are inhibited and a read will return all '0's. The CPU can continue to read EEPROM memory, regardless of the protection bit settings.

4.4 Write Protection

Write protection allows the device to be protected from unintended self-writes. Applications, such as boot loader software, can be protected while allowing other regions of the program memory to be modified.

The WRT<1:0> bits in Configuration Words define the size of the program memory block that is protected.

4.5 User ID

Four memory locations (8000h-8003h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are readable and writable during normal execution. See **Section 10.4.7 "NVMREG Data EEPROM Memory, User ID, Device ID and Configuration Word Access"** for more information on accessing these memory locations. For more information on checksum calculation, see the *"PIC16(L)F188XX Memory Programming Specification"* (DS40001753).

6.2 Clock Source Types

Clock sources can be classified as external or internal.

External clock sources rely on external circuitry for the clock source to function. Examples are: oscillator modules (ECH, ECM, ECL mode), quartz crystal resonators or ceramic resonators (LP, XT and HS modes).

Internal clock sources are contained within the oscillator module. The internal oscillator block has two internal oscillators and a dedicated Phase Lock Loop (PLL) that are used to generate internal system clock sources. The High-Frequency Internal Oscillator (HFINTOSC) can produce a range from 1 to 32 MHz. The Low-Frequency Internal Oscillator (LFINTOSC) generates a 31 kHz frequency. The external oscillator block can also be used with the PLL. See **Section 6.2.1.4 "4x PLL"** for more details.

The system clock can be selected between external or internal clock sources via the NOSC bits in the OSCCON1 register. See **Section 6.3 "Clock Switching"** for additional information.

6.2.1 EXTERNAL CLOCK SOURCES

An external clock source can be used as the device system clock by performing one of the following actions:

- Program the RSTOSC<2:0> bits in the Configuration Words to select an external clock source that will be used as the default system clock upon a device Reset
- Write the NOSC<2:0> and NDIV<4:0> bits in the OSCCON1 register to switch the system clock source

See **Section 6.3 "Clock Switching"**for more information.

6.2.1.1 EC Mode

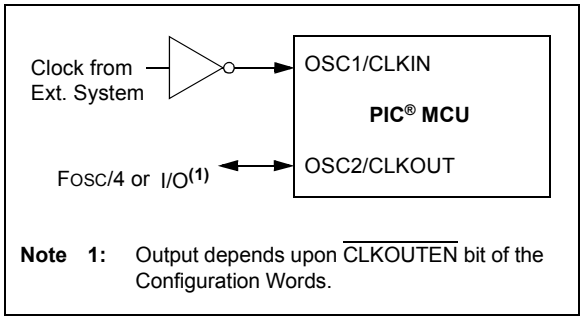
The External Clock (EC) mode allows an externally generated logic level signal to be the system clock source. When operating in this mode, an external clock source is connected to the OSC1 input. OSC2/CLKOUT is available for general purpose I/O or CLKOUT. Figure 6-2 shows the pin connections for EC mode.

EC mode has three power modes to select from through Configuration Words:

- ECH – High power, 4-32 MHz
- ECM – Medium power, 0.1-4 MHz
- ECL – Low power, 0-0.1 MHz

The Oscillator Start-up Timer (OST) is disabled when EC mode is selected. Therefore, there is no delay in operation after a Power-on Reset (POR) or wake-up from Sleep. Because the PIC® MCU design is fully static, stopping the external clock input will have the effect of halting the device while leaving all data intact. Upon restarting the external clock, the device will resume operation as if no time had elapsed.

FIGURE 6-2: EXTERNAL CLOCK (EC) MODE OPERATION



Note 1: Output depends upon $\overline{\text{CLKOUTEN}}$ bit of the Configuration Words.

6.2.1.2 LP, XT, HS Modes

The LP, XT and HS modes support the use of quartz crystal resonators or ceramic resonators connected to OSC1 and OSC2 (Figure 6-3). The three modes select a low, medium or high gain setting of the internal inverter-amplifier to support various resonator types and speed.

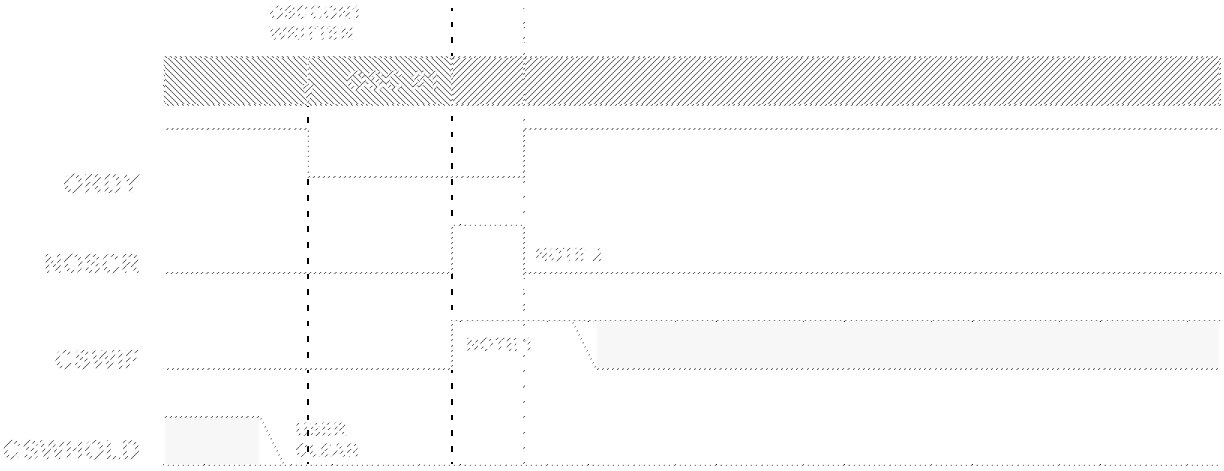
LP Oscillator mode selects the lowest gain setting of the internal inverter-amplifier. LP mode current consumption is the least of the three modes. This mode is designed to drive only 32.768 kHz tuning-fork type crystals (watch crystals).

XT Oscillator mode selects the intermediate gain setting of the internal inverter-amplifier. XT mode current consumption is the medium of the three modes. This mode is best suited to drive resonators with a medium drive level specification.

HS Oscillator mode selects the highest gain setting of the internal inverter-amplifier. HS mode current consumption is the highest of the three modes. This mode is best suited for resonators that require a high drive setting.

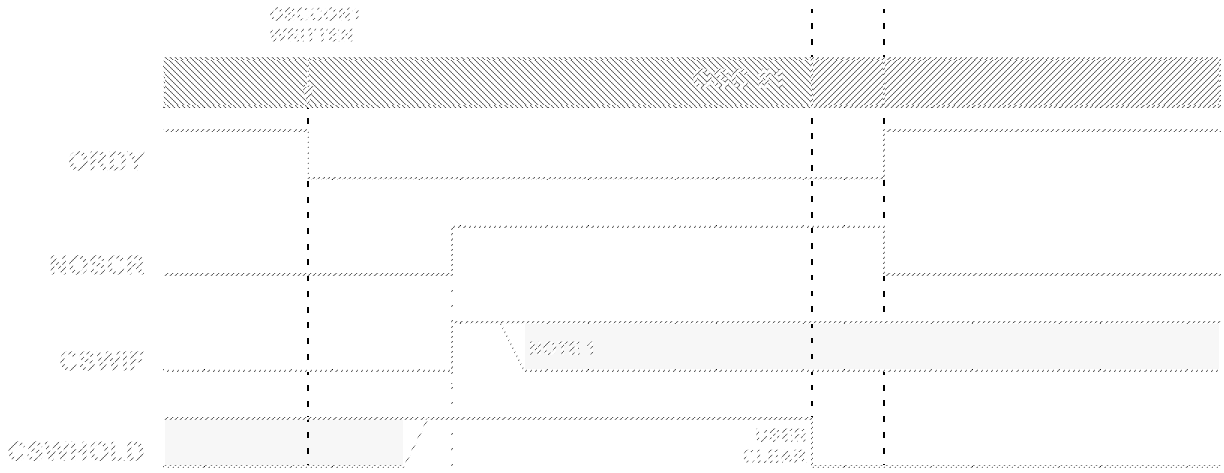
Figure 6-3 and Figure 6-4 show typical circuits for quartz crystal and ceramic resonators, respectively.

FIGURE 6-6: CLOCK SWITCH (CSWHOLD = 0)



Note 1: CSWIF is asserted coincident with NOSCR; interrupt is serviced at OSC#2 speed.
2: The assertion of NOSCR is hidden from the user because it appears only for the duration of the switch.

FIGURE 6-7: CLOCK SWITCH (CSWHOLD = 1)



Note 1: CSWIF is asserted coincident with NOSCR, and may be cleared before or after clearing CSWHOLD = 0.

TABLE 8-1: SUMMARY OF REGISTERS ASSOCIATED WITH POWER-DOWN MODE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	—	—	—	—	—	INTEDG	134
PIE0	—	—	TMR0IE	IOCIE	—	—	—	INTE	135
PIE1	OSFIE	CSWIE	—	—	—	—	ADTIE	ADIE	136
PIE2	—	ZCDIE	—	—	—	—	C2IE	C1IE	137
PIE3	—	—	RCIE	TXIE	BCL2IE	SSP2IE	BCL1IE	SSP1IE	138
PIE4	—	—	TMR6IE	TMR5IE	TMR4IE	TMR3IE	TMR2IE	TMR1IE	139
PIR0	—	—	TMR0IF	IOCIF	—	—	—	INTF	144
PIR1	OSFIF	CSWIF	—	—	—	—	ADTIF	ADIF	145
PIR2	—	ZCDIF	—	—	—	—	C2IF	C1IF	146
PIR3	—	—	RCIF	TXIF	BCL2IF	SSP2IF	BCL1IF	SSP1IF	147
PIR4	—	—	TMR6IF	TMR5IF	TMR4IF	TMR3IF	TMR2IF	TMR1IF	148
IOCAP	IOCAP7	IOCAP6	IOCAP5	IOCAP4	IOCAP3	IOCAP2	IOCAP1	IOCAP0	262
IOCAN	IOCAN7	IOCAN6	IOCAN5	IOCAN4	IOCAN3	IOCAN2	IOCAN1	IOCAN0	262
IOCAF	IOCAF7	IOCAF6	IOCAF5	IOCAF4	IOCAF3	IOCAF2	IOCAF1	IOCAF0	262
IOCCP	IOCCP7	IOCCP6	IOCCP5	IOCCP4	IOCCP3	IOCCP2	IOCCP1	IOCCP0	264
IOCBP	IOCBP7	IOCBP6	IOCBP5	IOCBP4	IOCBP3	IOCBP2	IOCBP1	IOCBP0	263
IOCBN	IOCBN7	IOCBN6	IOCBN5	IOCBN4	IOCBN3	IOCBN2	IOCBN1	IOCBN0	263
IOCBF	IOCBF7	IOCBF6	IOCBF5	IOCBF4	IOCBF3	IOCBF2	IOCBF1	IOCBF0	263
IOCCN	IOCCN7	IOCCN6	IOCCN5	IOCCN4	IOCCN3	IOCCN2	IOCCN1	IOCCN0	264
IOCCF	IOCCF7	IOCCF6	IOCCF5	IOCCF4	IOCCF3	IOCCF2	IOCCF1	IOCCF0	264
IOCEP	—	—	—	—	IOCEP3	—	—	—	265
IOCEN	—	—	—	—	IOCEN3	—	—	—	265
IOCEF	—	—	—	—	IOCEF3	—	—	—	266
STATUS	—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC	C	38
VREGCON	—	—	—	—	—	—	VREGPM	Reserved	159
CPUDOZE	IDLEN	DOZEN	ROI	DOE	—	DOZE<2:0>			160
WDTCON0	—	—	WDTPS<4:0>					SWDTEN	166
IOCEP	—	—	—	—	IOCEP3	—	—	—	265
IOCEN	—	—	—	—	IOCEN3	—	—	—	265
IOCEF	—	—	—	—	IOCEF3	—	—	—	266

Legend: — = unimplemented location, read as '0'. Shaded cells are not used in Power-Down mode.

REGISTER 12-38: SLRCOND: PORTD SLEW RATE CONTROL REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
SLRD7	SLRD6	SLRD5	SLRD4	SLRD3	SLRD2	SLRD1	SLRD0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **SLRD<7:0>:** PORTD Slew Rate Enable bits
For RD<7:0> pins, respectively
1 = Port pin slew rate is limited
0 = Port pin slews at maximum rate

REGISTER 12-39: INLVLD: PORTD INPUT LEVEL CONTROL REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
INLVLD7	INLVLD6	INLVLD5	INLVLD4	INLVLD3	INLVLD2	INLVLD1	INLVLD0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **INLVLD<7:0>:** PORTD Input Level Select bits
For RD<7:0> pins, respectively
1 = ST input used for PORT reads and interrupt-on-change
0 = TTL input used for PORT reads and interrupt-on-change

REGISTER 12-44: INLVLE: PORTE INPUT LEVEL CONTROL REGISTER

U-0	U-0	U-0	U-0	R/W-1/1	U-0	U-0	U-0
—	—	—	—	INLVLE3	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **INLVLE3:** PORTE Input Level Select bits
For RE3 pin,
1 = ST input used for PORT reads and interrupt-on-change
0 = TTL input used for PORT reads and interrupt-on-change

bit 2-0 **Unimplemented:** Read as '0'

TABLE 12-6: SUMMARY OF REGISTERS ASSOCIATED WITH PORTE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
PORTE	—	—	—	—	RE3	—	—	—	233
WPUE	—	—	—	—	WPUE3	—	—	—	233
INLVLE	—	—	—	—	INLVLE3	—	—	—	234

Legend: x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by PORTE.

TABLE 12-7: SUMMARY OF CONFIGURATION WORD WITH PORTE

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
CONFIG2	13:8	—	—	$\overline{\text{DEBUG}}$	STVREN	PPS1WAY	ZCDDIS	BORV	—	93
	7:0	BOREN<1:0>		$\overline{\text{LPBOREN}}$	—	—	—	$\overline{\text{PWRTE}}$	MCLRE	

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by PORTE.

19.1.1 PWM CLOCK SELECTION

The PIC16(L)F18855/75 allows each individual CCP and PWM module to select the timer source that controls the module. Each module has an independent selection.

As there are up to three 8-bit timers with auto-reload (Timer2/4/6), PWM mode on the CCP and PWM modules can use any of these timers.

The CCPTMRS0 and CCPTMRS1 register are used to select which timer is used.

19.1.2 USING THE TMR2/4/6 WITH THE PWM MODULE

This device has a newer version of the TMR2 module that has many new modes, which allow for greater customization and control of the PWM signals than on older parts. Refer to Section 29.5, Operation Examples for examples of PWM signal generation using the different modes of Timer2. PWM operation requires that the timer used as the PWM time base has the FOSC/4 clock source selected.

19.1.3 PWM PERIOD

Referring to Figure 19-1, the PWM output has a period and a pulse width. The frequency of the PWM is the inverse of the period (1/period).

The PWM period is specified by writing to the PR2 register. The PWM period can be calculated using the following formula:

EQUATION 19-1: PWM PERIOD

$$PWM\ Period = [(PR2) + 1] \cdot 4 \cdot TOSC \cdot (TMR2\ Prescale\ Value)$$

Note 1: TOSC = 1/FOSC

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The PWMx pin is set (Exception: If the PWM duty cycle = 0%, the pin will not be set.)
- The PWM pulse width is latched from PWMxDC.

Note:	If the pulse width value is greater than the period the assigned PWM pin(s) will remain unchanged.

19.1.4 PWM DUTY CYCLE

The PWM duty cycle is specified by writing a 10-bit value to the PWMxDC register. The PWMxDCH contains the eight MSbs and the PWMxDCL<7:6> bits contain the two LSbs.

The PWMDC register is double-buffered and can be updated at any time. This double buffering is essential for glitch-free PWM operation. New values take effect when TMR2 = PR2. Note that PWMDC is left-justified.

The 8-bit timer TMR2 register is concatenated with either the 2-bit internal system clock (FOSC), or two bits of the prescaler, to create the 10-bit time base. The system clock is used if the Timer2 prescaler is set to 1:1.

Equation 19-2 is used to calculate the PWM pulse width.

Equation 19-3 is used to calculate the PWM duty cycle ratio.

EQUATION 19-2: PULSE WIDTH

$$Pulse\ Width = (PWMxDC) \cdot TOSC \cdot (TMR2\ Prescale\ Value)$$

EQUATION 19-3: DUTY CYCLE RATIO

$$Duty\ Cycle\ Ratio = \frac{(PWMxDC)}{4(PR2 + 1)}$$

19.1.5 PWM RESOLUTION

The resolution determines the number of available duty cycles for a given period. For example, a 10-bit resolution will result in 1024 discrete duty cycles, whereas an 8-bit resolution will result in 256 discrete duty cycles.

The maximum PWM resolution is ten bits when PR2 is 255. The resolution is a function of the PR2 register value as shown by Equation 19-4.

EQUATION 19-4: PWM RESOLUTION

$$Resolution = \frac{\log[4(PR2 + 1)]}{\log(2)}\ bits$$

Note:	If the pulse width value is greater than the period the assigned PWM pin(s) will remain unchanged.

19.1.6 OPERATION IN SLEEP MODE

In Sleep mode, the TMR2 register will not increment and the state of the module will not change. If the PWMx pin is driving a value, it will continue to drive that value. When the device wakes up, TMR2 will continue from its previous state.

21.6 Handling VPEAK variations

If the peak amplitude of the external voltage is expected to vary, the series resistor must be selected to keep the ZCD current source and sink below the design maximum range of ± 600 μA and above a reasonable minimum range. A general rule of thumb is that the maximum peak voltage can be no more than six times the minimum peak voltage. To ensure that the maximum current does not exceed ± 600 μA and the minimum is at least ± 100 μA, compute the series resistance as shown in Equation 21-5. The compensating pull-up for this series resistance can be determined with Equation 21-4 because the pull-up value is independent from the peak voltage.

EQUATION 21-5: SERIES R FOR V RANGE

$$R_{SERIES} = \frac{V_{MAXPEAK} + V_{MINPEAK}}{7 \times 10^{-4}}$$

21.7 Operation During Sleep

The ZCD current sources and interrupts are unaffected by Sleep.

21.8 Effects of a Reset

The ZCD circuit can be configured to default to the active or inactive state on Power-On-Reset (POR). When the ZCDDIS Configuration bit is cleared, the ZCD circuit will be active at POR. When the $\overline{ZCD}$ Configuration bit is set, the EN bit of the ZCDxCON register must be set to enable the ZCD module.

21.9 Disabling the ZCD Module

The ZCD module can be disabled in two ways:

1. Configuration Word 2H has the $\overline{ZCD}$ bit, which disables the ZCD module when set, but it can be enabled using the EN bit of the ZCDCON register (Register 21-1). If the $\overline{ZCD}$ bit is clear, the ZCD is always enabled.
2. The ZCD can also be disabled using the ZCDMD bit of the PMD2 register (Register 14-3) this is subject to the status of the $\overline{ZCD}$ bit.

REGISTER 23-8: ADPCH: ADC POSITIVE CHANNEL SELECTION REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	ADPCH<5:0>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **Unimplemented**: Read as '0'

bit 5-0 **ADPCH<5:0>**: ADC Positive Input Channel Selection bits

111111 = Fixed Voltage Reference (FVR)(2)
111110 = DAC1 output(1)
111101 = Temperature Indicator(3)
111100 = AVSS (Analog Ground)
111011 = Reserved. No channel connected.
•
•
•
100010 = ANE2(4)
100001 = ANE1(4)
100000 = ANE0(4)
011111 = AND7(4)
011110 = AND6(4)
011101 = AND5(4)
011100 = AND4(4)
011011 = AND3(4)
011010 = AND2(4)
011001 = AND1(4)
011000 = AND0(4)
010111 = ANC7
010110 = ANC6
010101 = ANC5
010100 = ANC4
010011 = ANC3
010010 = ANC2
010001 = ANC1
010000 = ANC0
001111 = ANB7
001110 = ANB6
001101 = ANB5
001100 = ANB4
001011 = ANB3
001010 = ANB2
001001 = ANB1
001000 = ANB0
000111 = ANA7
000110 = ANA6
000101 = ANA5
000100 = ANA4
000011 = ANA3
000010 = ANA2
000001 = ANA1
000000 = ANA0

Note 1: See **Section 25.0 "5-Bit Digital-to-Analog Converter (DAC1) Module"** for more information.
2: See **Section 16.0 "Fixed Voltage Reference (FVR)"** for more information.
3: See **Section 17.0 "Temperature Indicator Module"** for more information.
4: PIC16(L)F18875 only.

REGISTER 29-2: TxCON: TIMER2/4/6 CONTROL REGISTER

R/W/HC-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
ON(1)	CKPS<2:0>			OUTPS<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HC = Bit is cleared by hardware

bit 7 **ON:** Timerx On bit
1 = Timerx is on
0 = Timerx is off: all counters and state machines are reset

bit 6-4 **CKPS<2:0>:** Timer2-type Clock Prescale Select bits
111 = 1:128 Prescaler
110 = 1:64 Prescaler
101 = 1:32 Prescaler
100 = 1:16 Prescaler
011 = 1:8 Prescaler
010 = 1:4 Prescaler
001 = 1:2 Prescaler
000 = 1:1 Prescaler

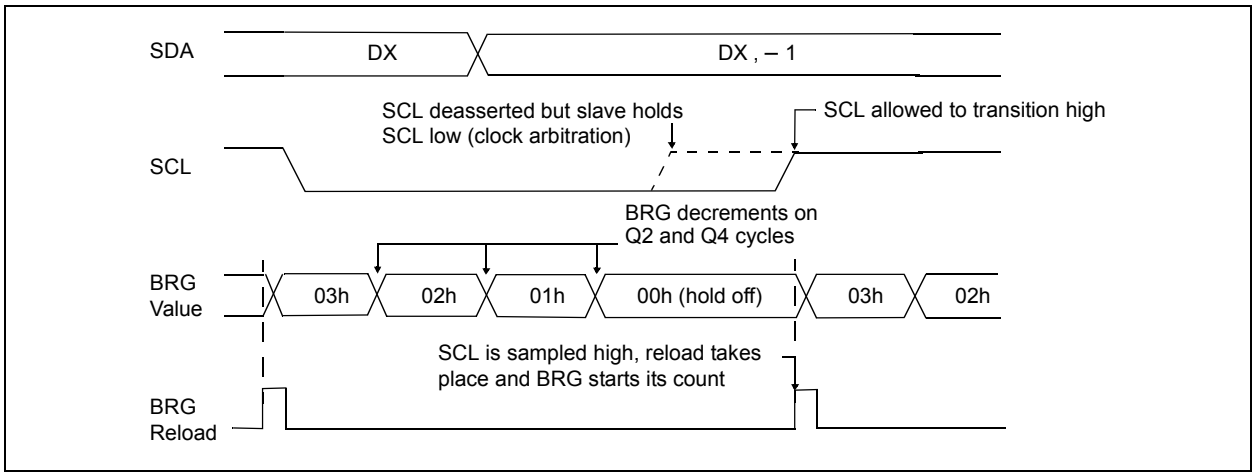
bit 3-0 **OUTPS<3:0>:** Timerx Output Postscaler Select bits
1111 = 1:16 Postscaler
1110 = 1:15 Postscaler
1101 = 1:14 Postscaler
1100 = 1:13 Postscaler
1011 = 1:12 Postscaler
1010 = 1:11 Postscaler
1001 = 1:10 Postscaler
1000 = 1:9 Postscaler
0111 = 1:8 Postscaler
0110 = 1:7 Postscaler
0101 = 1:6 Postscaler
0100 = 1:5 Postscaler
0011 = 1:4 Postscaler
0010 = 1:3 Postscaler
0001 = 1:2 Postscaler
0000 = 1:1 Postscaler

Note 1: In certain modes, the ON bit will be auto-cleared by hardware. See **Section 29.5 "Operation Examples"**.

31.6.2 CLOCK ARBITRATION

Clock arbitration occurs when the master, during any receive, transmit or Repeated Start/Stop condition, releases the SCL pin (SCL allowed to float high). When the SCL pin is allowed to float high, the Baud Rate Generator (BRG) is suspended from counting until the SCL pin is actually sampled high. When the SCL pin is sampled high, the Baud Rate Generator is reloaded with the contents of SSPxADD<7:0> and begins counting. This ensures that the SCL high time will always be at least one BRG rollover count in the event that the clock is held low by an external device (Figure 31-25).

FIGURE 31-25: BAUD RATE GENERATOR TIMING WITH CLOCK ARBITRATION



31.6.3 WCOL STATUS FLAG

If the user writes the SSPxBUF when a Start, Restart, Stop, Receive or Transmit sequence is in progress, the WCOL is set and the contents of the buffer are unchanged (the write does not occur). Any time the WCOL bit is set it indicates that an action on SSPxBUF was attempted while the module was not idle.

Note:	Because queuing of events is not allowed, writing to the lower five bits of SSPxCON2 is disabled until the Start condition is complete.

31.7 BAUD RATE GENERATOR

The MSSP module has a Baud Rate Generator available for clock generation in both I^2C and SPI Master modes. The Baud Rate Generator (BRG) reload value is placed in the SSPxADD register (Register 31-6). When a write occurs to SSPxBUF, the Baud Rate Generator will automatically begin counting down.

Once the given operation is complete, the internal clock will automatically stop counting and the clock pin will remain in its last state.

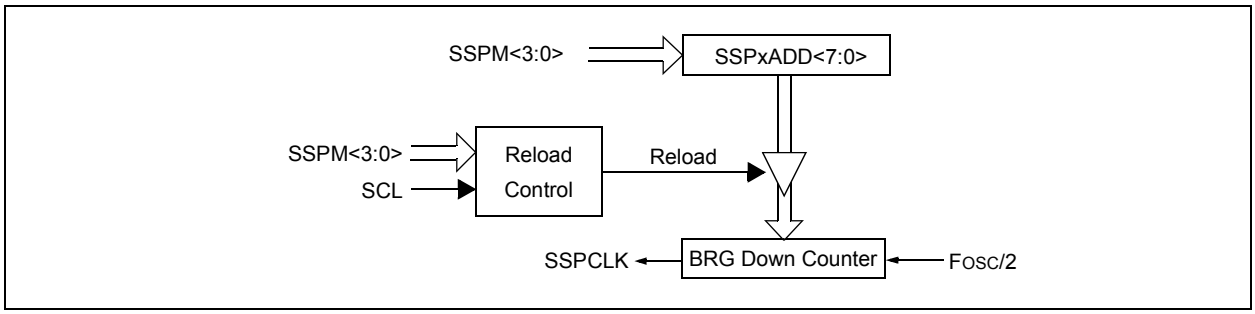
An internal signal “Reload” in Figure 31-40 triggers the value from SSPxADD to be loaded into the BRG counter. This occurs twice for each oscillation of the module clock line. The logic dictating when the reload signal is asserted depends on the mode the MSSP is being operated in.

Table 31-2 demonstrates clock rates based on instruction cycles and the BRG value loaded into SSPxADD.

EQUATION 31-1:

$$F_{CLOCK} = \frac{F_{OSC}}{(SSP1ADD + 1)(4)}$$

FIGURE 31-40: BAUD RATE GENERATOR BLOCK DIAGRAM



Note: Values of 0x00, 0x01 and 0x02 are not valid for SSPxADD when used as a Baud Rate Generator for I^2C. This is an implementation limitation.

TABLE 31-2: MSSP CLOCK RATE W/BRG

FOSC	FCY	BRG Value	FCLOCK (2 Rollovers of BRG)
32 MHz	8 MHz	13h	400 kHz
32 MHz	8 MHz	19h	308 kHz
32 MHz	8 MHz	4Fh	100 kHz
16 MHz	4 MHz	09h	400 kHz
16 MHz	4 MHz	0Ch	308 kHz
16 MHz	4 MHz	27h	100 kHz
4 MHz	1 MHz	09h	100 kHz

Note: Refer to the I/O port electrical specifications in Table 37-4 to ensure the system is designed to support IOL requirements.

REGISTER 31-7: SSPxBUF: MSSPx BUFFER REGISTER

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SSPBUF<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **SSPBUF<7:0>:** MSSP Buffer bits

TABLE 31-3: SUMMARY OF REGISTERS ASSOCIATED WITH MSSPx

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	—	—	—	—	—	INTEDG	134
PIR3	—	—	RCIF	TXIF	BCL2IF	SSP2IF	BCL1IF	SSP1IF	147
PIE3	—	—	RCIE	TXIE	BCL2IE	SSP2IE	BCL1IE	SSP1IE	138
SSP1STAT	SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	503
SSP1CON1	WCOL	SSPOV	SSPEN	CKP	SSPM<3:0>				504
SSP1CON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	505
SSP1CON3	ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	503
SSP1MSK	SSPMSK<7:0>								507
SSP1ADD	SSPADD<7:0>								507
SSP1BUF	SSPBUF<7:0>								508
SSP2STAT	SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	503
SSP2CON1	WCOL	SSPOV	SSPEN	CKP	SSPM<3:0>				504
SSP2CON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	505
SSP2CON3	ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	503
SSP2MSK	SSPMSK<7:0>								507
SSP2ADD	SSPADD<7:0>								507
SSP2BUF	SSPBUF<7:0>								508
SSP1CLKPPS	—	—	—	SSP1CLKPPS<4:0>					249
SSP1DATPPS	—	—	—	SSP1DATPPS<4:0>					249
SSP1SSPPS	—	—	—	SSP1SSPPS<4:0>					249
SSP2CLKPPS	—	—	—	SSP2CLKPPS<4:0>					249
SSP2DATPPS	—	—	—	SSP2DATPPS<4:0>					249
SSP2SSPPS	—	—	—	SSP2SSPPS<4:0>					249
RxyPPS	—	—	—	RxyPPS<4:0>					250

Legend: — = Unimplemented location, read as '0'. Shaded cells are not used by the MSSPx module

Note 1: When using designated I^2C pins, the associated pin values in INLVLx will be ignored.

Note: Unless otherwise noted, VIN = 5V, FOSC = 300 kHz, CIN = 0.1 µF, TA = 25°C.

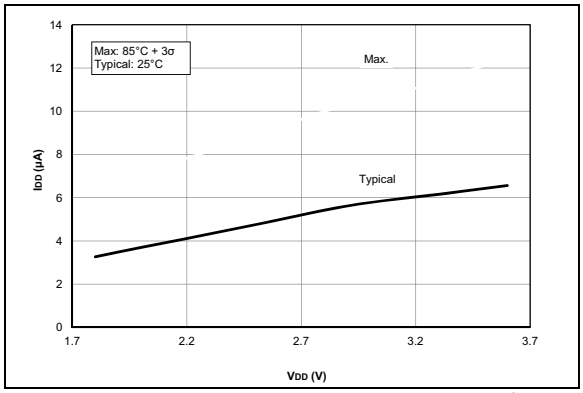


FIGURE 38-7: *IDD, LFINT, Fosc = 31 kHz, PIC16LF18855/75 Only.*

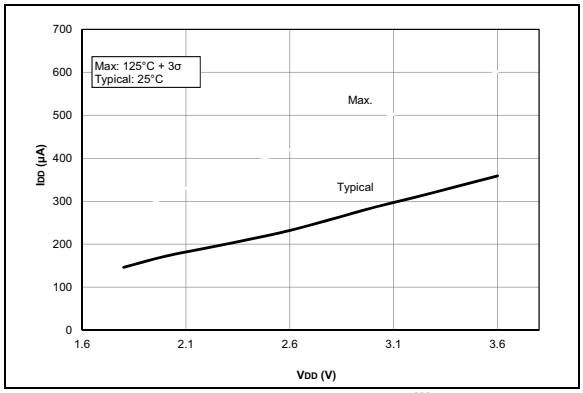


FIGURE 38-10: *IDD, ECM Oscillator, Fosc = 4 MHz, PIC16LF18855/75 Only.*

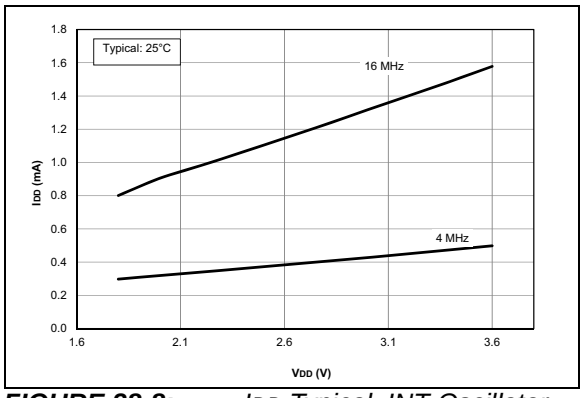


FIGURE 38-8: *IDD Typical, INT Oscillator, PIC16LF18855/75 Only.*

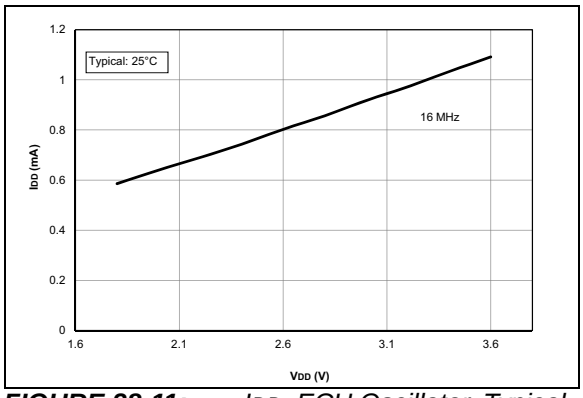


FIGURE 38-11: *IDD, ECH Oscillator, Typical, PIC16LF18855/75 Only.*

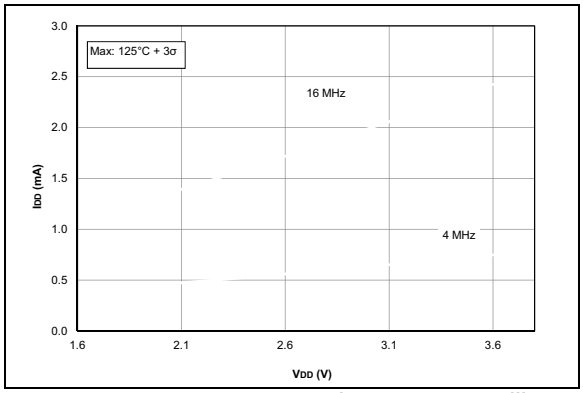


FIGURE 38-9: *IDD Maximum, INT Oscillator, PIC16LF18855/75 Only.*

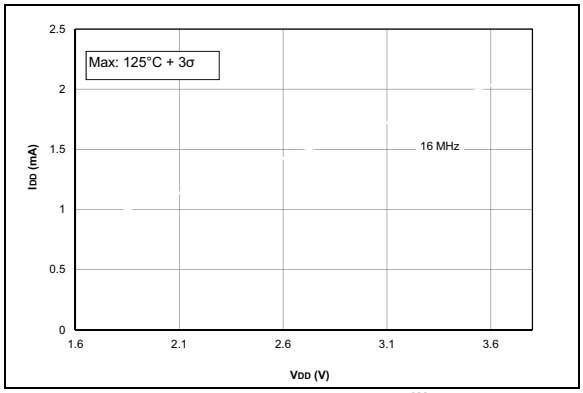


FIGURE 38-12: *IDD, ECH Oscillator, LP Mode, Maximum, PIC16LF18855/75 Only.*