



Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 35x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f18875t-i-ml

TABLE 3-13: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-31 (CONTINUED)

Address	Name	PIC16(L)F18855	PIC16(L)F18875	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Bank 30 (Continued)													
F5Ch	SLRCOND	—	X	SLRD7	SLRD6	SLRD5	SLRD4	SLRD3	SLRD2	SLRD1	SLRD0	1111 1111	1111 1111
		X	—	Unimplemented								---- ----	---- ----
F5Dh	INLVLD	—	X	INLVLD7	INLVLD6	INLVLD5	INLVLD4	INLVLD3	INLVLD2	INLVLD1	INLVLD0	1111 1111	1111 1111
		X	—	Unimplemented								---- ----	---- ----
F5Eh — F60h	—	—	—	Unimplemented								—	—
F61h	CCDND	—	X	CCDND7	CCDND6	CCDND5	CCDND4	CCDND3	CCDND2	CCDND1	CCDND0	0000 0000	0000 0000
		X	—	Unimplemented								---- ----	---- ----
F62h	CCDPD	—	X	CCDPD7	CCDPD6	CCDPD5	CCDPD4	CCDPD3	CCDPD2	CCDPD1	CCDPD0	0000 0000	0000 0000
		X	—	Unimplemented								---- ----	---- ----
F63h	—	—	—	Unimplemented								—	—
F64h	ANSELE	—	X	—	—	—	—	—	ANSE2	ANSE1	ANSE0	---- -111	---- -111
		X	—	Unimplemented								---- ----	---- ----
F65h	WPUE	—	X	—	—	—	—	WPUE3	WPUE2	WPUE1	WPUE0	---- 0000	---- 0000
		X	—	—	—	—	—	WPUE3	—	—	—	---- 0---	---- 0---
F66h	ODCONE	—	X	—	—	—	—	—	ODCE2	ODCE1	ODCE0	---- -000	---- -000
		X	—	Unimplemented								---- ----	---- ----
F67h	SLRCONE	—	X	—	—	—	—	—	SLRE2	SLRE1	SLRE0	---- -111	---- -111
		X	—	Unimplemented								---- ----	---- ----
F68h	INLVLE	—	X	—	—	—	—	INLVLE3	INLVLE2	INLVLE1	INLVLE0	---- 1111	---- 1111
		X	—	—	—	—	—	INLVLE3	—	—	—	---- 1---	---- 1---
F69h	IOCEP	—	—	—	—	—	—	IOCEP3	—	—	—	---- 0---	---- 0---
F6Ah	IOCEN	—	—	—	—	—	—	IOCEN3	—	—	—	---- 0---	---- 0---

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Register present on PIC16F18855/75 devices only.

Note 2: Unimplemented, read as '1'.

4.0 DEVICE CONFIGURATION

Device configuration consists of Configuration Words, Code Protection and Device ID.

4.1 Configuration Words

There are several Configuration Word bits that allow different oscillator and memory protection options. These are implemented as shown in Table 4-1.

TABLE 4-1: CONFIGURATION WORD LOCATIONS

Configuration Word	Location
CONFIG1	8007h
CONFIG2	8008h
CONFIG3	8009h
CONFIG4	800Ah
CONFIG5	800Bh

Note: The $\overline{\text{DEBUG}}$ bit in Configuration Words is managed automatically by device development tools including debuggers and programmers. For normal device operation, this bit should be maintained as a '1'.

PIC16(L)F18855/75

REGISTER 4-5: CONFIG5: CONFIGURATION WORD 5: CODE PROTECTION

U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—
bit 13			bit 8		

U-1	U-1	U-1	U-1	U-1	U-1	R/P-1	R/P-1
—	—	—	—	—	—	$\overline{\text{CPD}}$	$\overline{\text{CP}}$
bit 7						bit 0	

Legend:

R = Readable bit

P = Programmable bit

x = Bit is unknown

U = Unimplemented bit, read as '1'

'0' = Bit is cleared

'1' = Bit is set

W = Writable bit

n = Value when blank or after Bulk Erase

bit 13-2 **Unimplemented:** Read as '1'

bit 1 **CPD:** Data NVM (EEPROM) Memory Code Protection bit

1 = EEPROM code protection disabled

0 = EEPROM code protection enabled

bit 0 **CP:** Program Flash Memory Code Protection bit

1 = Program Flash Memory code protection disabled

0 = Program Flash Memory code protection enabled



PIC16(L)F18855/75

REGISTER 6-6: OSCFRQ: HFINTOSC FREQUENCY SELECTION REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-q/q	R/W-q/q	R/W-q/q
—	—	—	—	—	HFFRQ<2:0> ⁽¹⁾		
bit 7					bit 0		

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-3

Unimplemented: Read as '0'

bit 2-0

HFFRQ<2:0>: HFINTOSC Frequency Selection bits

Nominal Freq (MHz) (NOSC = 110):

111 = Reserved

110 = 32

101 = 16

100 = 12

011 = 8

010 = 4

001 = 2

000 = 1

Note 1: When RSTOSC=110 (HFINTOSC 1 MHz), the HFFRQ bits will default to '010' upon Reset; when RSTOSC = 000 (HFINTOSC 32 MHz), the HFFRQ bits will default to '110' upon Reset.

PIC16(L)F18855/75

TABLE 6-3: SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK SOURCES

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
OSCCON1	—	NOSC<2:0>			NDIV<3:0>				122
OSCCON2	—	COSC<2:0>			CDIV<3:0>				122
OSCCON3	CWSHOLD	SOSCPWR	—	ORDY	NOSCR	—	—	—	123
OSCFRQ	—	—	—	—	—	HFFRQ<2:0>			126
OSCSTAT	EXTOR	HFOR	MFOR	LFOR	SOR	ADOR	—	PLLOR	124
OSCTUNE	—	—	HFTUN<5:0>						127
OSCEN	EXTOEN	HFOEN	MFOEN	LFOEN	SOSCEN	ADOEN	—	—	125

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by clock sources.

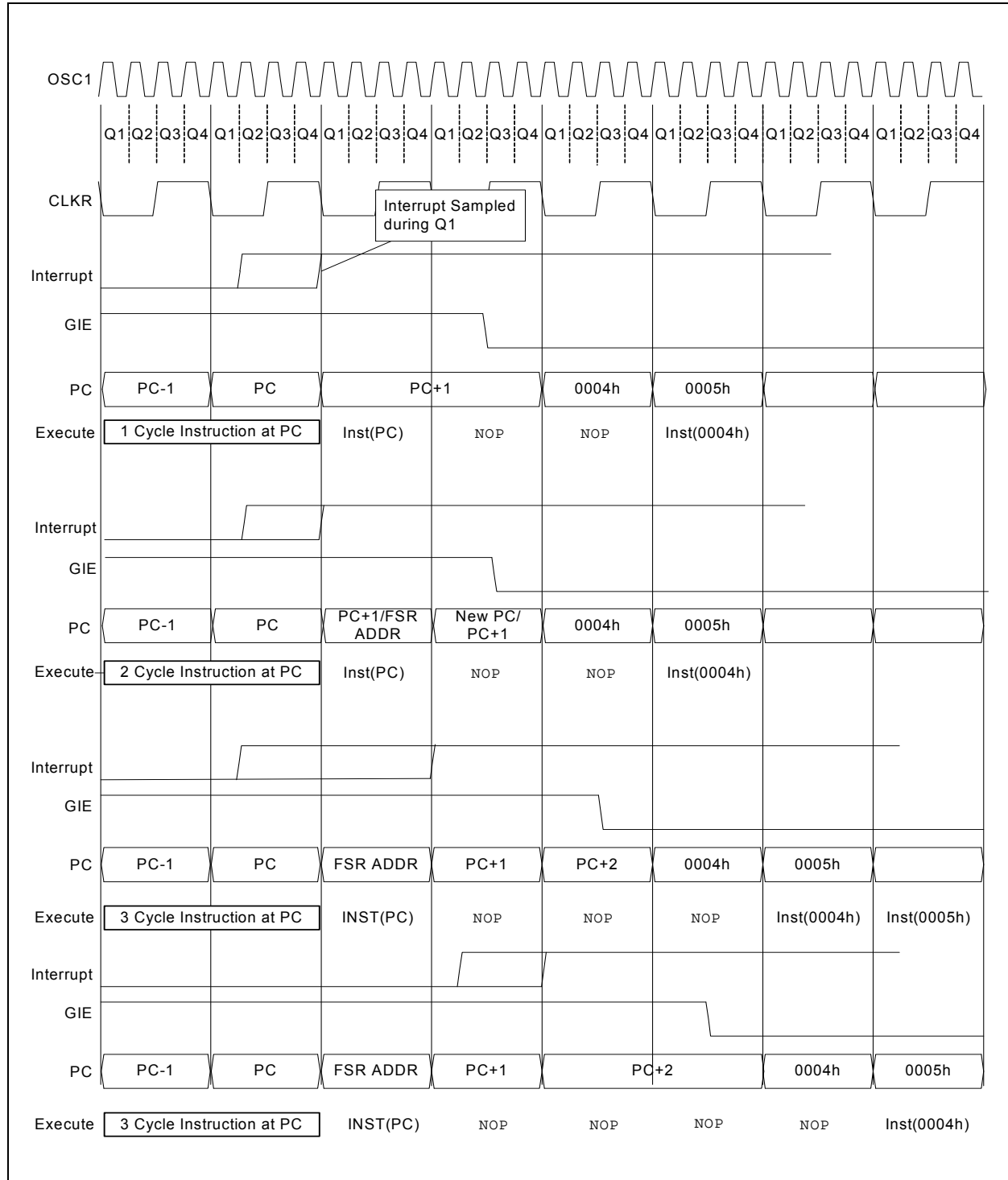
TABLE 6-4: SUMMARY OF CONFIGURATION WORD WITH CLOCK SOURCES

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
CONFIG1	13:8	—	—	FCMEN	—	CSWEN	—	—	CLKOUTEN	93
	7:0	—	RSTOSC<2:0>			—	FEXTOSC<2:0>			

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by clock sources.

PIC16(L)F18855/75

FIGURE 7-2: INTERRUPT LATENCY



PIC16(L)F18855/75

REGISTER 7-18: PIR6: PERIPHERAL INTERRUPT REQUEST REGISTER 6

U-0	U-0	U-0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0
—	—	—	CCP5IF	CCP4IF	CCP3IF	CCP2IF	CCP1IF
bit 7							
							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS = Hardware set

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **CCP5IF:** CCP5 Interrupt Flag bit

CCP5IF = 1:

Capture mode: Capture occurred (must be cleared in software)

Compare mode: Compare match occurred (must be cleared in software)

PWM mode: Output trailing edge occurred (must be cleared in software)

CCP5IF = 0:

Capture mode: Capture did not occur

Compare mode: Compare match did not occur

PWM mode: Output trailing edge did not occur

bit 3 **CCP4IF:** CCP4 Interrupt Flag bit

CCP4IF = 1:

Capture mode: Capture occurred (must be cleared in software)

Compare mode: Compare match occurred (must be cleared in software)

PWM mode: Output trailing edge occurred (must be cleared in software)

CCP4IF = 0:

Capture mode: Capture did not occur

Compare mode: Compare match did not occur

PWM mode: Output trailing edge did not occur

bit 2 **CCP3IF:** CCP3 Interrupt Flag bit

CCP3IF = 1:

Capture mode: Capture occurred (must be cleared in software)

Compare mode: Compare match occurred (must be cleared in software)

PWM mode: Output trailing edge occurred (must be cleared in software)

CCP3IF = 0:

Capture mode: Capture did not occur

Compare mode: Compare match did not occur

PWM mode: Output trailing edge did not occur

bit 1 **CCP2IF:** CCP2 Interrupt Flag bit

CCP2IF = 1:

Capture mode: Capture occurred (must be cleared in software)

Compare mode: Compare match occurred (must be cleared in software)

PWM mode: Output trailing edge occurred (must be cleared in software)

CCP2IF = 0:

Capture mode: Capture did not occur

Compare mode: Compare match did not occur

PWM mode: Output trailing edge did not occur

bit 0 **CCP1IF:** CCP1 Interrupt Flag bit

CCP1IF = 1:

Capture mode: Capture occurred (must be cleared in software)

Compare mode: Compare match occurred (must be cleared in software)

PWM mode: Output trailing edge occurred (must be cleared in software)

CCP1IF = 0:

Capture mode: Capture did not occur

Compare mode: Compare match did not occur

PWM mode: Output trailing edge did not occur

PIC16(L)F18855/75

REGISTER 7-20: PIR8: PERIPHERAL INTERRUPT REQUEST REGISTER 8

U-0	U-0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0
—	—	SMT2PWAIF	SMT2PRAIF	SMT2IF	SMT1PWAIF	SMT1PRAIF	SMT1IF
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

HS = Hardware set

bit 7-6 **Unimplemented:** Read as '0'.

bit 5 **SMT2PWAIF:** SMT2 Pulse Width Acquisition Interrupt Flag bit

1 = Interrupt is pending

0 = Interrupt is not pending

bit 4 **SMT2PRAIF:** SMT2 Period Acquisition Interrupt Flag bit

1 = Interrupt is pending

0 = Interrupt is not pending

bit 3 **SMT2IF:** SMT2 Overflow Interrupt Flag bit

1 = An SMT overflow event has occurred (must be cleared in software)

0 = No overflow event detected

bit 2 **SMT1PWAIF:** SMT1 Pulse Width Acquisition Interrupt Flag bit

1 = Interrupt is pending

0 = Interrupt is not pending

bit 1 **SMT1PRAIF:** SMT1 Period Acquisition Interrupt Flag bit

1 = Interrupt is pending

0 = Interrupt is not pending

bit 0 **SMT1IF:** SMT1 Overflow Interrupt Flag bit

1 = An SMT overflow event has occurred (must be cleared in software)

0 = No overflow event detected

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

PIC16(L)F18855/75

REGISTER 11-3: CRCDATH: CRC DATA HIGH BYTE REGISTER

R/W-xx	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x
DAT<15:8>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-0 **DAT<15:8>**: CRC Input/Output Data bits

REGISTER 11-4: CRCDATL: CRC DATA LOW BYTE REGISTER

R/W-xx	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x
DAT<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-0 **DAT<7:0>**: CRC Input/Output Data bits
Writing to this register fills the shifter.

REGISTER 11-5: CRCACCH: CRC ACCUMULATOR HIGH BYTE REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
ACC<15:8>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-0 **ACC<15:8>**: CRC Accumulator Register bits
Writing to this register writes to the CRC accumulator register. Reading from this register reads the CRC accumulator.

REGISTER 11-6: CRCACCL: CRC ACCUMULATOR LOW BYTE REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
ACC<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-0 **ACC<7:0>**: CRC Accumulator Register bits
Writing to this register writes to the CRC accumulator register through the CRC write bus. Reading from this register reads the CRC accumulator.

PIC16(L)F18855/75

12.0 I/O PORTS

TABLE 12-1: PORT AVAILABILITY PER DEVICE

Device	PORTA	PORTB	PORTC	PORTD	PORTE
PIC16(L)F18855	•	•	•		•
PIC16(L)F18875	•	•	•	•	•

Each port has ten standard registers for its operation. These registers are:

- PORTx registers (reads the levels on the pins of the device)
- LATx registers (output latch)
- TRISx registers (data direction)
- ANSELx registers (analog select)
- WPUx registers (weak pull-up)
- CCPx registers (current control positive)
- CCDNx registers (current control negative)
- INLVx (input level control)
- SLRCONx registers (slew rate)
- ODCONx registers (open-drain)

Most port pins share functions with device peripherals, both analog and digital. In general, when a peripheral is enabled on a port pin, that pin cannot be used as a general purpose output; however, the pin can still be read.

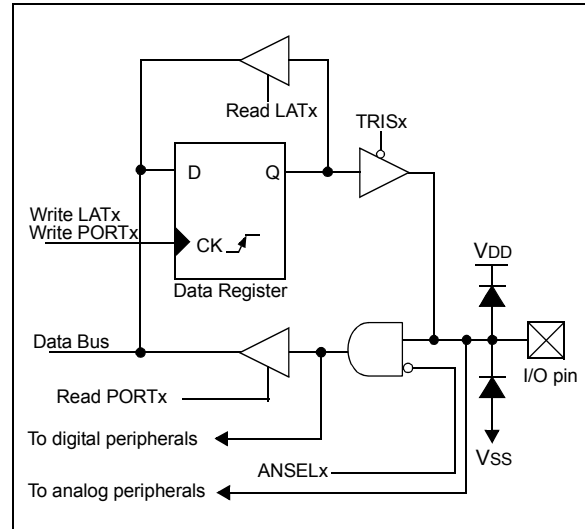
The Data Latch (LATx registers) is useful for read-modify-write operations on the value that the I/O pins are driving.

A write operation to the LATx register has the same effect as a write to the corresponding PORTx register. A read of the LATx register reads of the values held in the I/O PORT latches, while a read of the PORTx register reads the actual I/O pin value.

Ports that support analog inputs have an associated ANSELx register. When an ANSEL bit is set, the digital input buffer associated with that bit is disabled.

Disabling the input buffer prevents analog signal levels on the pin between a logic high and low from causing excessive current in the logic input circuitry. A simplified model of a generic I/O port, without the interfaces to other peripherals, is shown in Figure 12-1.

FIGURE 12-1: GENERIC I/O PORT OPERATION



12.1 Current-Controlled Mode

Current-Controlled mode allows output currents to be regulated for both high-side and low-side drivers. All source and sink drivers for each port pin will operate at the specified current, when enabled individually by the Current-Controlled Enable registers.

Note: Current-Controlled mode is available regardless of which peripheral drives the output.

The Current-Controlled Configuration (CCDCON) register enables the Current-Controlled mode for all ports and sets the current levels.

Note: Setting CCDEN = 1 increases the device VDDIO current requirement by a fixed amount regardless of how many CCPx[n] or CCDNx[n] bits are set.

The Current-Controlled Enable registers enable each individual port pin's positive-going (CCDPx) or negative-going (CCDNx) output driver.

PIC16(L)F18855/75

REGISTER 12-25: ANSEL: PORTC ANALOG SELECT REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
ANSC7	ANSC6	ANSC5	ANSC4	ANSC3	ANSC2	ANSC1	ANSC0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-0

ANSC<7:0>: Analog Select between Analog or Digital Function on Pins RC<7:0>, respectively⁽¹⁾

0 = Digital I/O. Pin is assigned to port or digital special function.

1 = Analog input. Pin is assigned as analog input⁽¹⁾. Digital input buffer disabled.

Note 1: When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

REGISTER 12-26: WPUC: WEAK PULL-UP PORTC REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
WPUC7	WPUC6	WPUC5	WPUC4	WPUC3	WPUC2	WPUC1	WPUC0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-0

WPUC<7:0>: Weak Pull-up Register bits⁽¹⁾

1 = Pull-up enabled

0 = Pull-up disabled

Note 1: The weak pull-up device is automatically disabled if the pin is configured as an output.

12.10.8 CURRENT-CONTROLLED DRIVE MODE CONTROL

The CCDPD and CCDND registers (Register 12-40 and Register 12-41) control the Current-Controlled Drive mode for both the positive-going and negative-going drivers. When a CCDPD[y] or CCDND[y] bit is set and the CCDEN bit of the CCDCON register is set, the Current-Controlled mode is enabled for the corresponding port pin. When the CCDPD[y] or CCDND[y] bit is clear, the Current-Controlled mode for the corresponding port pin is disabled. If the CCDPD[y] or CCDND[y] bit is set and the CCDEN bit is clear, operation of the port pin is undefined (see **Section 12.1.1 “Current-Controlled Drive”** for current-controlled use precautions).

12.10.9 PORTD FUNCTIONS AND OUTPUT PRIORITIES

Each pin defaults to the PORT latch data after Reset. Other output functions are selected with the peripheral pin select logic. See **Section 13.0 “Peripheral Pin Select (PPS) Module”** for more information.

Analog input functions, such as ADC and comparator inputs, are not shown in the peripheral pin select lists. Digital output functions may continue to control the pin when it is in Analog mode.

12.14.8 CURRENT-CONTROLLED DRIVE MODE CONTROL

The CCDPE and CCDNE registers (Register 12-53 and Register 12-54) control the Current-Controlled Drive mode for both the positive-going and negative-going drivers. When a CCDPE[y] or CCDNE[y] bit is set and the CCDEN bit of the CCDCON register is set, the Current-Controlled mode is enabled for the corresponding port pin. When the CCDPE[y] or CCDNE[y] bit is clear, the Current-Controlled mode for the corresponding port pin is disabled. If the CCDPE[y] or CCDNE[y] bit is set and the CCDEN bit is clear, operation of the port pin is undefined (see **Section 12.1.1 “Current-Controlled Drive”** for current-controlled use precautions).

12.14.9 PORTE FUNCTIONS AND OUTPUT PRIORITIES

Each pin defaults to the PORT latch data after Reset. Other output functions are selected with the peripheral pin select logic. See **Section 13.0 “Peripheral Pin Select (PPS) Module”** for more information.

Analog input functions, such as ADC and comparator inputs, are not shown in the peripheral pin select lists. Digital output functions may continue to control the pin when it is in Analog mode.

12.14.10 PORTE FUNCTIONS AND OUTPUT PRIORITIES

Each pin defaults to the PORT latch data after Reset. Other output functions are selected with the peripheral pin select logic. See **Section 13.0 “Peripheral Pin Select (PPS) Module”** for more information.

Analog input functions, such as ADC and comparator inputs, are not shown in the peripheral pin select lists. Digital output functions may continue to control the pin when it is in Analog mode.

PIC16(L)F18855/75

REGISTER 24-3: NCO1ACCL: NCO1 ACCUMULATOR REGISTER – LOW BYTE

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
NCO1ACC<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **NCO1ACC<7:0>**: NCO1 Accumulator, Low Byte

REGISTER 24-4: NCO1ACCH: NCO1 ACCUMULATOR REGISTER – HIGH BYTE

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
NCO1ACC<15:8>							
bit 7				bit 0			

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **NCO1ACC<15:8>**: NCO1 Accumulator, High Byte

REGISTER 24-5: NCO1ACCU: NCO1 ACCUMULATOR REGISTER – UPPER BYTE⁽¹⁾

U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	NCO1ACC<19:16>			
bit 7				bit 0			

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-4 **Unimplemented**: Read as '0'

bit 3-0 **NCO1ACC<19:16>**: NCO1 Accumulator, Upper Byte

Note 1: The accumulator spans registers NCO1ACCU:NCO1ACCH: NCO1ACCL. The 24 bits are reserved but not all are used. This register updates in real-time, asynchronously to the CPU; there is no provision to guarantee atomic access to this 24-bit space using an 8-bit bus. Writing to this register while the module is operating will produce undefined results.

PIC16(L)F18855/75

REGISTER 27-1: T0CON0: TIMER0 CONTROL REGISTER 0

R/W-0/0	U-0	R-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
T0EN	—	T0OUT	T016BIT	T0OUTPS<3:0>			
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7	T0EN: TMR0 Enable bit 1 = The module is enabled and operating 0 = The module is disabled and in the lowest power mode
bit 6	Unimplemented: Read as '0'
bit 5	T0OUT: TMR0 Output bit (read-only) TMR0 output bit
bit 4	T016BIT: TMR0 Operating as 16-bit Timer Select bit 1 = TMR0 is a 16-bit timer 0 = TMR0 is an 8-bit timer
bit 3-0	T0OUTPS<3:0>: TMR0 output postscaler (divider) select bits 1111 = 1:16 Postscaler 1110 = 1:15 Postscaler 1101 = 1:14 Postscaler 1100 = 1:13 Postscaler 1011 = 1:12 Postscaler 1010 = 1:11 Postscaler 1001 = 1:10 Postscaler 1000 = 1:9 Postscaler 0111 = 1:8 Postscaler 0110 = 1:7 Postscaler 0101 = 1:6 Postscaler 0100 = 1:5 Postscaler 0011 = 1:4 Postscaler 0010 = 1:3 Postscaler 0001 = 1:2 Postscaler 0000 = 1:1 Postscaler

31.4 I²C MODE OPERATION

All MSSP I²C communication is byte oriented and shifted out MSb first. Six SFR registers and two interrupt flags interface the module with the PIC[®] microcontroller and user software. Two pins, SDA and SCL, are exercised by the module to communicate with other external I²C devices.

31.4.1 BYTE FORMAT

All communication in I²C is done in 9-bit segments. A byte is sent from a master to a slave or vice-versa, followed by an Acknowledge bit sent back. After the eighth falling edge of the SCL line, the device outputting data on the SDA changes that pin to an input and reads in an acknowledge value on the next clock pulse.

The clock signal, SCL, is provided by the master. Data is valid to change while the SCL signal is low, and sampled on the rising edge of the clock. Changes on the SDA line while the SCL line is high define special conditions on the bus, explained below.

31.4.2 DEFINITION OF I²C TERMINOLOGY

There is language and terminology in the description of I²C communication that have definitions specific to I²C. That word usage is defined below and may be used in the rest of this document without explanation. This table was adapted from the Philips I²C specification.

31.4.3 SDA AND SCL PINS

Selection of any I²C mode with the SSPEN bit set, forces the SCL and SDA pins to be open-drain. These pins should be set by the user to inputs by setting the appropriate TRIS bits.

Note 1: Data is tied to output zero when an I²C mode is enabled.

2: Any device pin can be selected for SDA and SCL functions with the PPS peripheral. These functions are bidirectional. The SDA input is selected with the SSPDATPPS registers. The SCL input is selected with the SSPCLKPPS registers. Outputs are selected with the RxyPPS registers. It is the user's responsibility to make the selections so that both the input and the output for each function is on the same pin.

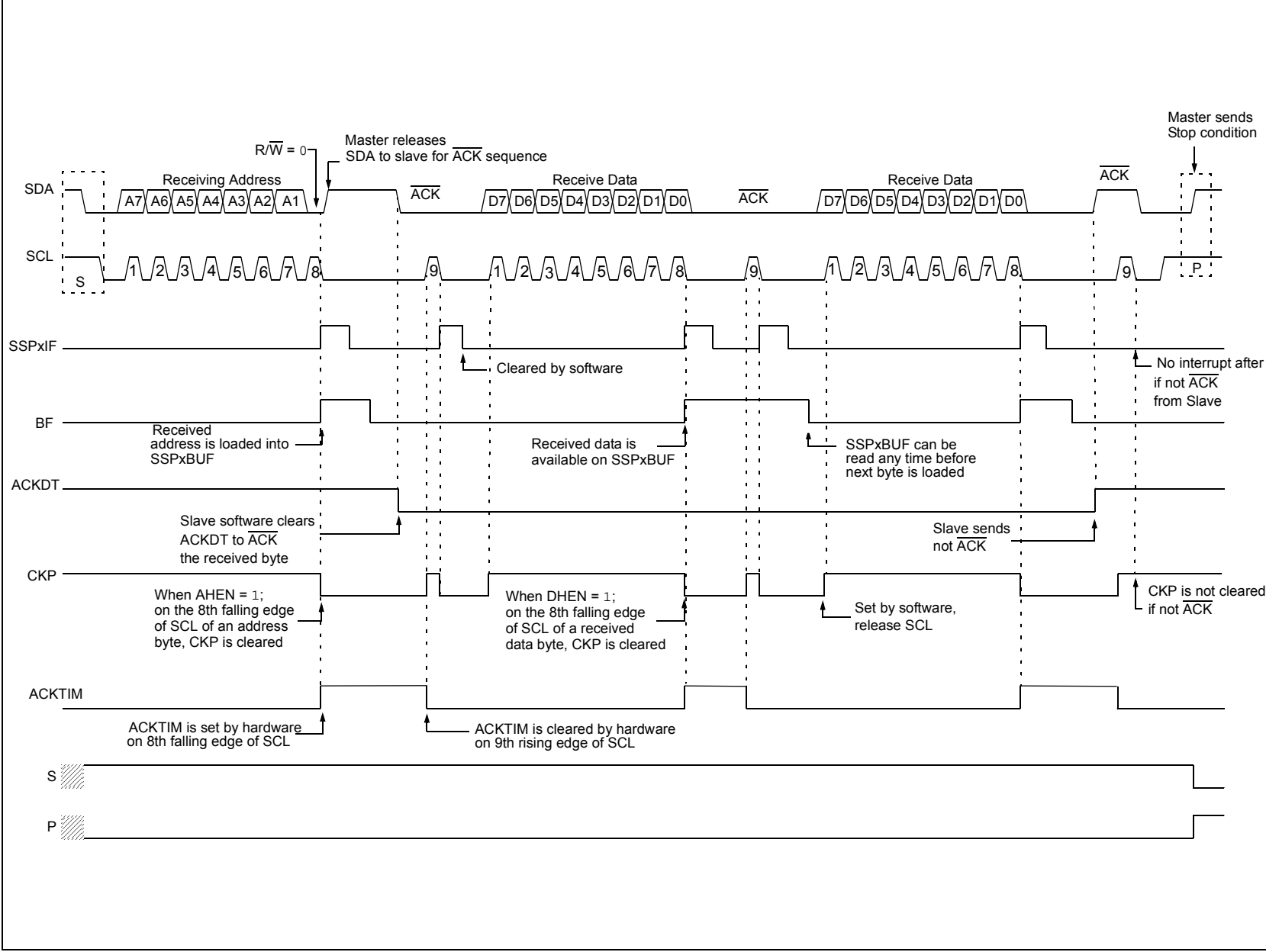
31.4.4 SDA HOLD TIME

The hold time of the SDA pin is selected by the SDAHT bit of the SSPxCON3 register. Hold time is the time SDA is held valid after the falling edge of SCL. Setting the SDAHT bit selects a longer 300 ns minimum hold time and may help on buses with large capacitance.

TABLE 31-1: I²C BUS TERMS

TERM	Description
Transmitter	The device which shifts data out onto the bus.
Receiver	The device which shifts data in from the bus.
Master	The device that initiates a transfer, generates clock signals and terminates a transfer.
Slave	The device addressed by the master.
Multi-master	A bus with more than one device that can initiate data transfers.
Arbitration	Procedure to ensure that only one master at a time controls the bus. Winning arbitration ensures that the message is not corrupted.
Synchronization	Procedure to synchronize the clocks of two or more devices on the bus.
Idle	No master is controlling the bus, and both SDA and SCL lines are high.
Active	Any time one or more master devices are controlling the bus.
Addressed Slave	Slave device that has received a matching address and is actively being clocked by a master.
Matching Address	Address byte that is clocked into a slave that matches the value stored in SSPxADD.
Write Request	Slave receives a matching address with R/W bit clear, and is ready to clock in data.
Read Request	Master sends an address byte with the R/W bit set, indicating that it wishes to clock data out of the Slave. This data is the next and all following bytes until a Restart or Stop.
Clock Stretching	When a device on the bus hold SCL low to stall communication.
Bus Collision	Any time the SDA line is sampled low by the module while it is outputting and expected high state.

FIGURE 31-17: I²C SLAVE, 7-BIT ADDRESS, RECEPTION (SEN = 1, AHEN = 1, DHEN = 1)



PIC16(L)F18855/75

37.0 ELECTRICAL SPECIFICATIONS

37.1 Absolute Maximum Ratings^(†)

Ambient temperature under bias	-40°C to +125°C
Storage temperature	-65°C to +150°C
Voltage on pins with respect to V _{SS}	
on V _{DD} pin	
PIC16F18855/75	-0.3V to +6.5V
PIC16LF18855/75	-0.3V to +4.0V
on MCLR pin	-0.3V to +9.0V
on all other pins	-0.3V to (V _{DD} + 0.3V)
Maximum current	
on V _{SS} pin ⁽¹⁾	
-40°C ≤ T _A ≤ +85°C	350 mA
85°C < T _A ≤ +125°C	120 mA
on V _{DD} pin for 28-Pin devices ⁽¹⁾	
-40°C ≤ T _A ≤ +85°C	250 mA
85°C < T _A ≤ +125°C	85 mA
on V _{DD} pin for 40-Pin devices ⁽¹⁾	
-40°C ≤ T _A ≤ +85°C	350 mA
85°C < T _A ≤ +125°C	120 mA
on any standard I/O pin	±50 mA
Clamp current, I _K (V _{PIN} < 0 or V _{PIN} > V _{DD})	±20 mA
Total power dissipation ⁽²⁾	800 mW

Note 1: Maximum current rating requires even load distribution across I/O pins. Maximum current rating may be limited by the device package power dissipation characterizations, see Table 37-6 to calculate device specifications.

2: Power dissipation is calculated as follows:

$$P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OI} \times I_{OL})$$

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

PIC16(L)F18855/75

TABLE 37-11: RESET, WDT, OSCILLATOR START-UP TIMER, POWER-UP TIMER, BROWN-OUT RESET AND LOW-POWER BROWN-OUT RESET SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated)							
Param. No.	Sym.	Characteristic	Min.	Typ†	Max.	Units	Conditions
RST01*	TMCLR	MCLR Pulse Width Low to ensure Reset	2	—	—	μs	
RST02*	TIOZ	I/O high-impedance from Reset detection	—	—	2	μs	
RST03	TWDT	Watchdog Timer Time-out Period	—	16	—	ms	16 ms Nominal Reset Time
RST04*	TPWRT	Power-up Timer Period	—	65	—	ms	
RST05	TOST	Oscillator Start-up Timer Period ^(1,2)	—	1024	—	T _{OSC}	
RST06	VBOR	Brown-out Reset Voltage ⁽⁴⁾	2.55	2.70	2.85	V	BORV = 0
			2.30	2.45	2.60	V	BORV = 1 (PIC16F18855/75)
			1.80	1.90	2.10	V	BORV = 1 (PIC16LF18855/75)
RST07	VBORHYS	Brown-out Reset Hysteresis	—	40	—	mV	
RST08	TBORDC	Brown-out Reset Response Time	—	3	—	μs	
RST09	VLPBOR	Low-Power Brown-out Reset Voltage	2.3	2.45	2.7	V	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: By design, the Oscillator Start-up Timer (OST) counts the first 1024 cycles, independent of frequency.

Note 2: To ensure these voltage tolerances, V_{DD} and V_{SS} must be capacitively decoupled as close to the device as possible. 0.1 μF and 0.01 μF values in parallel are recommended.

TABLE 37-12: ANALOG-TO-DIGITAL CONVERTER (ADC) ACCURACY SPECIFICATIONS^(1,2):

Operating Conditions (unless otherwise stated) V _{DD} = 3.0V, T _A = 25°C							
Param. No.	Sym.	Characteristic	Min.	Typ†	Max.	Units	Conditions
AD01	NR	Resolution	—	—	10	bit	
AD02	EIL	Integral Error	—	±0.1	±1.0	LSb	ADCREf+ = 3.0V, ADCREf- = 0V
AD03	EDL	Differential Error	—	±0.1	±1.0	LSb	ADCREf+ = 3.0V, ADCREf- = 0V
AD04	EOFF	Offset Error	—	0.5	2.0	LSb	ADCREf+ = 3.0V, ADCREf- = 0V
AD05	EGN	Gain Error	—	±0.2	±1.0	LSb	ADCREf+ = 3.0V, ADCREf- = 0V
AD06	VADREF	ADC Reference Voltage (ADREF+ - ADREF-)	1.8	—	V _{DD}	V	
AD07	VAIN	Full-Scale Range	ADREF-	—	ADREF+	V	
AD08	ZAIN	Recommended Impedance of Analog Voltage Source	—	10	—	kΩ	
AD09	RVREF	ADC Voltage Reference Ladder Impedance	—	50	—	kΩ	Note 3

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Total Absolute Error is the sum of the offset, gain and integral non-linearity (INL) errors.

Note 2: The ADC conversion result never decreases with an increase in the input and has no missing codes.

Note 3: This is the impedance seen by the VREF pads when the external reference pads are selected.