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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 35x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f18875t-i-pt

1.1 Register and Bit naming conventions

1.1.1 REGISTER NAMES

When there are multiple instances of the same peripheral in a device, the peripheral control registers will be depicted as the concatenation of a peripheral identifier, peripheral instance, and control identifier. The control registers section will show just one instance of all the register names with an 'x' in the place of the peripheral instance number. This naming convention may also be applied to peripherals when there is only one instance of that peripheral in the device to maintain compatibility with other devices in the family that contain more than one.

1.1.2 BIT NAMES

There are two variants for bit names:

- Short name: Bit function abbreviation
- Long name: Peripheral abbreviation + short name

1.1.2.1 Short Bit Names

Short bit names are an abbreviation for the bit function. For example, some peripherals are enabled with the EN bit. The bit names shown in the registers are the short name variant.

Short bit names are useful when accessing bits in C programs. The general format for accessing bits by the short name is *RegisterNamebits.ShortName*. For example, the enable bit, EN, in the COG1CON0 register can be set in C programs with the instruction `COG1CON0bits.EN = 1`.

Short names are generally not useful in assembly programs because the same name may be used by different peripherals in different bit positions. When this occurs, during the include file generation, all instances of that short bit name are appended with an underscore plus the name of the register in which the bit resides to avoid naming contentions.

1.1.2.2 Long Bit Names

Long bit names are constructed by adding a peripheral abbreviation prefix to the short name. The prefix is unique to the peripheral thereby making every long bit name unique. The long bit name for the COG1 enable bit is the COG1 prefix, G1, appended with the enable bit short name, EN, resulting in the unique bit name G1EN.

Long bit names are useful in both C and assembly programs. For example, in C the COG1CON0 enable bit can be set with the `G1EN = 1` instruction. In assembly, this bit can be set with the `BSF COG1CON0,G1EN` instruction.

1.1.2.3 Bit Fields

Bit fields are two or more adjacent bits in the same register. Bit fields adhere only to the short bit naming convention. For example, the three Least Significant bits of the COG1CON0 register contain the mode control bits. The short name for this field is MD. There is no long bit name variant. Bit field access is only possible in C programs. The following example demonstrates a C program instruction for setting the COG1 to the Push-Pull mode:

```
COG1CON0bits.MD = 0x5;
```

Individual bits in a bit field can also be accessed with long and short bit names. Each bit is the field name appended with the number of the bit position within the field. For example, the Most Significant mode bit has the short bit name MD2 and the long bit name is G1MD2. The following two examples demonstrate assembly program sequences for setting the COG1 to Push-Pull mode:

Example 1:

```
MOVLW ~(1<<G1MD1)
ANDWF COG1CON0,F
MOVLW 1<<G1MD2 | 1<<G1MD0
IORWF COG1CON0,F
```

Example 2:

```
BSF COG1CON0,G1MD2
BCF COG1CON0,G1MD1
BSF COG1CON0,G1MD0
```

1.1.3 REGISTER AND BIT NAMING EXCEPTIONS

1.1.3.1 Status, Interrupt, and Mirror Bits

Status, interrupt enables, interrupt flags, and mirror bits are contained in registers that span more than one peripheral. In these cases, the bit name shown is unique so there is no prefix or short name variant.

1.1.3.2 Legacy Peripherals

There are some peripherals that do not strictly adhere to these naming conventions. Peripherals that have existed for many years and are present in almost every device are the exceptions. These exceptions were necessary to limit the adverse impact of the new conventions on legacy code. Peripherals that do adhere to the new convention will include a table in the registers section indicating the long name prefix for each peripheral instance. Peripherals that fall into the exception category will not have this table. These peripherals include, but are not limited to, the following:

- EUSART
- MSSP

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TABLE 1-3: PIC16F18875 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC6/ANC6/CK ⁽³⁾ /IOCC6	RC6	TTL/ST	CMOS/OD	General purpose I/O.
	ANC6	AN	—	ADC Channel C6 input.
	CK ⁽³⁾	TTL/ST	CMOS/OD	EUSART synchronous mode clock input/output.
	IOCC6	TTL/ST	—	Interrupt-on-change input.
RC7/ANC7/RX ⁽¹⁾ /DT ⁽³⁾ /IOCC7	RC7	TTL/ST	CMOS/OD	General purpose I/O.
	ANC7	AN	—	ADC Channel C7 input.
	RX ⁽¹⁾	TTL/ST	—	EUSART Asynchronous mode receiver data input.
	DT ⁽³⁾	TTL/ST	CMOS/OD	EUSART Synchronous mode data input/output.
	IOCC7	TTL/ST	—	Interrupt-on-change input.
RD0	RD0	TTL/ST	CMOS/OD	General purpose I/O.
	AND0	AN	—	ADC Channel D0 input.
RD1	RD1	TTL/ST	CMOS/OD	General purpose I/O.
	AND1	AN	—	ADC Channel D1 input.
RD2	RD2	TTL/ST	CMOS/OD	General purpose I/O.
	AND2	AN	—	ADC Channel D2 input.
RD3	RD3	TTL/ST	CMOS/OD	General purpose I/O.
	AND3	AN	—	ADC Channel D3 input.
RD4	RD4	TTL/ST	CMOS/OD	General purpose I/O.
	AND4	AN	—	ADC Channel D4 input.
RD5	RD5	TTL/ST	CMOS/OD	General purpose I/O.
	AND5	AN	—	ADC Channel D5 input.
RD6	RD6	TTL/ST	CMOS/OD	General purpose I/O.
	AND6	AN	—	ADC Channel D6 input.
RD7	RD7	TTL/ST	CMOS/OD	General purpose I/O.
	AND7	AN	—	ADC Channel D7 input.
RE0	RE0	TTL/ST	CMOS/OD	General purpose I/O.
	ANE0	AN	—	ADC Channel E0 input.
RE1	RE1	TTL/ST	CMOS/OD	General purpose I/O.
	ANE1	AN	—	ADC Channel E1 input.
RE2	RE2	TTL/ST	CMOS/OD	General purpose I/O.
	ANE2	AN	—	ADC Channel E2 input.
RE3/IOCE3/ $\overline{\text{MCLR}}$ /VPP	RE3	TTL/ST	—	General purpose input-only (when $\overline{\text{MCLR}}$ is disabled by config bit).
	IOCE3	TTL/ST	—	Interrupt-on-change input.
	$\overline{\text{MCLR}}$	ST	—	Master clear input with internal weak pull-up resistor.
	VPP	HV	—	ICSP™ high voltage programming mode entry input.
VDD	VDD	Power	—	Positive supply voltage input.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I²C = Schmitt Trigger input with I²CHV=
High Voltage XTAL= Crystal levels

- Note**
- 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 13-1 for details on which PORT pins may be used for this signal.
 - 2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 13-3.
 - 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
 - 4: These pins are configured for I²C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I²C specific or SMBus input buffer thresholds.

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REGISTER 4-2: CONFIG2: CONFIGURATION WORD 2: SUPERVISORS

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	U-1
<u>DEBUG</u>	STVREN	PPS1WAY	ZCDDIS	BORV	—
bit 13					bit 8

R/P-1	R/P-1	R/P-1	U-1	U-1	U-1	R/P-1	R/P-1
BOREN<1:0>	<u>LPBOREN</u>	—	—	—	—	<u>PWRT</u>	MCLRE
bit 7							bit 0

Legend:

R = Readable bit

P = Programmable bit

U = Unimplemented bit, read as '1'

'0' = Bit is cleared

'1' = Bit is set

n = Value when blank or after Bulk Erase

- bit 13 **DEBUG:** Debugger Enable bit⁽²⁾
 1 = OFF Background debugger disabled; ICSPCLK and ICSPDAT are general purpose I/O pins
 0 = ON Background debugger enabled; ICSPCLK and ICSPDAT are dedicated to the debugger
- bit 12 **STVREN:** Stack Overflow/Underflow Reset Enable bit
 1 = ON Stack Overflow or Underflow will cause a Reset
 0 = OFF Stack Overflow or Underflow will not cause a Reset
- bit 11 **PPS1WAY:** PPSLOCKED One-Way Set Enable bit
 1 = ON The PPSLOCKED bit can be cleared and set only once; PPS registers remain locked after one clear/set cycle
 0 = OFF The PPSLOCKED bit can be set and cleared repeatedly (subject to the unlock sequence)
- bit 10 **ZCDDIS:** Zero-Cross Detect Disable bit
 1 = ON ZCD disabled. ZCD can be enabled by setting the EN bit of the ZCDxCON register
 0 = OFF ZCD always enabled (EN bit is ignored)
- bit 9 **BORV:** Brown-out Reset Voltage Selection bit⁽¹⁾
 1 = LOW Brown-out Reset voltage (VBOR) set to lower trip point level
 0 = HIGH Brown-out Reset voltage (VBOR) set to higher trip point level
 The higher voltage setting is recommended for operation at or above 16 MHz.
- bit 8 **Unimplemented:** Read as '1'
- bit 7-6 **BOREN<1:0>:** Brown-out Reset Enable bits
 When enabled, Brown-out Reset Voltage (VBOR) is set by the BORV bit
 11 = ON Brown-out Reset is enabled; SBORV bit is ignored
 10 = SLEEP Brown-out Reset is enabled while running, disabled in Sleep; SBORV bit is ignored
 01 = SBORV Brown-out Reset is enabled according to SBORV
 00 = OFF Brown-out Reset is disabled
- bit 5 **LPBOREN:** Low-power BOR enable bit
 1 = LPBOR disabled
 0 = LPBOR enabled
- bit 4-2 **Unimplemented:** Read as '1'
- bit 1 **PWRT:** Power-up Timer Enable bit
 1 = OFF PWRT is disabled
 0 = ON PWRT is enabled
- bit 0 **MCLRE:** Master Clear (MCLR) Enable bit
 If LVP = 1:
 RA3 pin function is MCLR.
 If LVP = 0:
 1 = ON MCLR pin is MCLR.
 0 = OFF MCLR pin function is port-defined function.

- Note** 1: See VBOR parameter for specific trip point voltages.
 2: The DEBUG bit in Configuration Words is managed automatically by device development tools including debuggers and programmers. For normal device operation, this bit should be maintained as a '1'.

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REGISTER 6-4: OSCSTAT: OSCILLATOR STATUS REGISTER 1

R-q/q	R-0/q	R-0/q	R-0/q	R-q/q	R-q/q	U-0	R-q/q
EXTOR	HFOR	MFOR	LFOR	SOR	ADOR	—	PLLr
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7	EXTOR: EXTOSC (external) Oscillator Ready bit 1 = The oscillator is ready to be used 0 = The oscillator is not enabled, or is not yet ready to be used.
bit 6	HFOR: HFINTOSC Oscillator Ready bit 1 = The oscillator is ready to be used 0 = The oscillator is not enabled, or is not yet ready to be used.
bit 5	MFOR: MFINTOSC Oscillator Ready bit 1 = The oscillator is ready to be used 0 = The oscillator is not enabled, or is not yet ready to be used
bit 4	LFOR: LFINTOSC Oscillator Ready bit 1 = The oscillator is ready to be used 0 = The oscillator is not enabled, or is not yet ready to be used.
bit 3	SOR: Secondary (Timer1) Oscillator Ready bit 1 = The oscillator is ready to be used 0 = The oscillator is not enabled, or is not yet ready to be used.
bit 2	ADOR: CRC Oscillator Ready bit 1 = The oscillator is ready to be used 0 = The oscillator is not enabled, or is not yet ready to be used
bit 1	Unimplemented: Read as '0'
bit 0	PLLr: PLL is Ready bit 1 = The PLL is ready to be used 0 = The PLL is not enabled, the required input source is not ready, or the PLL is not locked.

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REGISTER 6-6: OSCFRQ: HFINTOSC FREQUENCY SELECTION REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-q/q	R/W-q/q	R/W-q/q
—	—	—	—	—	HFFRQ<2:0> ⁽¹⁾		
bit 7					bit 0		

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-3

Unimplemented: Read as '0'

bit 2-0

HFFRQ<2:0>: HFINTOSC Frequency Selection bits

Nominal Freq (MHz) (NOSC = 110):

111 = Reserved

110 = 32

101 = 16

100 = 12

011 = 8

010 = 4

001 = 2

000 = 1

Note 1: When RSTOSC=110 (HFINTOSC 1 MHz), the HFFRQ bits will default to '010' upon Reset; when RSTOSC = 000 (HFINTOSC 32 MHz), the HFFRQ bits will default to '110' upon Reset.

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REGISTER 12-34: LATD: PORTD TRI-STATE REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-0 **LATD<7:0>**: LATD I/O Value bits⁽¹⁾

1 = Port pin is $\geq V_{IH}$

0 = Port pin is $\leq V_{IL}$

Note 1: Writes to LATD are actually written to corresponding LATD register. Reads from PORTD register is return of actual I/O pin values.

REGISTER 12-35: ANSEL: PORTD TRI-STATE REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
ANSD7	ANSD6	ANSD5	ANSD4	ANSD3	ANSD2	ANSD1	ANSD0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-0 **ANSD<7:0>**: ANSD I/O Value bits⁽¹⁾

1 = Port pin is $\geq V_{IH}$

0 = Port pin is $\leq V_{IL}$

Note 1: When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.0

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REGISTER 12-47: LATE: PORTE DATA LATCH REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u
—	—	—	—	—	LATE2	LATE1	LATE0
bit 7					bit 0		

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **LATE<2:0>:** PORTE Output Latch Value bits⁽¹⁾

Note 1: Writes to PORTE are actually written to the corresponding LATE register. Reads from the PORTE register is return of actual I/O pin values.

REGISTER 12-48: ANSELE: PORTE ANALOG SELECT REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-1/1	R/W-1/1	R/W-1/1
—	—	—	—	—	ANSE2	ANSE1	ANSE0
bit 7					bit 0		

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **ANSE<2:0>:** Analog Select between Analog or Digital Function on pins RE<2:0>, respectively
0 = Digital I/O. Pin is assigned to port or digital special function.
1 = Analog input. Pin is assigned as analog input⁽¹⁾. Digital input buffer disabled.

Note 1: When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

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REGISTER 12-53: CCDPE: CURRENT CONTROL DRIVE NEGATIVE PORTE REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	—	CCDPE2	CCDPE1	CCDPE0
bit 7					bit 0		

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **CCDPE<2:0>:** RE<2:0> Current Control Drive Positive Control bits⁽¹⁾

1 = Current control source enabled

0 = Current control source disabled

Note 1: If CCDPEy is set, when CCDEN = 0 (Register 12-1), operation of the pin is undefined.

REGISTER 12-54: CCDNE: CURRENT CONTROL DRIVE NEGATIVE PORTE REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	—	CCDNE2	CCDNE1	CCDNE0
bit 7					bit 0		

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **CCDNE<2:0>:** RE<2:0> Current Control Drive Negative Control bits⁽¹⁾

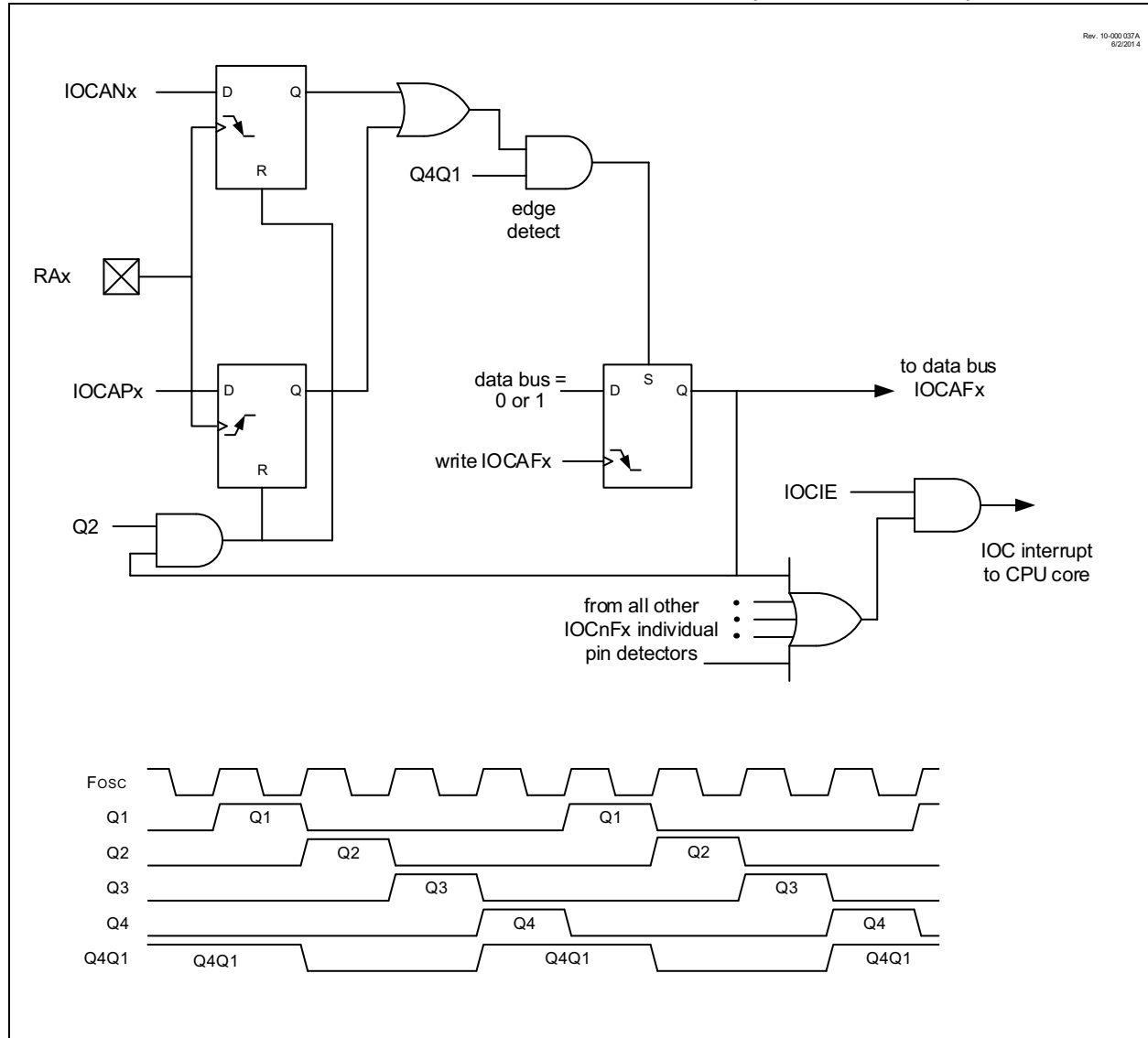
1 = Current control source enabled

0 = Current control source disabled

Note 1: If CCDNEy is set, when CCDEN = 0 (Register 12-1), operation of the pin is undefined.

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FIGURE 15-1: INTERRUPT-ON-CHANGE BLOCK DIAGRAM (PORTA EXAMPLE)



18.2 Comparator Control

Each comparator has two control registers: CMxCON0 and CMxCON1.

The CMxCON0 register (see Register 18-1) contains Control and Status bits for the following:

- Enable
- Output
- Output polarity
- Speed/Power selection
- Hysteresis enable
- Timer1 output synchronization

The CMxCON1 register (see Register 18-2) contains Control bits for the following:

- Interrupt on positive/negative edge enables
- Positive input channel selection
- Negative input channel selection

18.2.1 COMPARATOR ENABLE

Setting the CxON bit of the CMxCON0 register enables the comparator for operation. Clearing the CxON bit disables the comparator resulting in minimum current consumption.

18.2.2 COMPARATOR OUTPUT

The output of the comparator can be monitored by reading either the CxOUT bit of the CMxCON0 register or the MCxOUT bit of the CMOUT register.

The comparator output can also be routed to an external pin through the RxyPPS register (Register 13-2). The corresponding TRIS bit must be clear to enable the pin as an output.

Note 1: The internal output of the comparator is latched with each instruction cycle. Unless otherwise specified, external outputs are not latched.

18.2.3 COMPARATOR OUTPUT POLARITY

Inverting the output of the comparator is functionally equivalent to swapping the comparator inputs. The polarity of the comparator output can be inverted by setting the CxPOL bit of the CMxCON0 register. Clearing the CxPOL bit results in a non-inverted output.

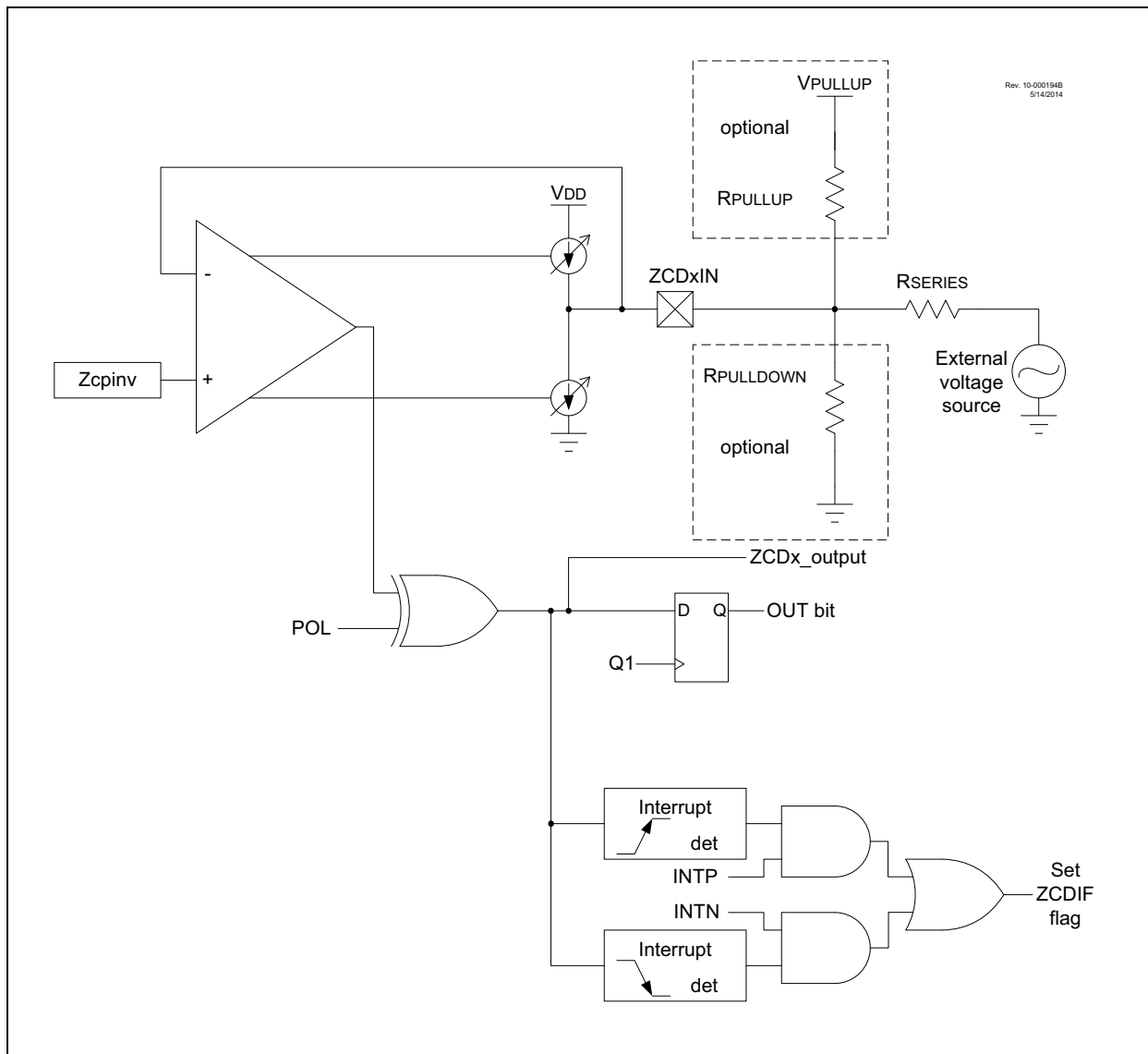
Table 18-2 shows the output state versus input conditions, including polarity control.

TABLE 18-2: COMPARATOR OUTPUT STATE VS. INPUT CONDITIONS

Input Condition	CxPOL	CxOUT
$CxV_N > CxV_P$	0	0
$CxV_N < CxV_P$	0	1
$CxV_N > CxV_P$	1	1
$CxV_N < CxV_P$	1	0

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FIGURE 21-2: SIMPLIFIED ZCD BLOCK DIAGRAM



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TABLE 23-1: ADC CLOCK PERIOD (T_{AD}) Vs. DEVICE OPERATING FREQUENCIES

ADC Clock Period (T _{AD})		Device Frequency (F _{osc})					
ADC Clock Source	ADCCS<5:0>	32 MHz	20 MHz	16 MHz	8 MHz	4 MHz	1 MHz
Fosc/2	000000	62.5ns ⁽²⁾	100 ns ⁽²⁾	125 ns ⁽²⁾	250 ns ⁽²⁾	500 ns ⁽²⁾	2.0 μs
Fosc/4	000001	125 ns ⁽²⁾	200 ns ⁽²⁾	250 ns ⁽²⁾	500 ns ⁽²⁾	1.0 μs	4.0 μs
Fosc/6	000010	187.5 ns ⁽²⁾	300 ns ⁽²⁾	375 ns ⁽²⁾	750 ns ⁽²⁾	1.5 μs	6.0 μs
Fosc/8	000011	250 μs ⁽²⁾	400 ns ⁽²⁾	500 μs ⁽²⁾	1.0 μs	2.0 μs	8.0 μs ⁽³⁾
...
Fosc/16	000111	500 ns ⁽²⁾	800 ns ⁽²⁾	1.0 μs	2.0 μs	4.0 μs	16.0 μs ⁽²⁾
...
Fosc/128	111111	4.0 μs	6.4 μs	8.0 μs	16.0 μs ⁽³⁾	32.0 μs ⁽²⁾	128.0 μs ⁽²⁾
FRC	ADCS(ADCON0<4>)=1	1.0-6.0 μs ⁽¹⁾	1.0-6.0 μs ⁽¹⁾	1.0-6.0 μs ⁽¹⁾	1.0-6.0 μs ⁽¹⁾	1.0-6.0 μs ⁽¹⁾	1.0-6.0 μs ⁽¹⁾

Legend: Shaded cells are outside of recommended range.

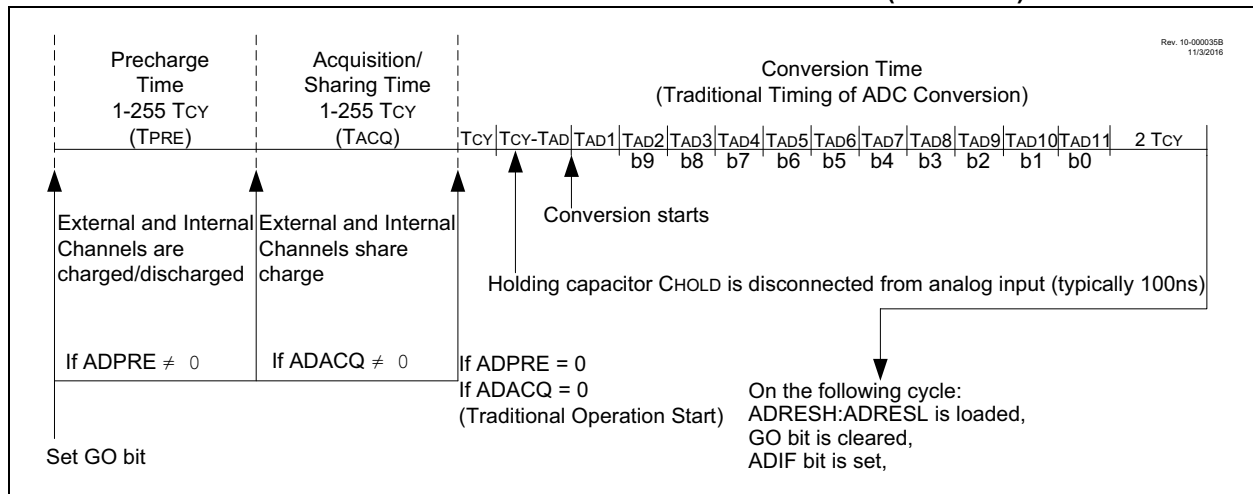
Note 1: See T_{AD} parameter for FRC source typical T_{AD} value.

2: These values violate the required T_{AD} time.

3: Outside the recommended T_{AD} time.

4: The ADC clock period (T_{AD}) and total ADC conversion time can be minimized when the ADC clock is derived from the system clock Fosc. However, the FRC oscillator source must be used when conversions are to be performed with the device in Sleep mode.

FIGURE 23-2: ANALOG-TO-DIGITAL CONVERSION T_{AD} CYCLES (ADSC = 0)



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REGISTER 23-4: ADCON3: ADC THRESHOLD REGISTER

U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W/HC-0	R/W-0/0	R/W-0/0	R/W-0/0
—	ADCALC<2:0>			ADSOI	ADTMD<2:0>		
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

HC = Bit is cleared by hardware

bit 7

Unimplemented: Read as '0'

bit 6-4

ADCALC<2:0>: ADC Error Calculation Mode Select bits

ADCALC	Action During 1st Precharge Stage		Application
	ADDSEN = 0 Single-Sample Mode	ADDSEN = 1 CVD Double-Sample Mode ⁽¹⁾	
111	Reserved	Reserved	Reserved
110	Reserved	Reserved	Reserved
101	ADFLTR-ADSTPT	ADFLTR-ADSTPT	Average/filtered value vs. setpoint
100	ADPREV-ADFLTR	ADPREV-ADFLTR	First derivative of filtered value ⁽³⁾ (negative)
011	Reserved	Reserved	Reserved
010	ADRES-ADFLTR	(ADRES-ADPREV)-ADFLTR	Actual result vs. averaged/filtered value
001	ADRES-ADSTPT	(ADRES-ADPREV)-ADSTPT	Actual result vs. setpoint
000	ADRES-ADPREV	ADRES-ADPREV	First derivative of single measurement ⁽²⁾
			Actual CVD result in CVD mode ⁽²⁾

bit 3

ADSOI: ADC Stop-on-Interrupt bit

If ADCONT = 1:

1 = ADGO is cleared when the threshold conditions are met, otherwise the conversion is retriggered

0 = ADGO is not cleared by hardware, must be cleared by software to stop retriggers

If ADCONT = 0 bit is ignored.

bit 2-0

ADTMD<2:0>: Threshold Interrupt Mode Select bits

111 = Always set ADTIF at end of calculation

110 = Set ADTIF if ADERR>ADUTH

101 = Set ADTIF if ADERR≤ADUTH

100 = Set ADTIF if ADERR<ADLTH or ADERR>ADUTH

011 = Set ADTIF if ADERR>ADLTH and ADERR<ADUTH

010 = Set ADTIF if ADERR≥ADLTH

001 = Set ADTIF if ADERR<ADLTH

000 = ADTIF is disabled

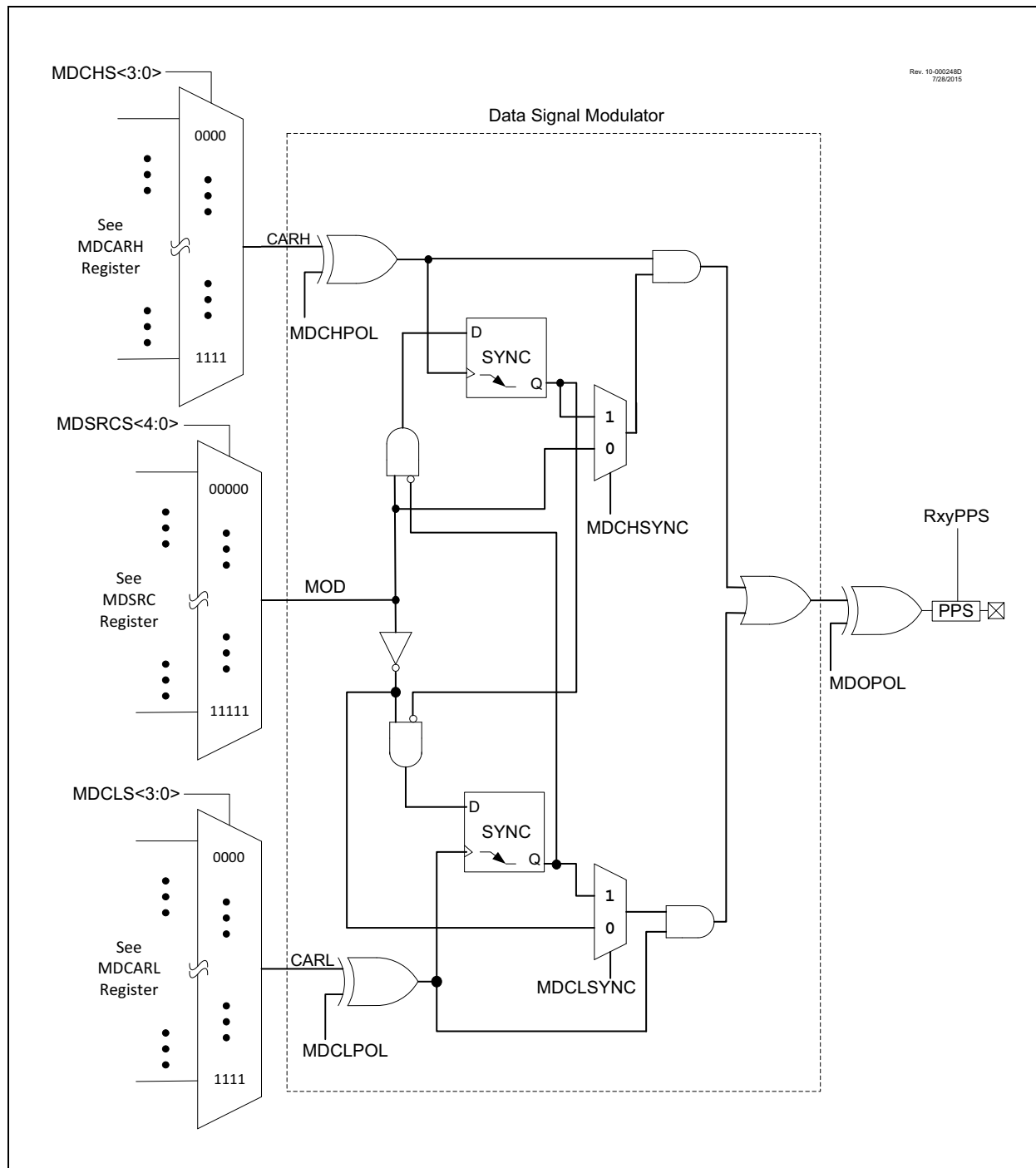
Note 1: When ADPSIS = 0, the value of (ADRES-ADPREV) is the value of (S2-S1) from Table 23-3.

2: When ADPSIS = 0

3: When ADPSIS = 1.

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FIGURE 26-1: SIMPLIFIED BLOCK DIAGRAM OF THE DATA SIGNAL MODULATOR



26.1 DSM Operation

The DSM module can be enabled by setting the MDEN bit in the MDCON register. Clearing the MDEN bit in the MDCON register, disables the DSM module by automatically switching the carrier high and carrier low signals to the Vss signal source. The modulator signal source is also switched to the MDBIT in the MDCON register. This not only assures that the DSM module is inactive, but that it is also consuming the least amount of current.

The values used to select the carrier high, carrier low, and modulator sources held by the Modulation Source, Modulation High Carrier, and Modulation Low Carrier control registers are not affected when the MDEN bit is cleared and the DSM module is disabled. The values inside these registers remain unchanged while the DSM is inactive. The sources for the carrier high, carrier low and modulator signals will once again be selected when the MDEN bit is set and the DSM module is again enabled and active.

The modulated output signal can be disabled without shutting down the DSM module. The DSM module will remain active and continue to mix signals, but the output value will not be sent to the DSM pin. During the time that the output is disabled, the DSM pin will remain low. The modulated output can be disabled by clearing the MDEN bit in the MDCON register.

26.2 Modulator Signal Sources

The modulator signal can be supplied from the following sources:

- External Signal on MDSRCPPS pin
- MDBIT bit in the MDCON0 register
- CCP1 Signal
- CCP2 Signal
- CCP3 Signal
- CCP4 Signal
- CCP5 Signal
- PWM6 Signal
- PWM7 Signal
- NCO output
- Comparator C1 Signal
- Comparator C2 Signal
- CLC1 Output
- CLC2 Output
- CLC3 Output
- CLC4 Output
- EUSART DT Signal
- EUSART TX/CK Signal
- MSSP1 SDO Signal (SPI Mode Only)
- MSSP2 SDO Signal

The modulator signal is selected by configuring the MDMS <4:0> bits in the MDSRC register.

26.3 Carrier Signal Sources

The carrier high signal and carrier low signal can be supplied from the following sources:

- External Signal on MDCARH/LPPS pins
- FOSC (system clock)
- HFINTOSC
- Reference Clock Module Signal
- CCP1 Signal
- CCP2 Signal
- CCP3 Signal
- CCP4 Signal
- CCP5 Signal
- PWM6 Output
- PWM7 Output
- NCO output
- CLC1 output
- CLC2 output
- CLC3 output
- CLC4 output

The carrier high signal is selected by configuring the MDCHS <3:0> bits in the MDCARH register. The carrier low signal is selected by configuring the MDCLS <3:0> bits in the MDCARL register.

26.4 Carrier Synchronization

During the time when the DSM switches between carrier high and carrier low signal sources, the carrier data in the modulated output signal can become truncated. To prevent this, the carrier signal can be synchronized to the modulator signal. When synchronization is enabled, the carrier pulse that is being mixed at the time of the transition is allowed to transition low before the DSM switches over to the next carrier source.

Synchronization is enabled separately for the carrier high and carrier low signal sources. Synchronization for the carrier high signal is enabled by setting the MDCHSYNC bit in the MDCON1 register. Synchronization for the carrier low signal is enabled by setting the MDCLSYNC bit in the MDCON1 register.

Figure 26-1 through Figure 26-6 show timing diagrams of using various synchronization methods.

29.5.10 LEVEL-TRIGGERED HARDWARE LIMIT ONE-SHOT MODES

The Level-Triggered Hardware Limit One-Shot modes hold the timer in Reset on an external Reset level and start counting when both the ON bit is set and the external signal is not at the Reset level. If one of either the external signal is not in Reset or the ON bit is set then the other signal being set/made active will start the timer. Reset levels are selected as follows:

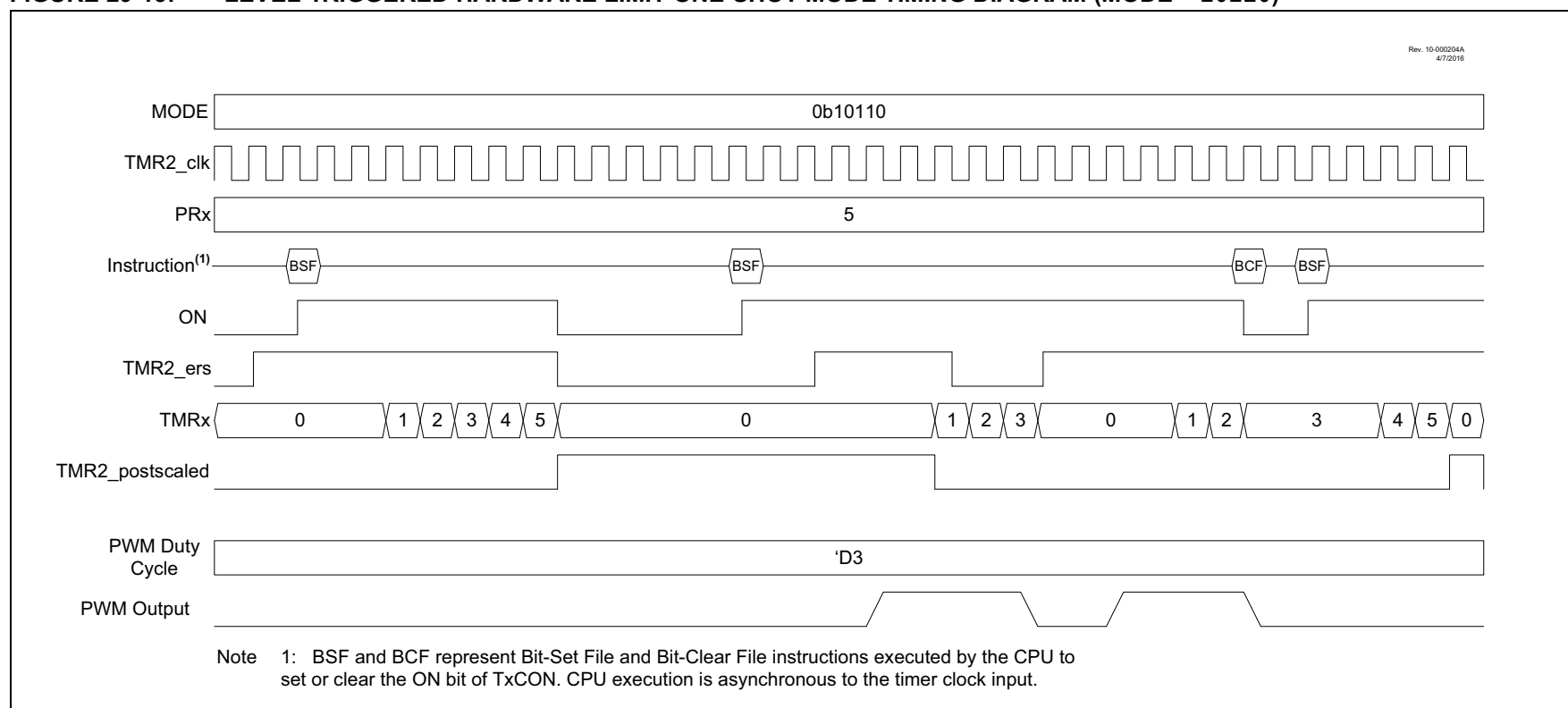
- Low Reset level (MODE<4:0> = 10110)

- High Reset level (MODE<4:0> = 10111)

When the timer count matches the PRx period count, the timer is reset and the ON bit is cleared. When the ON bit is cleared by either a PRx match or by software control the timer will stay in Reset until both the ON bit is set and the external signal is not at the Reset level.

When Level-Triggered Hardware Limit One-Shot modes are used in conjunction with the CCP PWM operation the PWM drive goes active with either the external signal edge or the setting of the ON bit, whichever of the two starts the timer.

FIGURE 29-13: LEVEL-TRIGGERED HARDWARE LIMIT ONE-SHOT MODE TIMING DIAGRAM (MODE = 10110)



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REGISTER 29-3: TxHLT: TIMERx HARDWARE LIMIT CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
PSYNC ^(1, 2)	CKPOL ⁽³⁾	CKSYNC ^(4, 5)	MODE<4:0> ^(6, 7)				
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

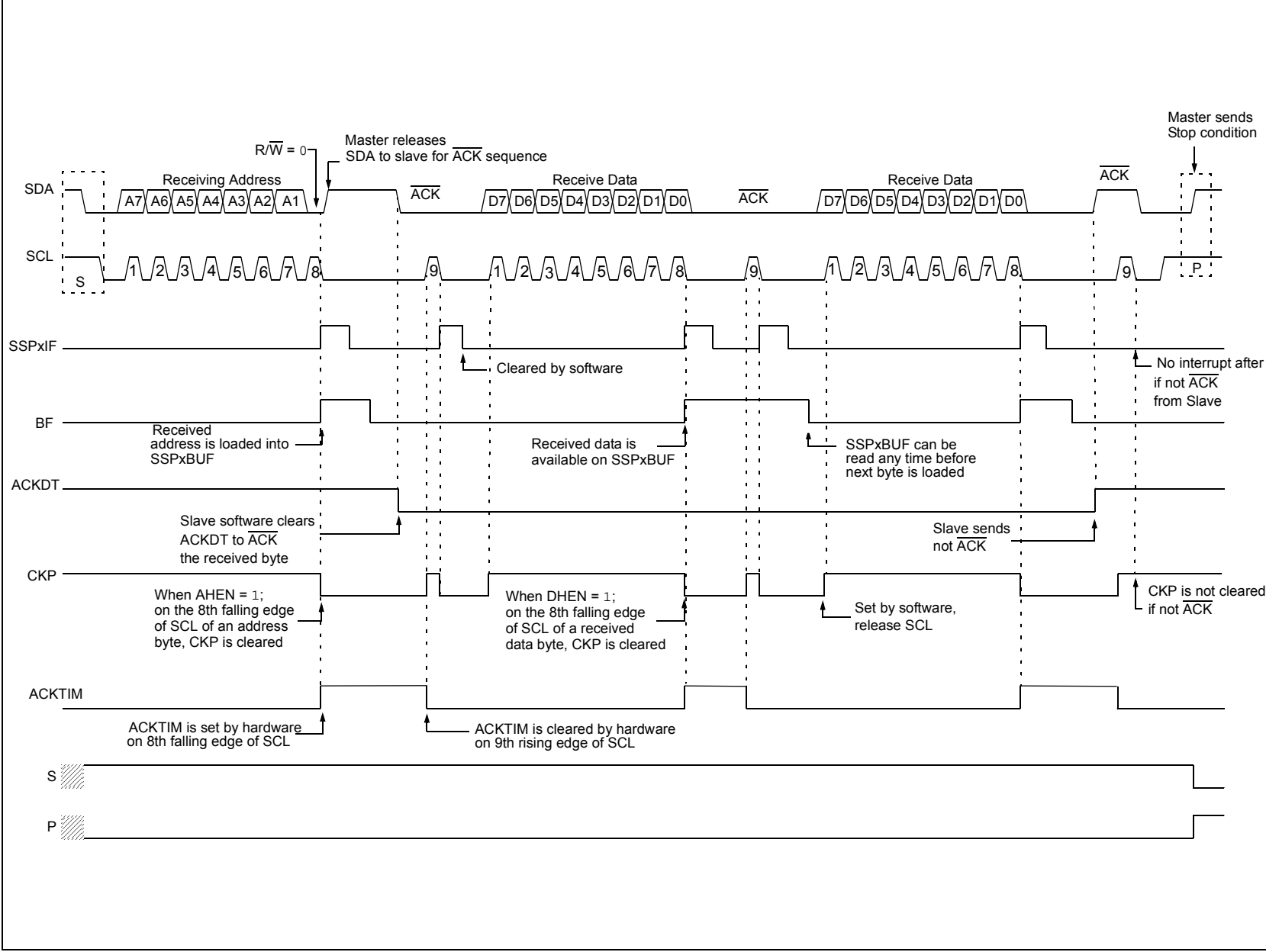
'1' = Bit is set

'0' = Bit is cleared

- bit 7 **PSYNC:** Timerx Prescaler Synchronization Enable bit^(1, 2)
 1 = TMRx Prescaler Output is synchronized to Fosc/4
 0 = TMRx Prescaler Output is not synchronized to Fosc/4
- bit 6 **CKPOL:** Timerx Clock Polarity Selection bit⁽³⁾
 1 = Falling edge of input clock clocks timer/prescaler
 0 = Rising edge of input clock clocks timer/prescaler
- bit 5 **CKSYNC:** Timerx Clock Synchronization Enable bit^(4, 5)
 1 = ON register bit is synchronized to TMR2_clk input
 0 = ON register bit is not synchronized to TMR2_clk input
- bit 4-0 **MODE<4:0>:** Timerx Control Mode Selection bits^(6, 7)
 See Table 29-1.

- Note 1:** Setting this bit ensures that reading TMRx will return a valid value.
- 2:** When this bit is '1', Timer2 cannot operate in Sleep mode.
- 3:** CKPOL should not be changed while ON = 1.
- 4:** Setting this bit ensures glitch-free operation when the ON is enabled or disabled.
- 5:** When this bit is set then the timer operation will be delayed by two TMRx input clocks after the ON bit is set.
- 6:** Unless otherwise indicated, all modes start upon ON = 1 and stop upon ON = 0 (stops occur without affecting the value of TMRx).
- 7:** When TMRx = PRx, the next clock clears TMRx, regardless of the operating mode.

FIGURE 31-17: I²C SLAVE, 7-BIT ADDRESS, RECEPTION (SEN = 1, AHEN = 1, DHEN = 1)



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31.5.6 CLOCK STRETCHING

Clock stretching occurs when a device on the bus holds the SCL line low, effectively pausing communication. The slave may stretch the clock to allow more time to handle data or prepare a response for the master device. A master device is not concerned with stretching as anytime it is active on the bus and not transferring data it is stretching. Any stretching done by a slave is invisible to the master software and handled by the hardware that generates SCL.

The CKP bit of the SSPxCON1 register is used to control stretching in software. Any time the CKP bit is cleared, the module will wait for the SCL line to go low and then hold it. Setting CKP will release SCL and allow more communication.

31.5.6.1 Normal Clock Stretching

Following an $\overline{\text{ACK}}$ if the R/W bit of SSPxSTAT is set, a read request, the slave hardware will clear CKP. This allows the slave time to update SSPxBUF with data to transfer to the master. If the SEN bit of SSPxCON2 is set, the slave hardware will always stretch the clock after the $\overline{\text{ACK}}$ sequence. Once the slave is ready; CKP is set by software and communication resumes.

Note 1: The BF bit has no effect on if the clock will be stretched or not. This is different than previous versions of the module that would not stretch the clock, clear CKP, if SSPxBUF was read before the ninth falling edge of SCL.

2: Previous versions of the module did not stretch the clock for a transmission if SSPxBUF was loaded before the ninth falling edge of SCL. It is now always cleared for read requests.

31.5.6.2 10-bit Addressing Mode

In 10-bit Addressing mode, when the UA bit is set the clock is always stretched. This is the only time the SCL is stretched without CKP being cleared. SCL is released immediately after a write to SSPxADD.

Note: Previous versions of the module did not stretch the clock if the second address byte did not match.

31.5.6.3 Byte NACKing

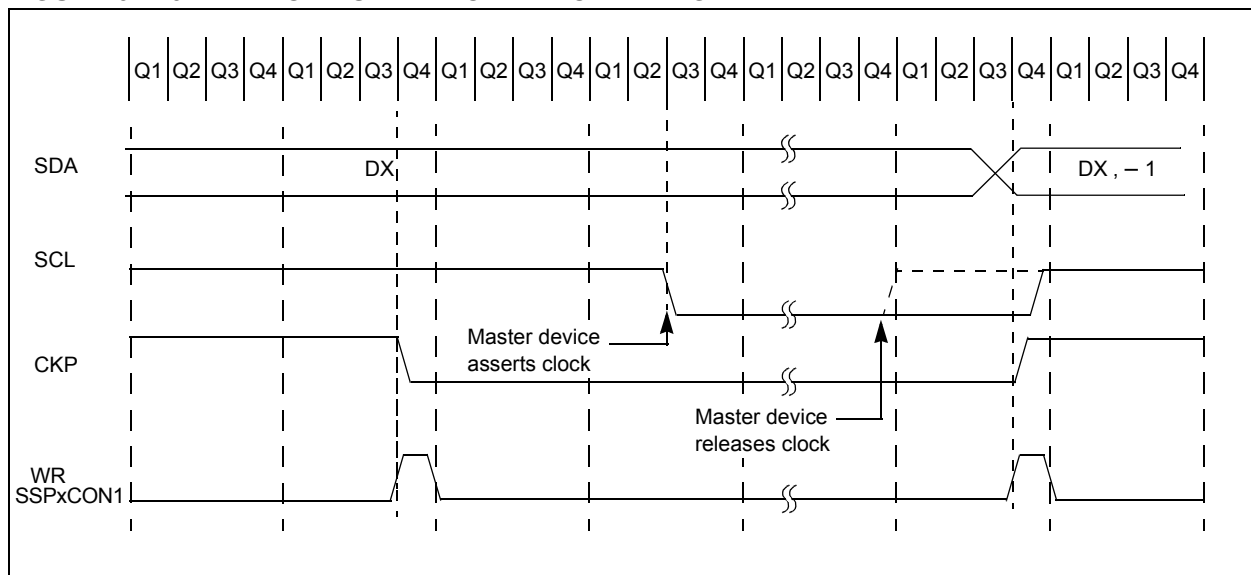
When AHEN bit of SSPxCON3 is set; CKP is cleared by hardware after the eighth falling edge of SCL for a received matching address byte. When DHEN bit of SSPxCON3 is set; CKP is cleared after the eighth falling edge of SCL for received data.

Stretching after the eighth falling edge of SCL allows the slave to look at the received address or data and decide if it wants to ACK the received data.

31.5.7 CLOCK SYNCHRONIZATION AND THE CKP BIT

Any time the CKP bit is cleared, the module will wait for the SCL line to go low and then hold it. However, clearing the CKP bit will not assert the SCL output low until the SCL output is already sampled low. Therefore, the CKP bit will not assert the SCL line until an external I²C master device has already asserted the SCL line. The SCL output will remain low until the CKP bit is set and all other devices on the I²C bus have released SCL. This ensures that a write to the CKP bit will not violate the minimum high time requirement for SCL (see Figure 31-23).

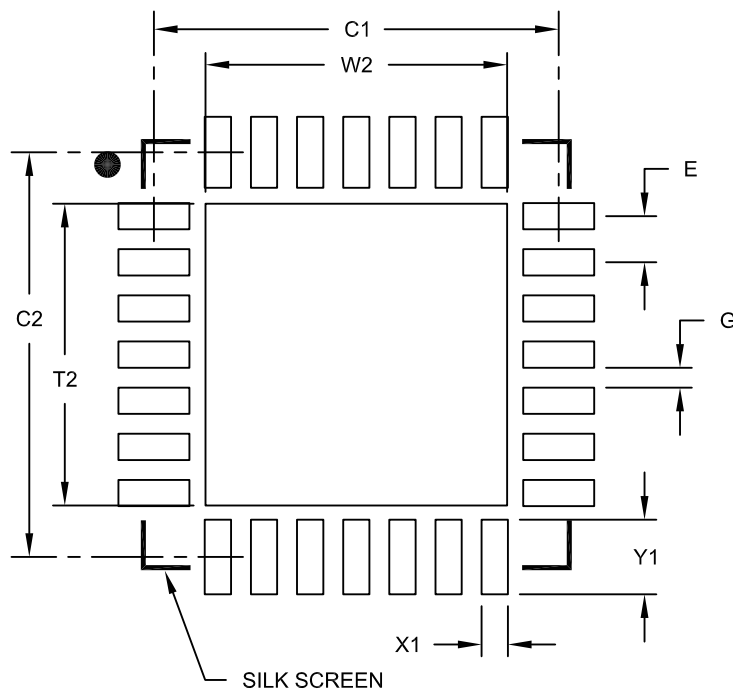
FIGURE 31-23: CLOCK SYNCHRONIZATION TIMING



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28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			4.25
Optional Center Pad Length	T2			4.25
Contact Pad Spacing	C1		5.70	
Contact Pad Spacing	C2		5.70	
Contact Pad Width (X28)	X1			0.37
Contact Pad Length (X28)	Y1			1.00
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2105A