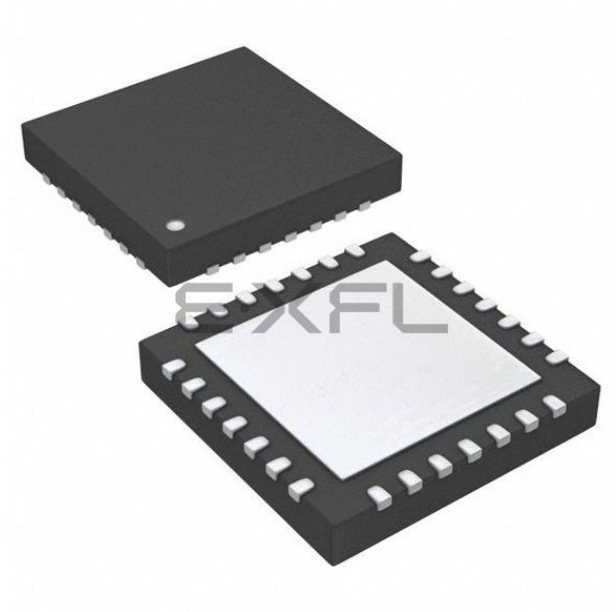

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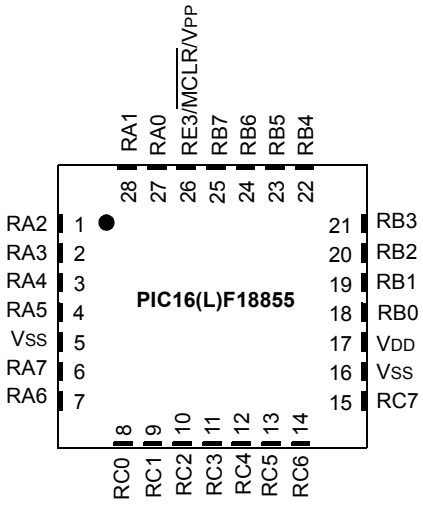
Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UFQFN Exposed Pad
Supplier Device Package	28-UQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf18855-e-mv

28-pin QFN (6x6), UQFN (4x4)

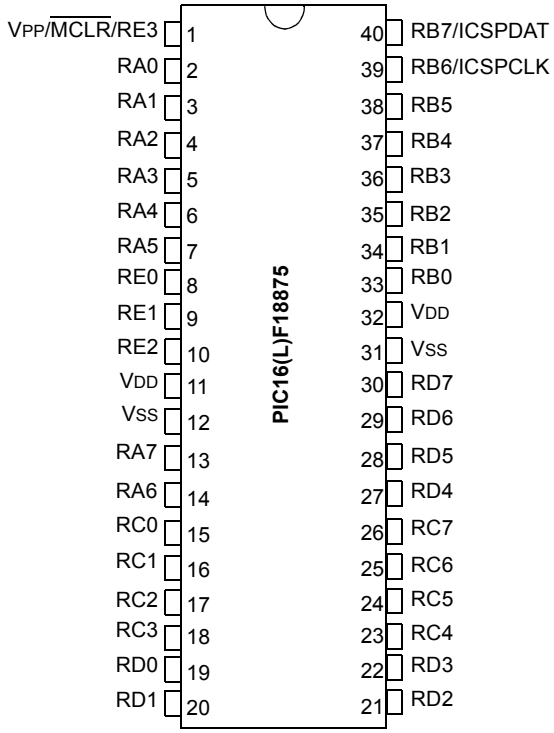


Note 1: See Table 2 for location of all peripheral functions.

2: All VDD and all VSS pins must be connected at the circuit board level. Allowing one or more VSS or VDD pins to float may result in degraded electrical performance or non-functionality.

3: The bottom pad of the QFN/UQFN package should be connected to VSS at the circuit board level.

40-pin PDIP



Note 1: See Table 3 for location of all peripheral function.

2: All VDD and all VSS pins must be connected at the circuit board level. Allowing one or more VSS or VDD pins to float may result in degraded electrical performance or non-functionality.

TABLE 3-13: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-31 (CONTINUED)

Address	Name	PIC16(L)F18855	PIC16(L)F18875	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Bank 4													
CPU CORE REGISTERS; see Table 3-2 for specifics													
20Ch	TMR1L			Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								0000 0000	uuuu uuuu
20Dh	TMR1H			Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								0000 0000	uuuu uuuu
20Eh	T1CON			—	—	CKPS<1:0>		—	$\overline{\text{SYNC}}$	RD16	ON	--00 -000	--uu -uuu
20Fh	T1GCON			GE	GPOL	GTM	GSPM	GGO/$\overline{\text{DONE}}$	GVAL	—	—	0000 0x--	uuuu ux--
210h	T1GATE			—	—	—	GSS<4:0>					---0 0000	---u uuuu
211h	T1CLK			—	—	—	—	CS<3:0>				---- 0000	---- uuuu
212h	TMR3L			Holding Register for the Least Significant Byte of the 16-bit TMR3 Register								0000 0000	uuuu uuuu
213h	TMR3H			Holding Register for the Most Significant Byte of the 16-bit TMR3 Register								0000 0000	uuuu uuuu
214h	T3CON			—	—	CKPS<1:0>		—	$\overline{\text{SYNC}}$	RD16	ON	--00 -000	--uu -uuu
215h	T3GCON			GE	GPOL	GTM	GSPM	GGO/$\overline{\text{DONE}}$	GVAL	—	—	0000 0x--	uuuu ux--
216h	T3GATE			—	—	—	GSS<4:0>					---0 0000	---u uuuu
217h	T3CLK			—	—	—	—	CS<3:0>				---- 0000	---- uuuu
218h	TMR5L			Holding Register for the Least Significant Byte of the 16-bit TMR5 Register								0000 0000	uuuu uuuu
219h	TMR5H			Holding Register for the Most Significant Byte of the 16-bit TMR5 Register								0000 0000	uuuu uuuu
21Ah	T5CON			—	—	CKPS<1:0>		—	$\overline{\text{SYNC}}$	RD16	ON	--00 -000	--uu -uuu
21Bh	T5GCON			GE	GPOL	GTM	GSPM	GGO/$\overline{\text{DONE}}$	GVAL	—	—	0000 0x--	uuuu ux--
21Ch	T5GATE			—	—	—	GSS<4:0>					---0 0000	---u uuuu
21Dh	T5CLK			—	—	—	—	CS<3:0>				---- 0000	---- uuuu
21Eh	CCPTMRS0			C4TSEL<1:0>		C3TSEL<1:0>		C2TSEL<1:0>		C1TSEL<1:0>		0101 0101	0101 0101
21Fh	CCPTMRS1			—	—	P7TSEL<1:0>		P6TSEL<1:0>		C5TSEL<1:0>		--01 0101	--01 0101

Legend: x = unknown, u = unchanged, q =depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Register present on PIC16F18855/75 devices only.

2: Unimplemented, read as '1'.

TABLE 3-13: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-31 (CONTINUED)

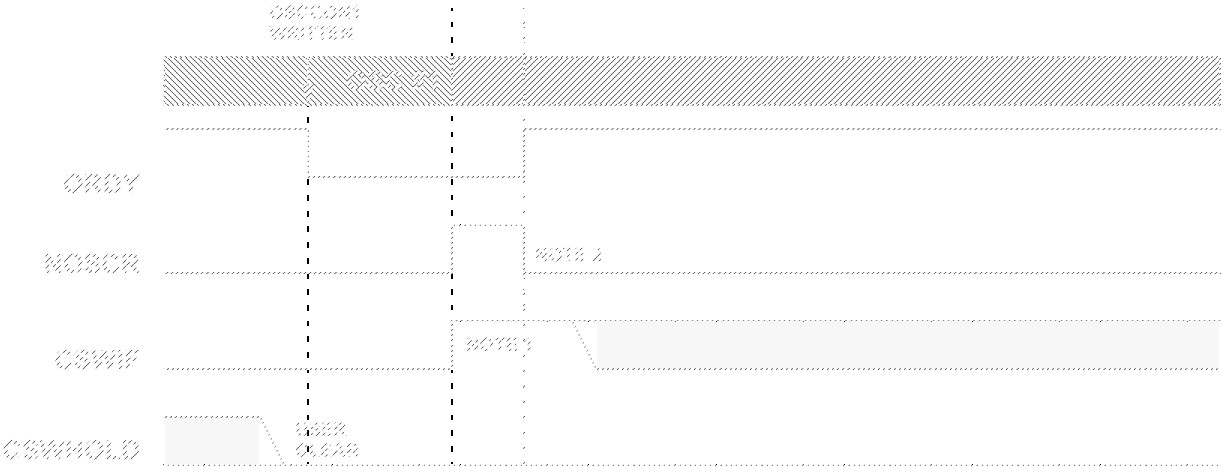
Address	Name	PIC16(L)F18855	PIC16(L)F18875	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Banks 17													
CPU CORE REGISTERS; see Table 3-2 for specifics													
88Ch	CPUDOZE			IDLEN	DOZEN	ROI	DOE	—	DOZE2	DOZE1	DOZE0	0000 -000	0000 -000
88Dh	OSCCON1			—	NOSC<2:0>			NDIV<3:0>				-qqq 0000	-qqq 0000
88Eh	OSCCON2			—	COSC<2:0>			CDIV<3:0>				-qqq qqqq	-qqq qqqq
88Fh	OSCCON3			CSWHOLD	SOSCPWR	—	ORDY	NOSCR	—	—	—	00-0 0---	00-0 0---
890h	OSCSTAT			EXTOR	HFOR	MFOR	LFOR	SOR	ADOR	—	PLLR	q0-0 qq-0	q0-0 qq-0
891h	OSCEN			EXTOEN	HFOEN	MFOEN	LFOEN	SOSCEN	ADOEN	—	—	00-0 00--	00-0 00--
892h	OSCTUNE			—	—	HFTUN<5:0>						--10 0000	--10 0000
893h	OSCFRQ			—	—	—	—	—	HFFRQ<2:0>			---- -qqq	---- -qqq
894h	—	—		Unimplemented								—	—
895h	CLKRCON			CLKREN	—	—	CLKRDC<1:0>		CLKRDIV<2:0>			0--1 0000	0--1 0000
896h	CLKRCLK			—	—	—	—	CLKRCLK<3:0>				---- 0000	---- 0000
897h	MDCON0			MDEN	—	MDOUT	MDOPOL	—	—	—	MDBIT	0-00 ---0	0-00 ---0
898h	MDCON1			—	—	MDCHPOL	MDCHSYNC	—	—	MDCLPOL	MDCLSYNC	--00 --00	--00 --00
899h	MDSRC			—	—	—	MDMS<4:0>					---0 0000	---0 0000
89Ah	MDCARL			—	—	—	—	MDCLS<3:0>				---- 0000	---- 0000
89Bh	MDCARH			—	—	—	—	MDCHS<3:0>				---- 0000	---- 0000
89Ch	—	—		Unimplemented								—	—
89Dh	—	—		Unimplemented								—	—
89Eh	—	—		Unimplemented								—	—
89Fh	—	—		Unimplemented								—	—

Legend: x = unknown, u = unchanged, q =depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Register present on PIC16F18855/75 devices only.

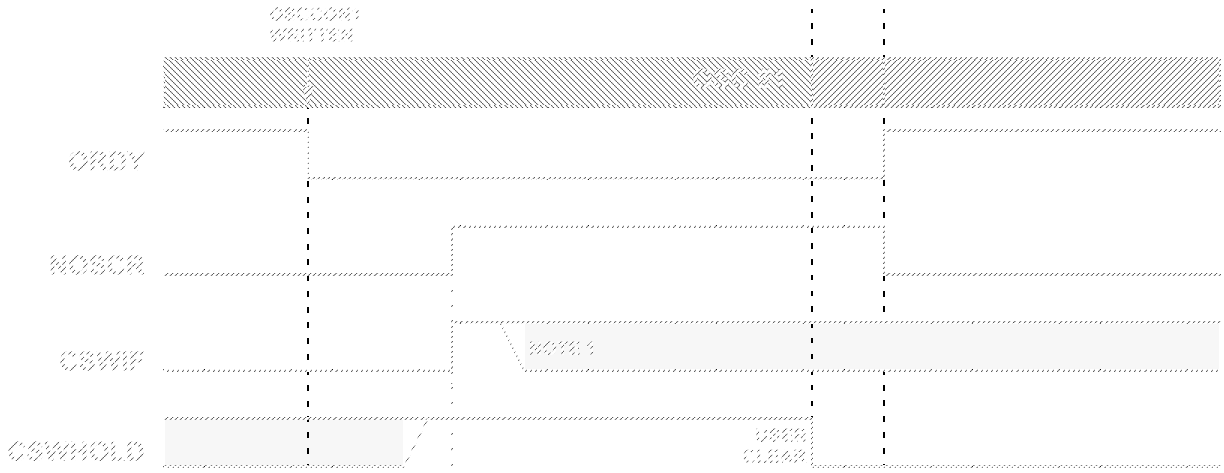
2: Unimplemented, read as '1'.

FIGURE 6-6: CLOCK SWITCH (CSWHOLD = 0)



Note 1: CSWIF is asserted coincident with NOSCR; interrupt is serviced at OSC#2 speed.
2: The assertion of NOSCR is hidden from the user because it appears only for the duration of the switch.

FIGURE 6-7: CLOCK SWITCH (CSWHOLD = 1)

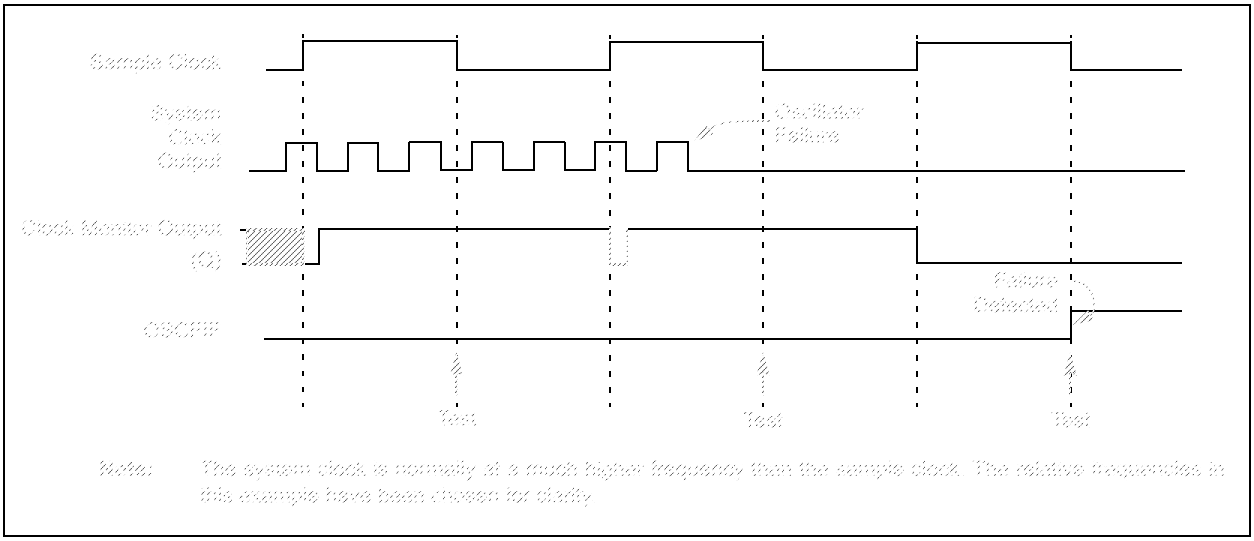


Note 1: CSWIF is asserted coincident with NOSCR, and may be cleared before or after clearing CSWHOLD = 0.

6.4.4 RESET OR WAKE-UP FROM SLEEP

The FSCM is designed to detect an oscillator failure after the Oscillator Start-up Timer (OST) has expired. The OST is used after waking up from Sleep and after any type of Reset. The OST is not used with the EC Clock modes so that the FSCM will be active as soon as the Reset or wake-up has completed. Therefore, the device will always be executing code while the OST is operating.

FIGURE 6-10: FSCM TIMING DIAGRAM



REGISTER 7-3: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1

R/W-0/0	R/W-0/0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0
OSFIE	CSWIE	—	—	—	—	ADTIE	ADIE
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **OSFIE:** Oscillator Fail Interrupt Enable bit
1 = Enables the Oscillator Fail Interrupt
0 = Disables the Oscillator Fail Interrupt

bit 6 **CSWIE:** Clock Switch Complete Interrupt Enable bit
1 = The clock switch module interrupt is enabled
0 = The clock switch module interrupt is disabled

bit 5-2 **Unimplemented:** Read as ‘0’

bit 1 **ADTIE:** Analog-to-Digital Converter (ADC) Threshold Compare Interrupt Enable bit
1 = Enables the ADC threshold compare interrupt
0 = Disables the ADC threshold compare interrupt

bit 0 **ADIE:** Analog-to-Digital Converter (ADC) Interrupt Enable bit
1 = Enables the ADC interrupt
0 = Disables the ADC interrupt

Note 1: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt controlled by registers PIE1-PIE8.

REGISTER 12-8: SLRCONA: PORTA SLEW RATE CONTROL REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
SLRA7	SLRA6	SLRA5	SLRA4	SLRA3	SLRA2	SLRA1	SLRA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **SLRA<7:0>:** PORTA Slew Rate Enable bits
For RA<7:0> pins, respectively
1 = Port pin slew rate is limited
0 = Port pin slews at maximum rate

REGISTER 12-9: INLVLA: PORTA INPUT LEVEL CONTROL REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
INLVLA7	INLVLA6	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **INLVLA<7:0>:** PORTA Input Level Select bits
For RA<7:0> pins, respectively
1 = ST input used for PORT reads and interrupt-on-change
0 = TTL input used for PORT reads and interrupt-on-change

TABLE 12-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	220
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	220
LATC	LATC7	LATC6	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0	220
ANSELC	ANSC7	ANSC6	ANSC5	ANSC4	ANSC3	ANSC2	ANSC1	ANSC0	221
WPUC	WPUC7	WPUC6	WPUC5	WPUC4	WPUC3	WPUC2	WPUC1	WPUC0	221
ODCONC	ODCC7	ODCC6	ODCC5	ODCC4	ODCC3	ODCC2	ODCC1	ODCC0	222
SLRCONC	SLRC7	SLRC6	SLRC5	SLRC4	SLRC3	SLRC2	SLRC1	SLRC0	222
INLVLC	INLVLC7	INLVLC6	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0	222
CCDPC	CCDPC7	CCDPC6	CCDPC5	CCDPC4	CCDPC3	CCDPC2	CCDPC1	CCDPC0	223
CCDNC	CCDNC7	CCDNC6	CCDNC5	CCDNC4	CCDNC3	CCDNC2	CCDNC1	CCDNC0	223
CCDCON	CCDEN	—	—	—	—	—	CCDS<1:0>		201

Legend: – = unimplemented locations read as '0'. Shaded cells are not used by PORTC.

12.12 PORTE Registers (PIC16(L)F18855)

12.12.1 DATA REGISTER

PORTE is a 4-bit wide, bidirectional port. The corresponding data direction register is TRISE (Register 12-42). Setting a TRISE bit (= 1) will make the corresponding PORTE pin an input (i.e., disable the output driver). Clearing a TRISE bit (= 0) will make the corresponding PORTE pin an output (i.e., enables output driver and puts the contents of the output latch on the selected pin). Example 12.4.9 shows how to initialize PORTE.

Reading the PORTE register (Register 12-42) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch (LATE).

12.12.2 INPUT THRESHOLD CONTROL

The INLVLE register (Register 12-44) controls the input voltage threshold for each of the available PORTE input pins. A selection between the Schmitt Trigger CMOS or the TTL Compatible thresholds is available. The input threshold is important in determining the value of a read of the PORTE register and also the level at which an interrupt-on-change occurs, if that feature is enabled. See Table 37-4 for more information on threshold levels.

Note:	Changing the input threshold selection should be performed while all peripheral modules are disabled. Changing the threshold level during the time a module is active may inadvertently generate a transition associated with an input pin, regardless of the actual voltage level on that pin.

12.12.3 WEAK PULL-UP CONTROL

The WPUE register (Register 12-43) controls the individual weak pull-ups for each port pin.

12.12.4 PORTE FUNCTIONS AND OUTPUT PRIORITIES

Each pin defaults to the PORT latch data after Reset. Other output functions are selected with the peripheral pin select logic. See **Section 13.0 "Peripheral Pin Select (PPS) Module"** for more information.

Analog input functions, such as ADC and comparator inputs, are not shown in the peripheral pin select lists. Digital output functions may continue to control the pin when it is in Analog mode.

12.12.5 PORTE FUNCTIONS AND OUTPUT PRIORITIES

Each pin defaults to the PORT latch data after Reset. Other output functions are selected with the peripheral pin select logic. See **Section 13.0 "Peripheral Pin Select (PPS) Module"** for more information.

Analog input functions, such as ADC and comparator inputs, are not shown in the peripheral pin select lists. Digital output functions may continue to control the pin when it is in Analog mode.

19.2 Register Definitions: PWM Control

REGISTER 19-1: PWMxCON: PWM CONTROL REGISTER

R/W-0/0	U-0	R-0	R/W-0/0	U-0	U-0	U-0	U-0
PWMxEN	—	PWMxOUT	PWMxPOL	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **PWMxEN:** PWM Module Enable bit
1 = PWM module is enabled
0 = PWM module is disabled

bit 6 **Unimplemented:** Read as ‘0’

bit 5 **PWMxOUT:** PWM Module Output Level when Bit is Read

bit 4 **PWMxPOL:** PWMx Output Polarity Select bit
1 = PWM output is active-low
0 = PWM output is active-high

bit 3-0 **Unimplemented:** Read as ‘0’

TABLE 19-3: SUMMARY OF REGISTERS ASSOCIATED WITH PWMx

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
PWM6CON	PWM6EN	—	PWM6OUT	PWM6POL	—	—	—	—	287
PWM6DCH	PWM6DC<9:2>								288
PWM6DCL	PWM6DC<1:0>		—	—	—	—	—	—	288
PWM7CON	PWM7EN	—	PWM7OUT	PWM7POL	—	—	—	—	287
PWM7DCH	PWM7DC<9:2>								288
PWM7DCL	PWM7DC<1:0>		—	—	—	—	—	—	288
T2CON	ON	CKPS<2:0>			OUTPS<3:0>				441
T4CON	ON	CKPS<2:0>			OUTPS<3:0>				441
T6CON	ON	CKPS<2:0>			OUTPS<3:0>				441
T2TMR	Holding Register for the 8-bit TMR2 Register								
T4TMR	Holding Register for the 8-bit TMR4 Register								
T6TMR	Holding Register for the 8-bit TMR6 Register								
T2PR	TMR2 Period Register								
T4PR	TMR4 Period Register								
T6PR	TMR6 Period Register								
RxyPPS	—	—	RxyPPS<5:0>						250
CWG1ISM	—	—	—	—	IS<3:0>				312
CWG2ISM					IS<3:0>				312
CWG3ISM					IS<3:0>				312
CLCxSELy	—	—	LCxDyS<5:0>						329
MDSRC	—	—	—	MDMS<4:0>					399
MDCARH	—	—	—	—	MDCHS<3:0>				400
MDCARL	—	—	—	—	MDCLS<3:0>				401
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	204
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	220

Legend: - = Unimplemented locations, read as '0'. Shaded cells are not used by the PWMx module.

TABLE 25-1: SUMMARY OF REGISTERS ASSOCIATED WITH THE DAC1 MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
DAC1CON0	DAC1EN	—	DAC1OE1	DAC1OE2	DAC1PSS<1:0>		—	DAC1NSS	389
DAC1CON1	—	—	—	DAC1R<4:0>					389
CM1PSEL	—	—	—	—	—	PCH<2:0>			281
CM2PSEL	—	—	—	—	—	PCH<2:0>			281
ADPCH	—	—	ADPCH<5:0>						357

Legend: — = Unimplemented location, read as '0'. Shaded cells are not used with the DAC module.

28.12 Register Definitions: Timer1 Control start here with Memory chapter compare

Long bit name prefixes for the Timer1/3/5 are shown in Table 28-3. Refer to **Section 1.1 "Register and Bit naming conventions"** for more information

TABLE 28-3:

Peripheral	Bit Name Prefix
Timer1	T1
Timer3	T3
Timer5	T5

REGISTER 28-1: TxCON: TIMER1/3/5 CONTROL REGISTER

U-0	U-0	R/W-0/u	R/W-0/u	U-0	R/W-0/u	R/W-0/u	R/W-0/u
—	—	CKPS<1:0>		—	$\overline{\text{SYNC}}$	RD16	ON
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **CKPS<1:0>:** Timer1 Input Clock Prescale Select bits
11 = 1:8 Prescale value
10 = 1:4 Prescale value
01 = 1:2 Prescale value
00 = 1:1 Prescale value

bit 3 **Unimplemented:** Read as '0'

bit 2 **SYNC:** Timer1 Synchronization Control bit
When TMR1CLK = FOSC or FOSC/4
This bit is ignored. The timer uses the internal clock and no additional synchronization is performed.
When TMR1CS<1:0> = (any setting other than FOSC or FOSC/4)
1 = Do not synchronize external clock input
0 = Synchronized external clock input with system clock

bit 1 **RD16:** Timer1 On bit
1 = All 16 bits of Timer1 can be read simultaneously (TMR1H is buffered)
0 = 16-bit reads of Timer1 are disabled (TMR1H is not buffered)

bit 0 **ON:** Timer1 On bit
1 = Enables Timer1
0 = Stops Timer1 and clears Timer1 gate flip-flop

31.2 SPI Mode Overview

The Serial Peripheral Interface (SPI) bus is a synchronous serial data communication bus that operates in Full-Duplex mode. Devices communicate in a master/slave environment where the master device initiates the communication. A slave device is controlled through a Chip Select known as Slave Select.

The SPI bus specifies four signal connections:

- Serial Clock (SCK)
- Serial Data Out (SDO)
- Serial Data In (SDI)
- Slave Select ($\overline{SS}$)

Figure 31-1 shows the block diagram of the MSSP module when operating in SPI mode.

The SPI bus operates with a single master device and one or more slave devices. When multiple slave devices are used, an independent Slave Select connection is required from the master device to each slave device.

Figure 31-4 shows a typical connection between a master device and multiple slave devices.

The master selects only one slave at a time. Most slave devices have tri-state outputs so their output signal appears disconnected from the bus when they are not selected.

Transmissions involve two shift registers, eight bits in size, one in the master and one in the slave. With either the master or the slave device, data is always shifted out one bit at a time, with the Most Significant bit (MSb) shifted out first. At the same time, a new Least Significant bit (LSb) is shifted into the same register.

Figure 31-5 shows a typical connection between two processors configured as master and slave devices.

Data is shifted out of both shift registers on the programmed clock edge and latched on the opposite edge of the clock.

The master device transmits information out on its SDO output pin which is connected to, and received by, the slave's SDI input pin. The slave device transmits information out on its SDO output pin, which is connected to, and received by, the master's SDI input pin.

To begin communication, the master device first sends out the clock signal. Both the master and the slave devices should be configured for the same clock polarity.

The master device starts a transmission by sending out the MSb from its shift register. The slave device reads this bit from that same line and saves it into the LSb position of its shift register.

During each SPI clock cycle, a full-duplex data transmission occurs. This means that while the master device is sending out the MSb from its shift register (on its SDO pin) and the slave device is reading this bit and saving it as the LSb of its shift register, that the slave device is also sending out the MSb from its shift register (on its SDO pin) and the master device is reading this bit and saving it as the LSb of its shift register.

After eight bits have been shifted out, the master and slave have exchanged register values.

If there is more data to exchange, the shift registers are loaded with new data and the process repeats itself.

Whether the data is meaningful or not (dummy data), depends on the application software. This leads to three scenarios for data transmission:

- Master sends useful data and slave sends dummy data.
- Master sends useful data and slave sends useful data.
- Master sends dummy data and slave sends useful data.

Transmissions may involve any number of clock cycles. When there is no more data to be transmitted, the master stops sending the clock signal and it deselects the slave.

Every slave device connected to the bus that has not been selected through its slave select line must disregard the clock and transmission signals and must not transmit out any data of its own.

31.5.3.3 7-bit Transmission with Address Hold Enabled

Setting the AHEN bit of the SSPxCON3 register enables additional clock stretching and interrupt generation after the eighth falling edge of a received matching address. Once a matching address has been clocked in, CKP is cleared and the SSPxIF interrupt is set.

Figure 31-19 displays a standard waveform of a 7-bit address slave transmission with AHEN enabled.

1. Bus starts Idle.
2. Master sends Start condition; the S bit of SSPxSTAT is set; SSPxIF is set if interrupt on Start detect is enabled.
3. Master sends matching address with R/$\overline{W}$ bit set. After the eighth falling edge of the SCL line the CKP bit is cleared and SSPxIF interrupt is generated.
4. Slave software clears SSPxIF.
5. Slave software reads ACKTIM bit of SSPxCON3 register, and R/$\overline{W}$ and D/$\overline{A}$ of the SSPxSTAT register to determine the source of the interrupt.
6. Slave reads the address value from the SSPxBUF register clearing the BF bit.
7. Slave software decides from this information if it wishes to $\overline{ACK}$ or not $\overline{ACK}$ and sets the ACKDT bit of the SSPxCON2 register accordingly.
8. Slave sets the CKP bit releasing SCL.
9. Master clocks in the $\overline{ACK}$ value from the slave.
10. Slave hardware automatically clears the CKP bit and sets SSPxIF after the $\overline{ACK}$ if the R/$\overline{W}$ bit is set.
11. Slave software clears SSPxIF.
12. Slave loads value to transmit to the master into SSPxBUF setting the BF bit.

Note: SSPxBUF cannot be loaded until after the $\overline{ACK}$.

13. Slave sets the CKP bit releasing the clock.
14. Master clocks out the data from the slave and sends an $\overline{ACK}$ value on the ninth SCL pulse.
15. Slave hardware copies the $\overline{ACK}$ value into the ACKSTAT bit of the SSPxCON2 register.
16. Steps 10-15 are repeated for each byte transmitted to the master from the slave.
17. If the master sends a not $\overline{ACK}$ the slave releases the bus allowing the master to send a Stop and end the communication.

Note: Master must send a not $\overline{ACK}$ on the last byte to ensure that the slave releases the SCL line to receive a Stop.

FIGURE 34-1: CLOCK REFERENCE BLOCK DIAGRAM

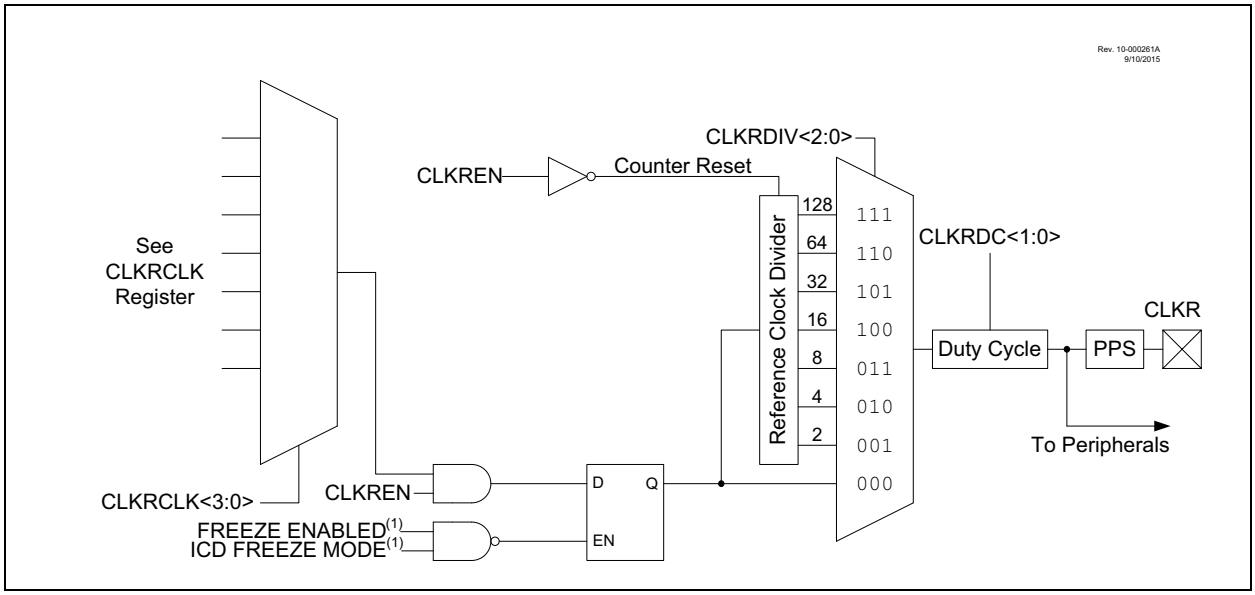


FIGURE 34-2: CLOCK REFERENCE TIMING

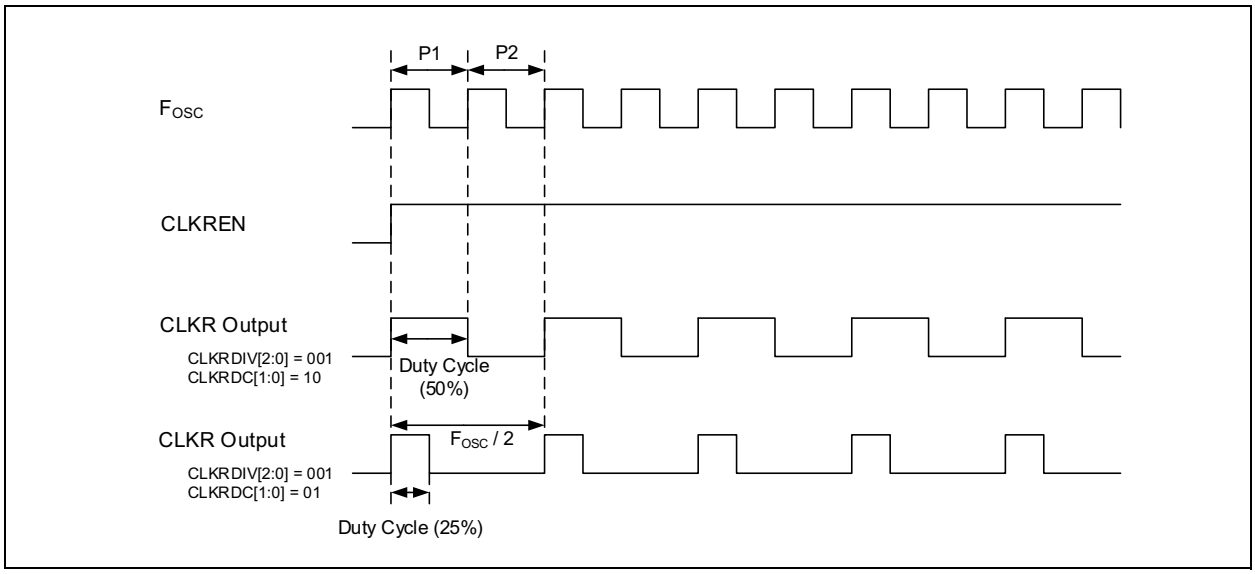
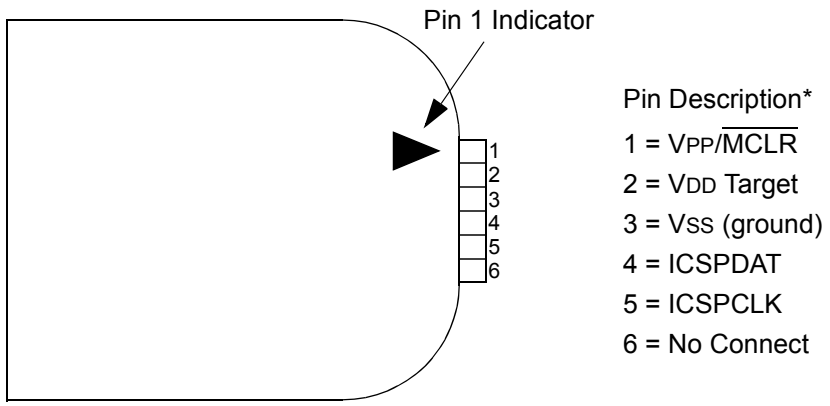
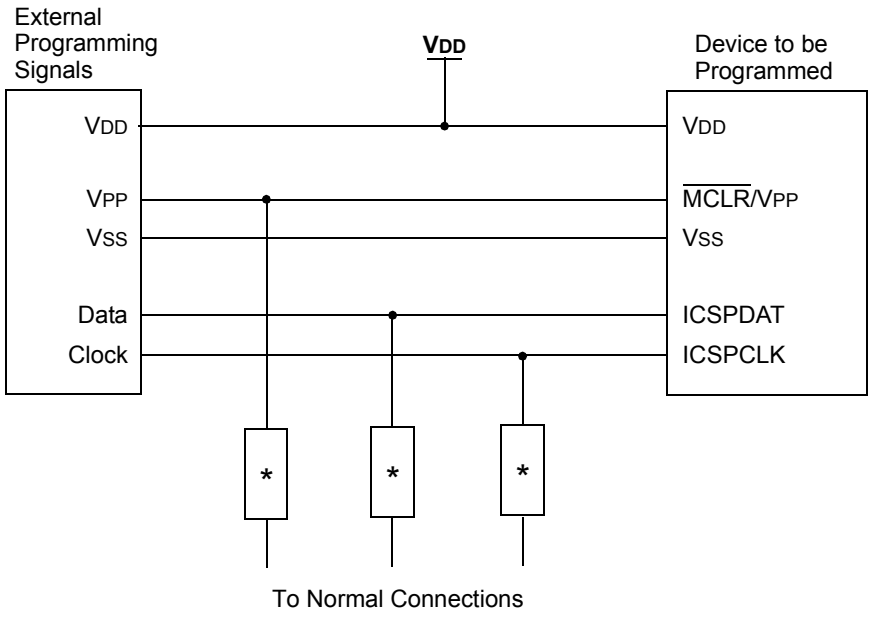


FIGURE 35-2: PICkit™ PROGRAMMER STYLE CONNECTOR INTERFACE



* The 6-pin header (0.100" spacing) accepts 0.025" square pins.

FIGURE 35-3: TYPICAL CONNECTION FOR ICSP™ PROGRAMMING



* Isolation devices (as required).

Note: Unless otherwise noted, VIN = 5V, FOSC = 300 kHz, CIN = 0.1 µF, TA = 25°C.

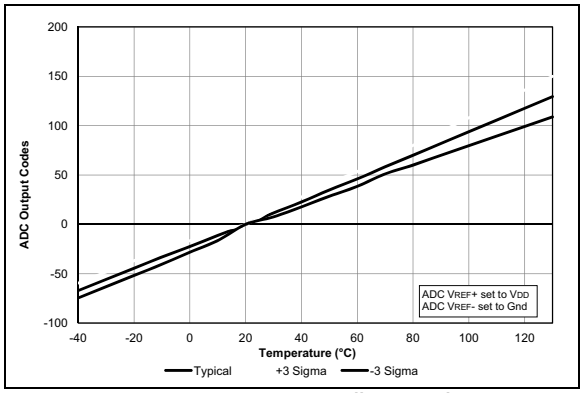


FIGURE 38-61: *Temp. Indicator Slope Normalized to 20°C, Low Range, VDD = 2.3V.*

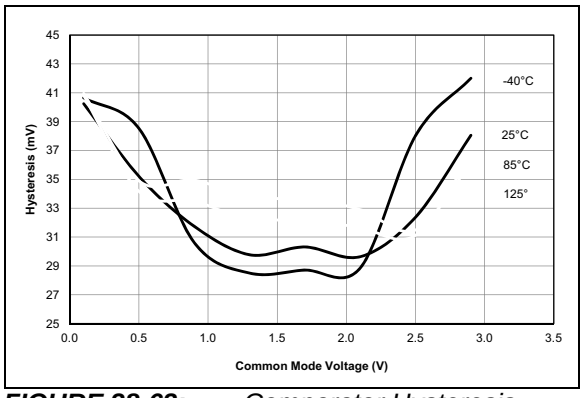


FIGURE 38-62: *Comparator Hysteresis, NP Mode (CxSP = 1), VDD = 3.0V, Typical Measured Values.*

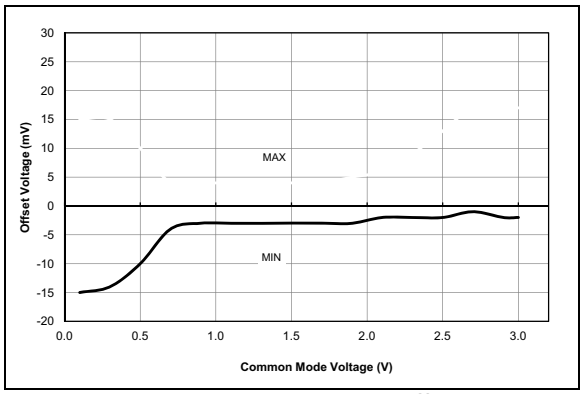


FIGURE 38-63: *Comparator Offset, NP Mode (CxSP = 1), VDD = 3.0V, Typical Measured Values at 25°C.*

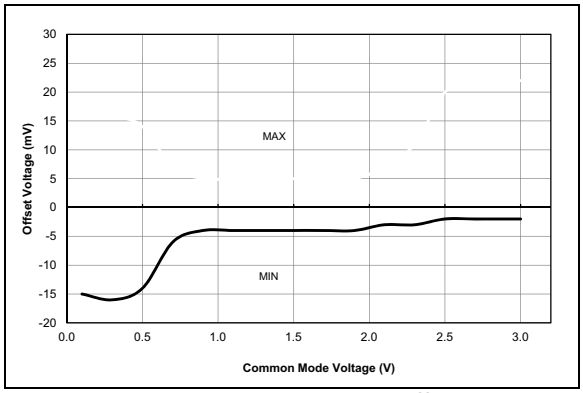


FIGURE 38-64: *Comparator Offset, NP Mode (CxSP = 1), VDD = 3.0V, Typical Measured Values from -40°C to 125°C.*

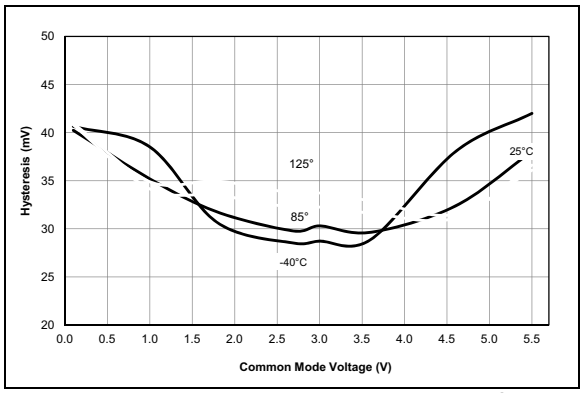


FIGURE 38-65: *Comparator Hysteresis, NP Mode (CxSP = 1), VDD = 5.5V, Typical Measured Values, PIC16F18855/75 Only.*

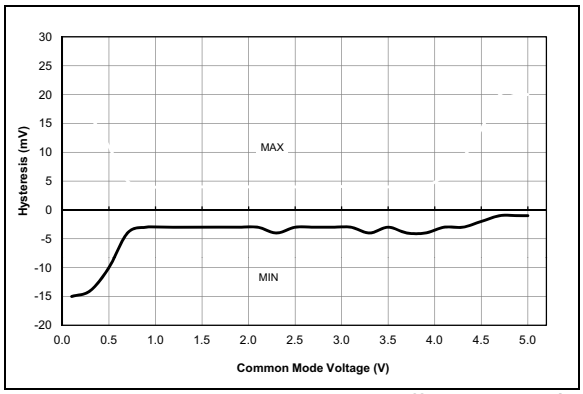
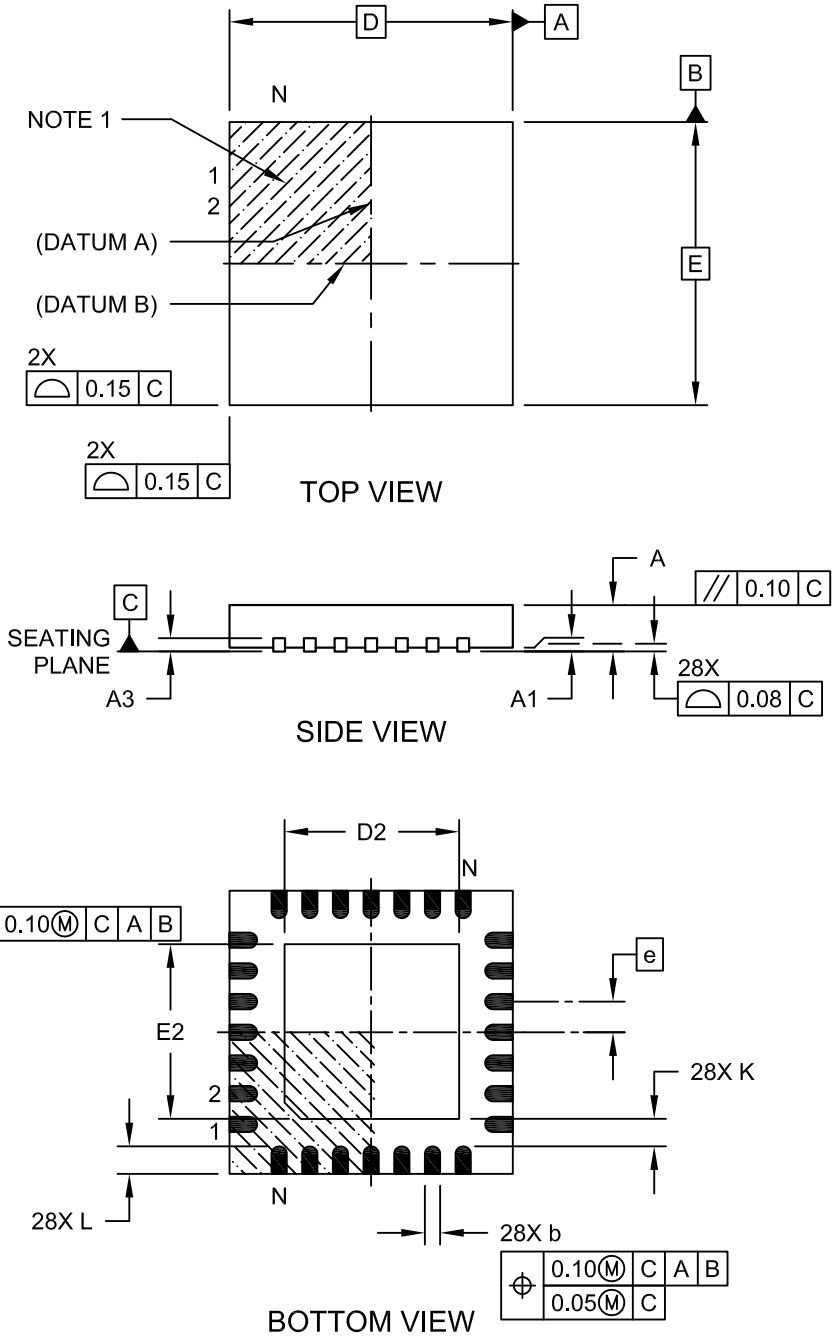


FIGURE 38-66: *Comparator Offset, NP Mode (CxSP = 1), VDD = 5.0V, Typical Measured Values at 25°C, PIC16F18855/75 Only.*

28-Lead Plastic Quad Flat, No Lead Package (ML) - 6x6 mm Body [QFN]
With 0.55 mm Terminal Length

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-105C Sheet 1 of 2

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	-	X	/XX	XXX
Device	Tape and Reel Option		Temperature Range	Package	Pattern

Device:	PIC16F18855; PIC16LF18855; PIC16F18875; PIC16LF18875	
Tape and Reel Option:	Blank T	= Standard packaging (tube or tray) = Tape and Reel(1)
Temperature Range:	I E	= -40°C to +85°C (Industrial) = -40°C to +125°C (Extended)
Package:(2)	ML ML MV MV P PT SO SP SS	= 28-lead QFN 6x6mm = 40-lead QFN 8x8mm = 28-lead UQFN 4x4x0.5mm = 40-lead UQFN 5x5x0.5mm = 40-lead PDIP = 44-lead TQFP 10x10x1 = 28-lead SOIC = 28-lead SPDIP = 28-lead SSOP
Pattern:	QTP, SQTP, Code or Special Requirements (blank otherwise)	

Examples:

a) PIC16F18855- E/SP
Extended temperature
SPDIP package

b) PIC16F18875- I/P
Industrial temperature
PDIP package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: Small form-factor packaging options may be available. Please check www.microchip.com/packaging for small-form factor package availability, or contact your local Sales Office.