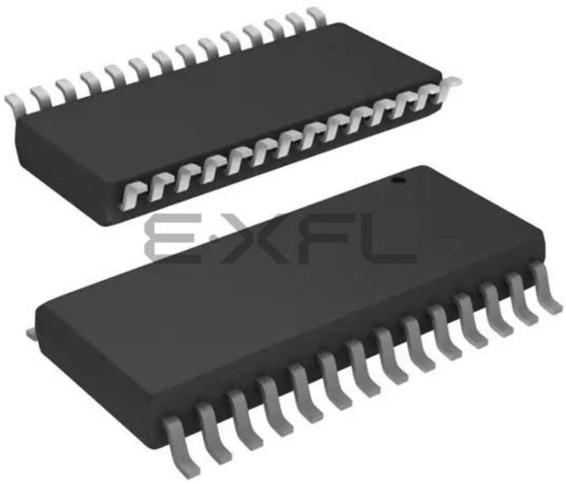

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	25
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf18855t-i-so

TABLE 3: 40/44-PIN ALLOCATION TABLE (PIC16F18875)

I/O	40-Pin PDIP	40-Pin UQFN	44-Pin QFN	44-Pin TQFP	ADC	Voltage Reference	DAC	Comparators	Zero-Cross Detect	MSSP (SPI/I²C)	EUSART	DSM	Timers/SMT	CCP and PWM	CWG	CLC	NCO	Clock Reference (CLKR)	Interrupt-on-Change	Basic
RA0	2	17	19	19	ANA0	—	—	C1IN0- C2IN0-	—	—	—	—	—	—	—	CLCIN0[1]	—	—	IOCA0	—
RA1	3	18	20	20	ANA1	—	—	C1IN1- C2IN1-	—	—	—	—	—	—	—	CLCIN1[1]	—	—	IOCA1	—
RA2	4	19	21	21	ANA2	VREF-	DAC1OUT1	C1IN0+ C2IN0+	—	—	—	—	—	—	—	—	—	—	IOCA2	—
RA3	5	20	22	22	ANA3	VREF+	—	C1IN1+	—	—	—	MDCARL[1]	—	—	—	—	—	—	IOCA3	—
RA4	6	21	23	23	ANA4	—	—	—	—	—	—	MDCARH[1]	T0CKI[1]	CCP5[1]	—	—	—	—	IOCA4	—
RA5	7	22	24	24	ANA5	—	—	—	—	SS1[1]	—	MDSRC[1]	—	—	—	—	—	—	IOCA5	—
RA6	14	29	33	31	ANA6	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCA6	OSC2 CLKOUT
RA7	13	28	32	30	ANA7	—	—	—	—	—	—	—	—	—	—	—	—	—	IOCA7	OSC1 CLKIN
RB0	33	8	9	8	ANB0	—	—	C2IN1+	ZCD	SS2[1]	—	—	—	CCP4[1]	CWG1IN[1]	—	—	—	INT[1] IOCB0	—
RB1	34	9	10	9	ANB1	—	—	C1IN3- C2IN3-	—	SCL2[3,4] SCK2[1]	—	—	—	—	CWG2IN[1]	—	—	—	IOCB1	—
RB2	35	10	11	10	ANB2	—	—	—	—	SDA2[3,4] SDI2[1]	—	—	—	—	CWG3IN[1]	—	—	—	IOCB2	—
RB3	36	11	12	11	ANB3	—	—	C1IN2- C2IN2-	—	—	—	—	—	—	—	—	—	—	IOCB3	—
RB4	37	12	14	14	ANB4 ADCACT[1]	—	—	—	—	—	—	—	T5G[1] SMTWIN2[1]	—	—	—	—	—	IOCB4	—
RB5	38	13	15	15	ANB5	—	—	—	—	—	—	—	T1G[1] SMTSIG2[1]	CCP3(1)	—	—	—	—	IOCB5	—
RB6	39	14	16	16	ANB6	—	—	—	—	—	—	—	—	—	—	CLCIN2[1]	—	—	IOCB6	ICSPCLK
RB7	40	15	17	17	ANB7	—	DAC1OUT2	—	—	—	—	—	T6IN[1]	—	—	CLCIN3[1]	—	—	IOCB7	ICSPDAT

Note 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 13-1 for details on which port pins may be used for this signal.

2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in Table 13-3.

3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.

4: These pins are configured for I²C logic levels.; The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I²C specific or SMbus input buffer thresholds.

TABLE 3-11: PIC16(L)F18875 MEMORY MAP, BANK 30

	Bank 30
F0Ch	—
F0Dh	—
F0Eh	—
F0Fh	—
F10h	RA0PPS
F11h	RA1PPS
F12h	RA2PPS
F13h	RA3PPS
F14h	RA4PPS
F15h	RA5PPS
F16h	RA6PPS
F17h	RA7PPS
F18h	RB0PPS
F19h	RB1PPS
F1Ah	RB2PPS
F1Bh	RB3PPS
F1Ch	RB4PPS
F1Dh	RB5PPS
F1Eh	RB6PPS
F1Fh	RB7PPS
F20h	RC0PPS
F21h	RC1PPS
F22h	RC2PPS
F23h	RC3PPS
F24h	RC4PPS
F25h	RC5PPS
F26h	RC6PPS
F27h	RC7PPS
F28h–F37h	—
F38h	ANSELA
F39h	WPUA
F3Ah	ODCONA
F3Bh	SLRCONA
F3Ch	INLVLA
F3Dh	IOCAP
F3Eh	IOCAN
F3Fh	IOCAF

	Bank 30
F40h	CCDNA
F41h	CCDPA
F42h	—
F43h	ANSELB
F44h	WPUB
F45h	ODCONB
F46h	SLRCONB
F47h	INLVLB
F48h	IOCBP
F49h	IOCBN
F4Ah	IOCBF
F4Bh	CCDNB
F4Ch	CCDPB
F4Dh	—
F4Eh	ANSELC
F4Fh	WPUC
F50h	ODCONC
F51h	SLRCONC
F52h	INLVLC
F53h	IOCCP
F54h	IOCCN
F55h	IOCCF
F56h	CCDNC
F57h	CCDPC
F58h	—
F59h	ANSELD
F5Ah	WPUD
F5Bh	ODCOND
F5Ch	SLRCOND
F5Dh	INLVLD
F5Eh	—
F5Fh	—
F60h	—
F61h	CCDND
F62h	CCDPD
F63h	—

	Bank 30
F64h	ANSELE
F65h	WPUE
F66h	ODCONE
F67h	SLRCONE
F68h	INLVLE
F69h	IOCEP
F6Ah	IOCEN
F6Bh	IOCEF
F6Ch	CCDNE
F6Dh	CCDPE
F6Eh	—
F6Fh	—

Legend: = Unimplemented data memory locations, read as '0'.

TABLE 3-13: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-31 (CONTINUED)

Address	Name	PIC16(L)F18855	PIC16(L)F18875	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Bank 29 (Continued)													
EBAh	MDSRCPPS			—	—	—	MDSRCPPS<4:0>					`---0 0101`	`---u uuuu`
EBBh	CLCIN0PPS			—	—	—	CLCIN0PPS<4:0>					`---0 0000`	`---u uuuu`
EBCh	CLCIN1PPS			—	—	—	CLCIN1PPS<4:0>					`---0 0001`	`---u uuuu`
EBDh	CLCIN2PPS			—	—	—	CLCIN2PPS<4:0>					`---0 1110`	`---u uuuu`
EBEh	CLCIN3PPS			—	—	—	CLCIN3PPS<4:0>					`---0 1111`	`---u uuuu`
EBFh	—	—		Unimplemented								—	—
EC0h	—	—		Unimplemented								—	—
EC1h	—	—		Unimplemented								—	—
EC2h	—	—		Unimplemented								—	—
EC3h	ADCACTPPS			—	—	—	ADCACTPPS<4:0>					`---0 1100`	`---u uuuu`
EC4h	—	—		Unimplemented								—	—
EC5h	SSP1CLKPPS			—	—	—	SSP1CLKPPS<4:0>					`---1 0011`	`---u uuuu`
EC6h	SSP1DATPPS			—	—	—	SSP1DATPPS<4:0>					`---1 0100`	`---u uuuu`
EC7h	SSP1SSPPS			—	—	—	SSP1SSPPS<4:0>					`---0 0101`	`---u uuuu`
EC8h	SSP2CLKPPS			—	—	—	SSP2CLKPPS<4:0>					`---0 1001`	`---u uuuu`
EC9h	SSP2DATPPS			—	—	—	SSP2DATPPS<4:0>					`---0 0010`	`---u uuuu`
ECAh	SSP2SSPPS			—	—	—	SSP2SSPPS<4:0>					`---0 1000`	`---u uuuu`
ECBh	RXPPS			—	—	—	RXPPS<4:0>					`---1 0111`	`---u uuuu`
ECCh	TXPPS			—	—	—	TXPPS<4:0>					`---1 0110`	`---u uuuu`
ECDh to EEFh	—	—		Unimplemented								—	—

Legend: x = unknown, u = unchanged, q =depends on condition, - = unimplemented, read as ‘0’, r = reserved. Shaded locations unimplemented, read as ‘0’.

Note 1: Register present on PIC16F18855/75 devices only.

2: Unimplemented, read as ‘1’.

TABLE 3-13: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-31 (CONTINUED)

Address	Name	PIC16(L)F18855	PIC16(L)F18875	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Bank 30 (Continued)													
F47h	INLVLB			INLVLB7	INLVLB6	INLVLB5	INLVLB4	INLVLB3	INLVLB2	INLVLB1	INLVLB0	1111 1111	1111 1111
F48h	IOCBP			IOCBP7	IOCBP6	IOCBP5	IOCBP4	IOCBP3	IOCBP2	IOCBP1	IOCBP0	0000 0000	0000 0000
F49h	IOCBN			IOCBN7	IOCBN6	IOCBN5	IOCBN4	IOCBN3	IOCBN2	IOCBN1	IOCBN0	0000 0000	0000 0000
F4Ah	IOCBF			IOCBF7	IOCBF6	IOCBF5	IOCBF4	IOCBF3	IOCBF2	IOCBF1	IOCBF0	0000 0000	0000 0000
F4Bh	CCDNB			CCDNB7	CCDNB6	CCDNB5	CCDNB4	CCDNB3	CCDNB2	CCDNB1	CCDNB0	0000 0000	0000 0000
F4Ch	CCDPB			CCDPB7	CCDPB6	CCDPB5	CCDPB4	CCDPB3	CCDPB2	CCDPB1	CCDPB0	0000 0000	0000 0000
F4Dh	—	—		Unimplemented								—	—
F4Eh	ANSELC			ANSC7	ANSC6	ANSC5	ANSC4	ANSC3	ANSC2	ANSC1	ANSC0	1111 1111	1111 1111
F4Fh	WPUC			WPUC7	WPUC6	WPUC5	WPUC4	WPUC3	WPUC2	WPUC1	WPUC0	0000 0000	0000 0000
F50h	ODCONC			ODCC7	ODCC6	ODCC5	ODCC4	ODCC3	ODCC2	ODCC1	ODCC0	0000 0000	0000 0000
F51h	SLRCONC			SLRC7	SLRC6	SLRC5	SLRC4	SLRC3	SLRC2	SLRC1	SLRC0	1111 1111	1111 1111
F52h	INLVLC			INLVLC7	INLVLC6	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0	1111 1111	1111 1111
F53h	IOCCP			IOCCP7	IOCCP6	IOCCP5	IOCCP4	IOCCP3	IOCCP2	IOCCP1	IOCCP0	0000 0000	0000 0000
F54h	IOCCN			IOCCN7	IOCCN6	IOCCN5	IOCCN4	IOCCN3	IOCCN2	IOCCN1	IOCCN0	0000 0000	0000 0000
F55h	IOCCF			IOCCF7	IOCCF6	IOCCF5	IOCCF4	IOCCF3	IOCCF2	IOCCF1	IOCCF0	0000 0000	0000 0000
F56h	CCDNC			CCDNC7	CCDNC6	CCDNC5	CCDNC4	CCDNC3	CCDNC2	CCDNC1	CCDNC0	0000 0000	0000 0000
F57h	CCDPC			CCDPC7	CCDPC6	CCDPC5	CCDPC4	CCDPC3	CCDPC2	CCDPC1	CCDPC0	0000 0000	0000 0000
F58h	—	—		Unimplemented								—	—
F59h	ANSELD	—	X	ANSD7	ANSD6	ANSD5	ANSD4	ANSD3	ANSD2	ANSD1	ANSD0	1111 1111	1111 1111
		X	—	Unimplemented								---- ----	---- ----
F5Ah	WPUD	—	X	WPUD7	WPUD6	WPUD5	WPUD4	WPUD3	WPUD2	WPUD1	WPUD0	0000 0000	0000 0000
		X	—	Unimplemented								---- ----	---- ----
F5Bh	ODCOND	—	X	ODCD7	ODCD6	ODCD5	ODCD4	ODCD3	ODCD2	ODCD1	ODCD0	0000 0000	0000 0000
		X	—	Unimplemented								---- ----	---- ----

Legend: x = unknown, u = unchanged, q =depends on condition, - = unimplemented, read as ‘0’, r = reserved. Shaded locations unimplemented, read as ‘0’.
Note 1: Register present on PIC16F18855/75 devices only.
2: Unimplemented, read as ‘1’.

6.0 OSCILLATOR MODULE (WITH FAIL-SAFE CLOCK MONITOR)

6.1 Overview

The oscillator module has a wide variety of clock sources and selection features that allow it to be used in a wide range of applications while maximizing performance and minimizing power consumption. Figure 6-1 illustrates a block diagram of the oscillator module.

Clock sources can be supplied from external oscillators, quartz-crystal resonators and ceramic resonators. In addition, the system clock source can be supplied from one of two internal oscillators and PLL circuits, with a choice of speeds selectable via software. Additional clock features include:

- Selectable system clock source between external or internal sources via software.
- Fail-Safe Clock Monitor (FSCM) designed to detect a failure of the external clock source (LP, XT, HS, ECH, ECM, ECL) and switch automatically to the internal oscillator.
- Oscillator Start-up Timer (OST) ensures stability of crystal oscillator sources.

The RSTOSC bits of Configuration Word 1 determine the type of oscillator that will be used when the device reset, including when it is first powered up.

The internal clock modes, LFINTOSC, HFINTOSC (set at 1 MHz), or HFINTOSC (set at 32 MHz) can be set through the RSTOSC bits.

If an external clock source is selected, the FEXTOSC bits of Configuration Word 1 must be used in conjunction with the RSTOSC bits to select the external clock mode.

The external oscillator module can be configured in one of the following clock modes, by setting the FEXTOSC<2:0> bits of Configuration Word 1:

1. ECL – External Clock Low-Power mode (below 500 kHz)
2. ECM – External Clock Medium Power mode (500 kHz to 8 MHz)
3. ECH – External Clock High-Power mode (above 8 MHz)
4. LP – 32 kHz Low-Power Crystal mode.
5. XT – Medium Gain Crystal or Ceramic Resonator Oscillator mode (between 100 kHz and 4 MHz)
6. HS – High Gain Crystal or Ceramic Resonator mode (above 4 MHz)

The ECH, ECM, and ECL clock modes rely on an external logic level signal as the device clock source. The LP, XT, and HS clock modes require an external crystal or resonator to be connected to the device. Each mode is optimized for a different frequency range. The INTOSC internal oscillator block produces low and high-frequency clock sources, designated LFINTOSC and HFINTOSC. (see Internal Oscillator Block, Figure 6-1). A wide selection of device clock frequencies may be derived from these clock sources.

6.2 Clock Source Types

Clock sources can be classified as external or internal.

External clock sources rely on external circuitry for the clock source to function. Examples are: oscillator modules (ECH, ECM, ECL mode), quartz crystal resonators or ceramic resonators (LP, XT and HS modes).

Internal clock sources are contained within the oscillator module. The internal oscillator block has two internal oscillators and a dedicated Phase Lock Loop (PLL) that are used to generate internal system clock sources. The High-Frequency Internal Oscillator (HFINTOSC) can produce a range from 1 to 32 MHz. The Low-Frequency Internal Oscillator (LFINTOSC) generates a 31 kHz frequency. The external oscillator block can also be used with the PLL. See **Section 6.2.1.4 "4x PLL"** for more details.

The system clock can be selected between external or internal clock sources via the NOSC bits in the OSCCON1 register. See **Section 6.3 "Clock Switching"** for additional information.

6.2.1 EXTERNAL CLOCK SOURCES

An external clock source can be used as the device system clock by performing one of the following actions:

- Program the RSTOSC<2:0> bits in the Configuration Words to select an external clock source that will be used as the default system clock upon a device Reset
- Write the NOSC<2:0> and NDIV<4:0> bits in the OSCCON1 register to switch the system clock source

See **Section 6.3 "Clock Switching"**for more information.

6.2.1.1 EC Mode

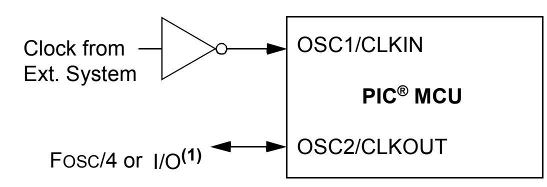
The External Clock (EC) mode allows an externally generated logic level signal to be the system clock source. When operating in this mode, an external clock source is connected to the OSC1 input. OSC2/CLKOUT is available for general purpose I/O or CLKOUT. Figure 6-2 shows the pin connections for EC mode.

EC mode has three power modes to select from through Configuration Words:

- ECH – High power, 4-32 MHz
- ECM – Medium power, 0.1-4 MHz
- ECL – Low power, 0-0.1 MHz

The Oscillator Start-up Timer (OST) is disabled when EC mode is selected. Therefore, there is no delay in operation after a Power-on Reset (POR) or wake-up from Sleep. Because the PIC® MCU design is fully static, stopping the external clock input will have the effect of halting the device while leaving all data intact. Upon restarting the external clock, the device will resume operation as if no time had elapsed.

FIGURE 6-2: EXTERNAL CLOCK (EC) MODE OPERATION



Note 1: Output depends upon $\overline{\text{CLKOUTEN}}$ bit of the Configuration Words.

6.2.1.2 LP, XT, HS Modes

The LP, XT and HS modes support the use of quartz crystal resonators or ceramic resonators connected to OSC1 and OSC2 (Figure 6-3). The three modes select a low, medium or high gain setting of the internal inverter-amplifier to support various resonator types and speed.

LP Oscillator mode selects the lowest gain setting of the internal inverter-amplifier. LP mode current consumption is the least of the three modes. This mode is designed to drive only 32.768 kHz tuning-fork type crystals (watch crystals).

XT Oscillator mode selects the intermediate gain setting of the internal inverter-amplifier. XT mode current consumption is the medium of the three modes. This mode is best suited to drive resonators with a medium drive level specification.

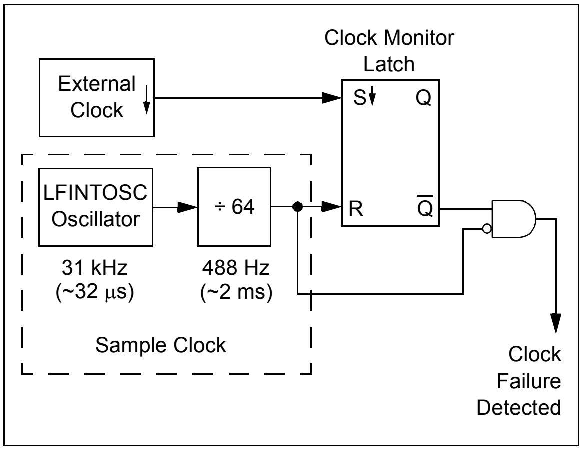
HS Oscillator mode selects the highest gain setting of the internal inverter-amplifier. HS mode current consumption is the highest of the three modes. This mode is best suited for resonators that require a high drive setting.

Figure 6-3 and Figure 6-4 show typical circuits for quartz crystal and ceramic resonators, respectively.

6.4 Fail-Safe Clock Monitor

The Fail-Safe Clock Monitor (FSCM) allows the device to continue operating should the external oscillator fail. The FSCM is enabled by setting the FCMEN bit in the Configuration Words. The FSCM is applicable to all external Oscillator modes (LP, XT, HS, EC and Secondary Oscillator).

FIGURE 6-9: FSCM BLOCK DIAGRAM



6.4.1 FAIL-SAFE DETECTION

The FSCM module detects a failed oscillator by comparing the external oscillator to the FSCM sample clock. The sample clock is generated by dividing the LFINTOSC by 64. See Figure 6-9. Inside the fail detector block is a latch. The external clock sets the latch on each falling edge of the external clock. The sample clock clears the latch on each rising edge of the sample clock. A failure is detected when an entire half-cycle of the sample clock elapses before the external clock goes low.

6.4.2 FAIL-SAFE OPERATION

When the external clock fails, the FSCM switches the device clock to the HFINTOSC at 1 MHz clock frequency and sets the bit flag OSFIF of the PIR1 register. Setting this flag will generate an interrupt if the OSFIE bit of the PIE1 register is also set. The device firmware can then take steps to mitigate the problems that may arise from a failed clock. The system clock will continue to be sourced from the internal clock source until the device firmware successfully restarts the external oscillator and switches back to external operation, by writing to the NOSC and NDIV bits of the OSCCON1 register.

6.4.3 FAIL-SAFE CONDITION CLEARING

The Fail-Safe condition is cleared after a Reset, executing a SLEEP instruction or changing the NOSC and NDIV bits of the OSCCON1 register. When switching to the external oscillator or PLL, the OST is restarted. While the OST is running, the device continues to operate from the INTOSC selected in OSCCON1. When the OST times out, the Fail-Safe condition is cleared after successfully switching to the external clock source. The OSFIF bit should be cleared prior to switching to the external clock source. If the Fail-Safe condition still exists, the OSFIF flag will again become set by hardware.

REGISTER 7-9: PIE7: PERIPHERAL INTERRUPT ENABLE REGISTER 7

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
SCANIE	CRCIE	NVMIE	NCO1IE	—	CWG3IE	CWG2IE	CWG1IE
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS = Hardware set

bit 7 **SCANIE:** Scanner Interrupt Enable bit
1 = Enables the scanner interrupt
0 = Disables the scanner interrupt

bit 6 **CRCIE:** CRC Interrupt Enable bit
1 = Enables the CRC interrupt
0 = Disables the CRC interrupt

bit 5 **NVMIE:** NVM Interrupt Enable bit
1 = NVM task complete interrupt enabled
0 = NVM interrupt not enabled

bit 4 **NCO1IE:** NCO Interrupt Enable bit
1 = NCO rollover interrupt enabled
0 = NCO rollover interrupt disabled

bit 3 **Unimplemented:** Read as '0'.

bit 2 **CWG3IE:** Complementary Waveform Generator (CWG) 3 Interrupt Enable bit
1 = CWG3 interrupt enabled
0 = CWG3 interrupt disabled

bit 1 **CWG2IE:** Complementary Waveform Generator (CWG) 2 Interrupt Enable bit
1 = CWG2 interrupt is enabled
0 = CWG2 interrupt disabled

bit 0 **CWG1IE:** Complementary Waveform Generator (CWG) 2 Interrupt Enable bit
1 = CWG1 interrupt is enabled
0 = CWG1 interrupt disabled

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt controlled by registers PIE1-PIE8.

REGISTER 7-17: PIR6: PERIPHERAL INTERRUPT REQUEST REGISTER 6

U-0	U-0	U-0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0
—	—	—	CCP5IF	CCP4IF	CCP3IF	CCP2IF	CCP1IF
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	HS = Hardware set

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4 **CCP5IF:** CCP5 Interrupt Flag bit

Value	CCPM Mode		
	Capture	Compare	PWM
1	Capture occurred (must be cleared in software)	Compare match occurred (must be cleared in software)	Output trailing edge occurred (must be cleared in software)
0	Capture did not occur	Compare match did not occur	Output trailing edge did not occur

bit 3 **CCP4IF:** CCP4 Interrupt Flag bit

Value	CCPM Mode		
	Capture	Compare	PWM
1	Capture occurred (must be cleared in software)	Compare match occurred (must be cleared in software)	Output trailing edge occurred (must be cleared in software)
0	Capture did not occur	Compare match did not occur	Output trailing edge did not occur

bit 2 **CCP3IF:** CCP3 Interrupt Flag bit

Value	CCPM Mode		
	Capture	Compare	PWM
1	Capture occurred (must be cleared in software)	Compare match occurred (must be cleared in software)	Output trailing edge occurred (must be cleared in software)
0	Capture did not occur	Compare match did not occur	Output trailing edge did not occur

bit 1 **CCP2IF:** CCP2 Interrupt Flag bit

Value	CCPM Mode		
	Capture	Compare	PWM
1	Capture occurred (must be cleared in software)	Compare match occurred (must be cleared in software)	Output trailing edge occurred (must be cleared in software)
0	Capture did not occur	Compare match did not occur	Output trailing edge did not occur

bit 0 **CCP1IF:** CCP1 Interrupt Flag bit

Value	CCPM Mode		
	Capture	Compare	PWM
1	Capture occurred (must be cleared in software)	Compare match occurred (must be cleared in software)	Output trailing edge occurred (must be cleared in software)
0	Capture did not occur	Compare match did not occur	Output trailing edge did not occur

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

TABLE 8-1: SUMMARY OF REGISTERS ASSOCIATED WITH POWER-DOWN MODE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	—	—	—	—	—	INTEDG	134
PIE0	—	—	TMR0IE	IOCIE	—	—	—	INTE	135
PIE1	OSFIE	CSWIE	—	—	—	—	ADTIE	ADIE	136
PIE2	—	ZCDIE	—	—	—	—	C2IE	C1IE	137
PIE3	—	—	RCIE	TXIE	BCL2IE	SSP2IE	BCL1IE	SSP1IE	138
PIE4	—	—	TMR6IE	TMR5IE	TMR4IE	TMR3IE	TMR2IE	TMR1IE	139
PIR0	—	—	TMR0IF	IOCIF	—	—	—	INTF	144
PIR1	OSFIF	CSWIF	—	—	—	—	ADTIF	ADIF	145
PIR2	—	ZCDIF	—	—	—	—	C2IF	C1IF	146
PIR3	—	—	RCIF	TXIF	BCL2IF	SSP2IF	BCL1IF	SSP1IF	147
PIR4	—	—	TMR6IF	TMR5IF	TMR4IF	TMR3IF	TMR2IF	TMR1IF	148
IOCAP	IOCAP7	IOCAP6	IOCAP5	IOCAP4	IOCAP3	IOCAP2	IOCAP1	IOCAP0	262
IOCAN	IOCAN7	IOCAN6	IOCAN5	IOCAN4	IOCAN3	IOCAN2	IOCAN1	IOCAN0	262
IOCAF	IOCAF7	IOCAF6	IOCAF5	IOCAF4	IOCAF3	IOCAF2	IOCAF1	IOCAF0	262
IOCCP	IOCCP7	IOCCP6	IOCCP5	IOCCP4	IOCCP3	IOCCP2	IOCCP1	IOCCP0	264
IOCBP	IOCBP7	IOCBP6	IOCBP5	IOCBP4	IOCBP3	IOCBP2	IOCBP1	IOCBP0	263
IOCBN	IOCBN7	IOCBN6	IOCBN5	IOCBN4	IOCBN3	IOCBN2	IOCBN1	IOCBN0	263
IOCBF	IOCBF7	IOCBF6	IOCBF5	IOCBF4	IOCBF3	IOCBF2	IOCBF1	IOCBF0	263
IOCCN	IOCCN7	IOCCN6	IOCCN5	IOCCN4	IOCCN3	IOCCN2	IOCCN1	IOCCN0	264
IOCCF	IOCCF7	IOCCF6	IOCCF5	IOCCF4	IOCCF3	IOCCF2	IOCCF1	IOCCF0	264
IOCEP	—	—	—	—	IOCEP3	—	—	—	265
IOCEN	—	—	—	—	IOCEN3	—	—	—	265
IOCEF	—	—	—	—	IOCEF3	—	—	—	266
STATUS	—	—	—	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	38
VREGCON	—	—	—	—	—	—	VREGPM	Reserved	159
CPUDOZE	IDLEN	DOZEN	ROI	DOE	—	DOZE<2:0>			160
WDTCON0	—	—	WDTPS<4:0>					SWDTEN	166
IOCEP	—	—	—	—	IOCEP3	—	—	—	265
IOCEN	—	—	—	—	IOCEN3	—	—	—	265
IOCEF	—	—	—	—	IOCEF3	—	—	—	266

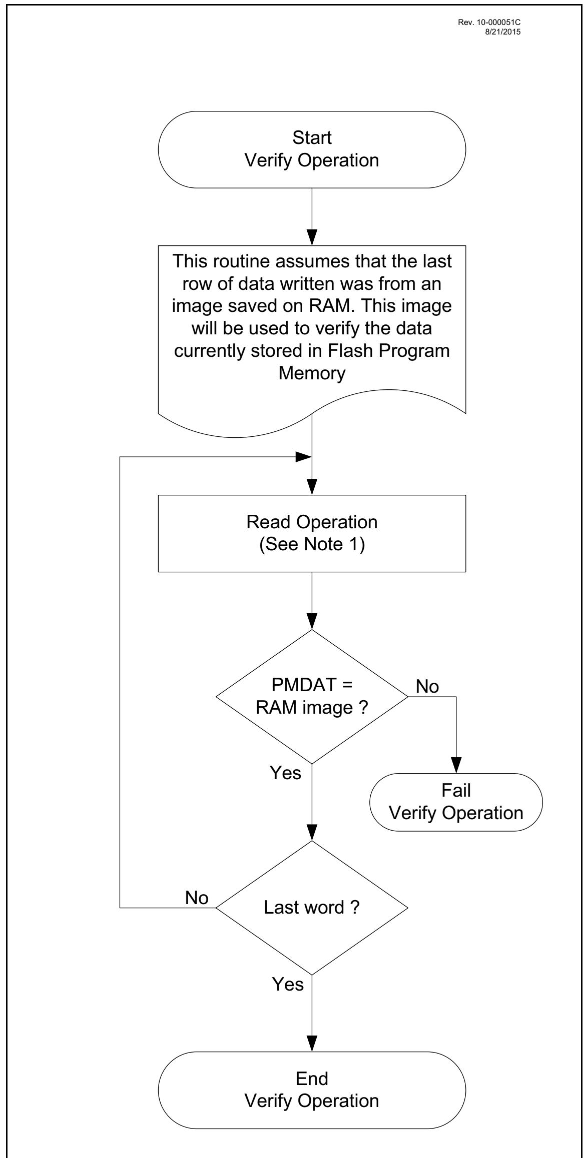
Legend: — = unimplemented location, read as '0'. Shaded cells are not used in Power-Down mode.

10.4.7 NVMREG DATA EEPROM MEMORY, USER ID, DEVICE ID AND CONFIGURATION WORD ACCESS

Instead of accessing Program Flash Memory (PFM), the Data EEPROM Memory, the User ID's, Device ID/ Revision ID and Configuration Words can be accessed when NVMREGS = `1` in the NVMCON1 register. This is the region that would be pointed to by PC<15> = `1`, but not all addresses are accessible. Different access may exist for reads and writes. Refer to Table 10-3.

When read access is initiated on an address outside the parameters listed in Table 10-3, the NVMDATH: NVMDATL register pair is cleared, reading back '`0`'s.

FIGURE 10-7: FLASH PROGRAM MEMORY MODIFY FLOWCHART



Note 1: See Figure 10-1.

TABLE 10-3: EEPROM, USER ID, DEV/REV ID AND CONFIGURATION WORD ACCESS (NVMREGS = 1)

Address	Function	Read Access	Write Access
8000h-8003h	User IDs	Yes	Yes
8005h-8006h	Device ID/Revision ID	Yes	No
8007h-800Bh	Configuration Words 1-5	Yes	No
F000h-F0FFh	EEPROM	Yes	Yes

REGISTER 10-5: NVMCON1: NONVOLATILE MEMORY CONTROL 1 REGISTER

U-0	R/W-0/0	R/W-0/0	R/W/HC-0/0	R/W/HC-x/q	R/W-0/0	R/S/HC-0/0	R/S/HC-0/0
—	NVMREGS	LWLO	FREE	WRERR(1,2,3)	WREN	WR(4,5,6)	RD(7)
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
S = Bit can only be set	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	HC = Bit is cleared by hardware

bit 7 **Unimplemented:** Read as ‘0’

bit 6 **NVMREGS:** Configuration Select bit
1 = Access EEPROM, Configuration, User ID and Device ID Registers
0 = Access PFM

bit 5 **LWLO:** Load Write Latches Only bit
When FREE = 0:
1 = The next WR command updates the write latch for this word within the row; no memory operation is initiated.
0 = The next WR command writes data or erases
Otherwise: The bit is ignored

bit 4 **FREE:** PFM Erase Enable bit
When NVMREGS:NVMADR points to a PFM location:
1 = Performs an erase operation with the next WR command; the 32-word pseudo-row containing the indicated address is erased (to all 1s) to prepare for writing.
0 = All write operations have completed normally

bit 3 **WRERR:** Program/Erase Error Flag bit(1,2,3)
This bit is normally set by hardware.
1 = A write operation was interrupted by a Reset, interrupted unlock sequence, or WR was written to one while NVMADR points to a write-protected address.
0 = The program or erase operation completed normally

bit 2 **WREN:** Program/Erase Enable bit
1 = Allows program/erase cycles
0 = Inhibits programming/erasing of program Flash

bit 1 **WR:** Write Control bit(4,5,6)
When NVMREG:NVMADR points to a EEPROM location:
1 = Initiates an erase/program cycle at the corresponding EEPROM location
0 = NVM program/erase operation is complete and inactive
When NVMREG:NVMADR points to a PFM location:
1 = Initiates the operation indicated by Table 10-4
0 = NVM program/erase operation is complete and inactive
Otherwise: This bit is ignored

bit 0 **RD:** Read Control bit(7)
1 = Initiates a read at address = NVMADR1, and loads data to NVMDAT Read takes one instruction cycle and the bit is cleared when the operation is complete. The bit can only be set (not cleared) in software.
0 = NVM read operation is complete and inactive

Note 1: Bit is undefined while WR = 1 (during the EEPROM write operation it may be ‘0’ or ‘1’).
2: Bit must be cleared by software; hardware will not clear this bit.
3: Bit may be written to ‘1’ by software in order to implement test sequences.
4: This bit can only be set by following the unlock sequence of **Section 10.4.2 “NVM Unlock Sequence”**.
5: Operations are self-timed, and the WR bit is cleared by hardware when complete.
6: Once a write operation is initiated, setting this bit to zero will have no effect.
7: Reading from EEPROM loads only NVMDATL<7:0> (Register 10-1).

REGISTER 12-6: WPUA: WEAK PULL-UP PORTA REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
WPUA7	WPUA6	WPUA5	WPUA4	WPUA3	WPUA2	WPUA1	WPUA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **WPUA<7:0>**: Weak Pull-up Register bits(1)
1 = Pull-up enabled
0 = Pull-up disabled

Note 1: The weak pull-up device is automatically disabled if the pin is configured as an output.

REGISTER 12-7: ODCONA: PORTA OPEN-DRAIN CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
ODCA7	ODCA6	ODCA5	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **ODCA<7:0>:** PORTA Open-Drain Enable bits
For RA<7:0> pins, respectively
1 = Port pin operates as open-drain drive (sink current only)
0 = Port pin operates as standard push-pull drive (source and sink current)

12.11 Register Definitions: PORTD

REGISTER 12-32: PORTD: PORTD REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **RD<7:0>**: PORTD I/O Value bits(1)
1 = Port pin is $\geq$ V_{IH}
0 = Port pin is $\leq$ V_{IL}

Note 1: Writes to PORTD are actually written to corresponding LATD register. Reads from PORTD register is return of actual I/O pin values.

REGISTER 12-33: TRISD: PORTD TRI-STATE REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **TRISD<7:0>**: TRISD I/O Value bits
1 = Port pin is $\geq$ V_{IH}
0 = Port pin is $\leq$ V_{IL}

REGISTER 18-3: CMxNSEL: COMPARATOR Cx NEGATIVE INPUT SELECT REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	—	NCH<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-2 **Unimplemented:** Read as ‘0’

bit 2-0 **NCH<2:0>:** Comparator Negative Input Channel Select bits
111 = CxVN connects to AVSS
110 = CxVN connects to FVR Buffer 2
101 = CxVN unconnected
100 = CxVN unconnected
011 = CxVN connects to CxIN3- pin
010 = CxVN connects to CxIN2- pin
001 = CxVN connects to CxIN1- pin
000 = CxVN connects to CxIN0- pin

REGISTER 18-4: CMxPSEL: COMPARATOR Cx POSITIVE INPUT SELECT REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	—	PCH<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-2 **Unimplemented:** Read as ‘0’

bit 5-3 **PCH<2:0>:** Comparator Positive Input Channel Select bits
111 = CxVP connects to AVSS
110 = CxVP connects to FVR Buffer 2
101 = CxVP connects to DAC output
100 = CxVP unconnected
011 = CxVP unconnected
010 = CxVP unconnected
001 = CxVP connects to CxIN1+ pin
000 = CxVP connects to CxIN0+ pin

REGISTER 20-7: CWGxSTR: CWGx STEERING CONTROL REGISTER[1]

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
OVRD	OVRC	OVRB	OVRA	STRD[2]	STRC[2]	STRB[2]	STRA[2]
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7 **OVRD:** Steering Data D bit

bit 6 **OVRC:** Steering Data C bit

bit 5 **OVRB:** Steering Data B bit

bit 4 **OVRA:** Steering Data A bit

bit 3 **STRD:** Steering Enable D bit[2]
1 = CWGxD output has the CWGx_data waveform with polarity control from POLD bit
0 = CWGxD output is assigned the value of OVRD bit

bit 2 **STRC:** Steering Enable C bit[2]
1 = CWGxC output has the CWGx_data waveform with polarity control from POLC bit
0 = CWGxC output is assigned the value of OVRC bit

bit 1 **STRB:** Steering Enable B bit[2]
1 = CWGxB output has the CWGx_data waveform with polarity control from POLB bit
0 = CWGxB output is assigned the value of OVRB bit

bit 0 **STRA:** Steering Enable A bit[2]
1 = CWGxA output has the CWGx_data waveform with polarity control from POLA bit
0 = CWGxA output is assigned the value of OVRA bit

Note 1: The bits in this register apply only when MODE<2:0> = 00x.
2: This bit is effectively double-buffered when MODE<2:0> = 001.

31.0 MASTER SYNCHRONOUS SERIAL PORT (MSSP) MODULES

31.1 MSSP Module Overview

The Master Synchronous Serial Port (MSSP) module is a serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be serial EEPROMs, shift registers, display drivers, A/D converters, etc. The MSSP module can operate in one of two modes:

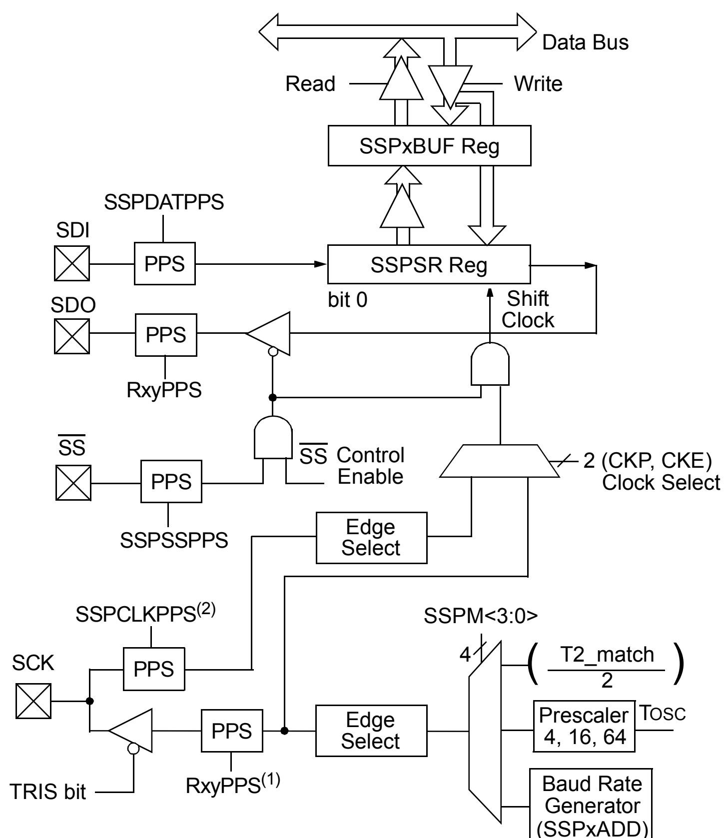
- Serial Peripheral Interface (SPI)
- Inter-Integrated Circuit (I^2C)

The SPI interface supports the following modes and features:

- Master mode
- Slave mode
- Clock Parity
- Slave Select Synchronization (Slave mode only)
- Daisy-chain connection of slave devices

Figure 31-1 is a block diagram of the SPI interface module.

FIGURE 31-1: MSSP BLOCK DIAGRAM (SPI MODE)



Note 1: Output selection for master mode

2: Input selection for slave mode

31.6.8 ACKNOWLEDGE SEQUENCE TIMING

An Acknowledge sequence is enabled by setting the Acknowledge Sequence Enable bit, ACKEN bit of the SSPxCON2 register. When this bit is set, the SCL pin is pulled low and the contents of the Acknowledge data bit are presented on the SDA pin. If the user wishes to generate an Acknowledge, then the ACKDT bit should be cleared. If not, the user should set the ACKDT bit before starting an Acknowledge sequence. The Baud Rate Generator then counts for one rollover period (TBRG) and the SCL pin is deasserted (pulled high). When the SCL pin is sampled high (clock arbitration), the Baud Rate Generator counts for TBRG. The SCL pin is then pulled low. Following this, the ACKEN bit is automatically cleared, the Baud Rate Generator is turned off and the MSSP module then goes into IDLE mode (Figure 31-30).

31.6.8.1 WCOL Status Flag

If the user writes the SSPxBUF when an Acknowledge sequence is in progress, then WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

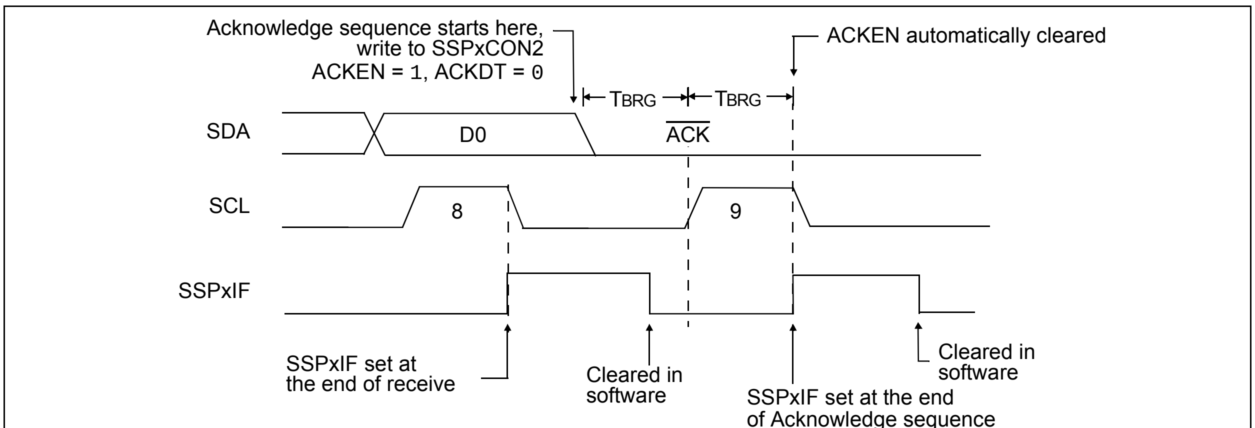
31.6.9 STOP CONDITION TIMING

A Stop bit is asserted on the SDA pin at the end of a receive/transmit by setting the Stop Sequence Enable bit, PEN bit of the SSPxCON2 register. At the end of a receive/transmit, the SCL line is held low after the falling edge of the ninth clock. When the PEN bit is set, the master will assert the SDA line low. When the SDA line is sampled low, the Baud Rate Generator is reloaded and counts down to '0'. When the Baud Rate Generator times out, the SCL pin will be brought high and one TBRG (Baud Rate Generator rollover count) later, the SDA pin will be deasserted. When the SDA pin is sampled high while SCL is high, the P bit of the SSPxSTAT register is set. A TBRG later, the PEN bit is cleared and the SSPxIF bit is set (Figure 31-31).

31.6.9.1 WCOL Status Flag

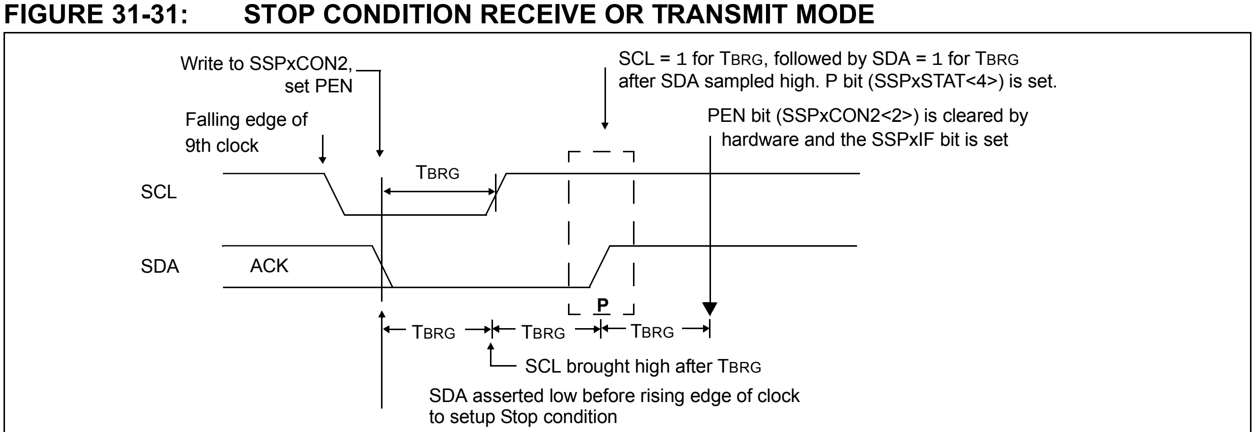
If the user writes the SSPxBUF when a Stop sequence is in progress, then the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

FIGURE 31-30: ACKNOWLEDGE SEQUENCE WAVEFORM



Note: TBRG = one Baud Rate Generator period.

FIGURE 31-31: STOP CONDITION RECEIVE OR TRANSMIT MODE



Note: TBRG = one Baud Rate Generator period.

FIGURE 32-11: WINDOWED MEASURE MODE SINGLE ACQUISITION TIMING DIAGRAM

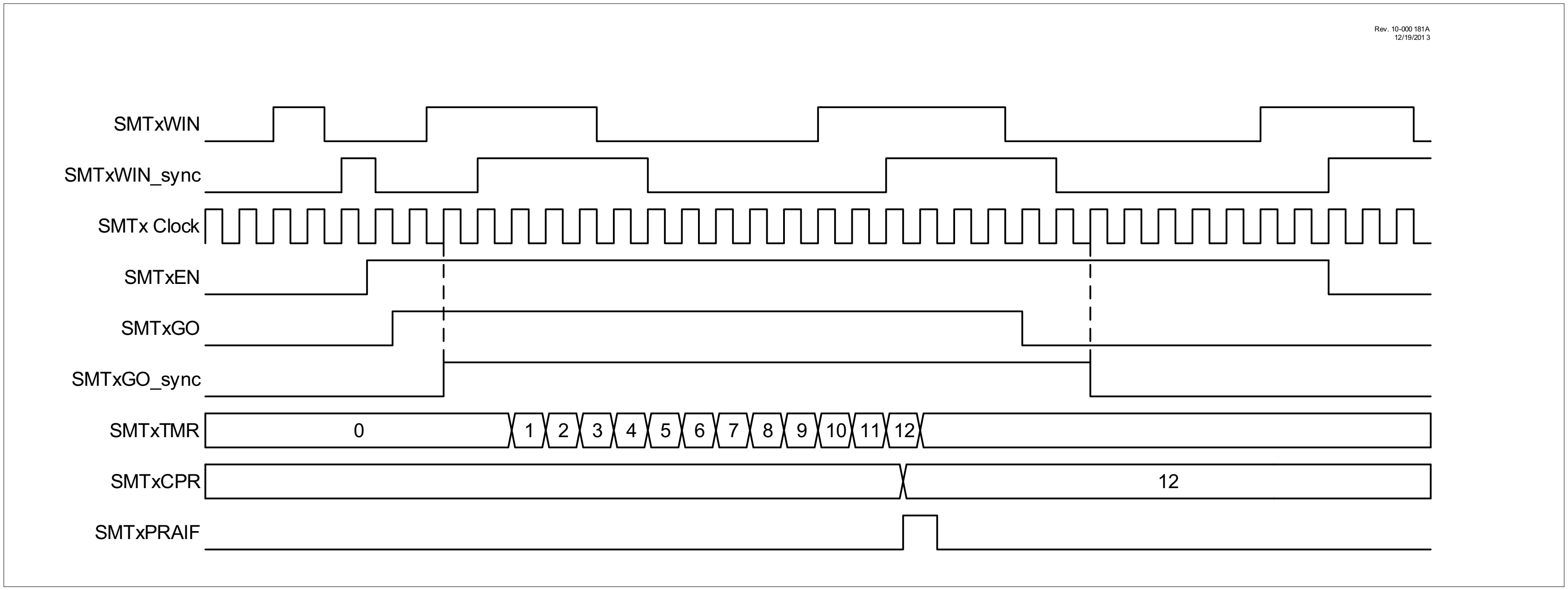


FIGURE 37-17: SPI MASTER MODE TIMING (CKE = 0, SMP = 0)

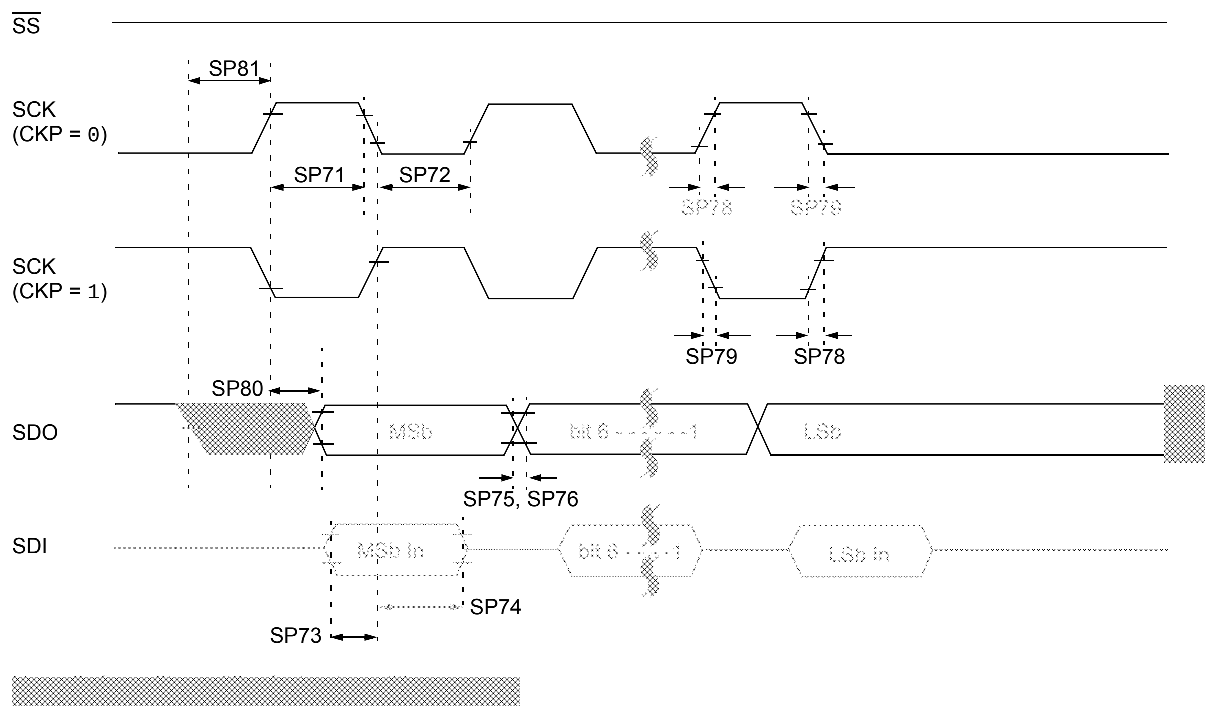
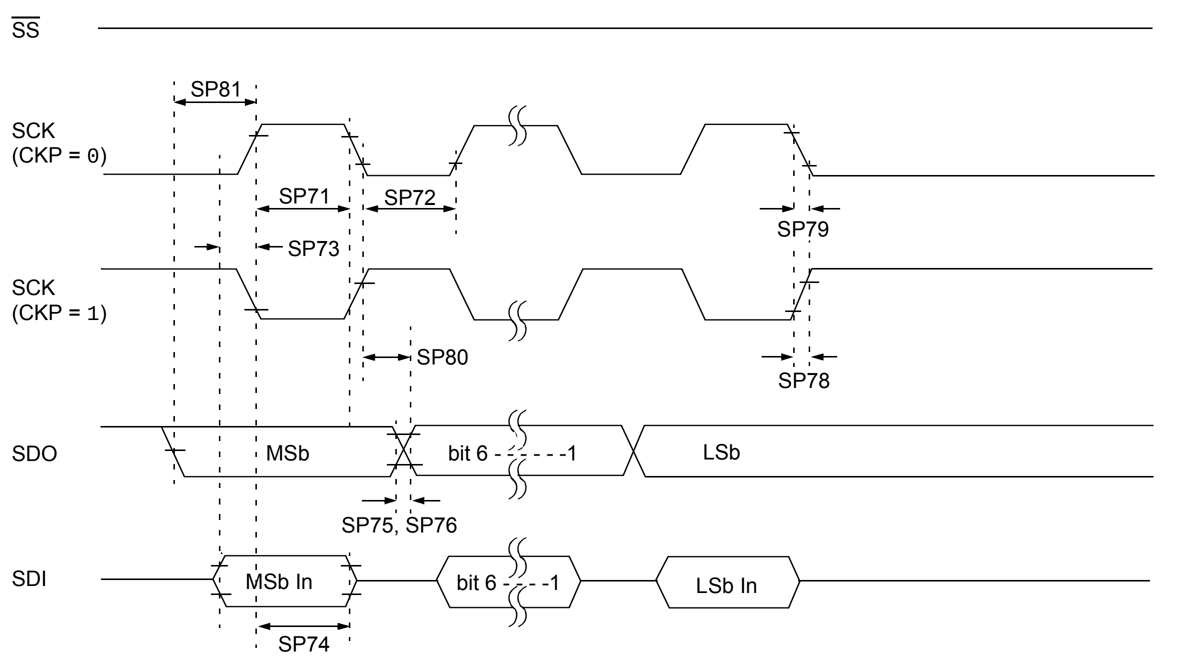


FIGURE 37-18: SPI MASTER MODE TIMING (CKE = 1, SMP = 1)



Note: Refer to Figure 37-4 for load conditions.

