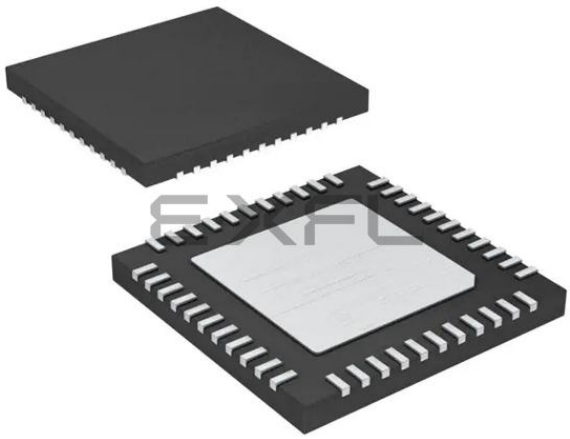

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	36
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 35x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf18875-i-ml

PIC16(L)F188XX Family Types

Device	Data Sheet Index	Program Flash Memory (Words)	Program Flash Memory (KB)	EEPROM (bytes)	Data SRAM (bytes)	I/O Pins[1]	10-Bit ADC[2] (ch)	5-Bit DAC	Comparator	8-Bit (with HLT)/ 16-Bit Timers	SMT	Windowed Watchdog Timer	CRC and Memory Scan	CCP/10-Bit PWM	Zero-Cross Detect	CWG	NCO	CLC	DSM	EUSART/I²C/SPI	Peripheral Pin Select	Peripheral Module Disable
PIC16(L)F18854	(1)	4096	7	256	512	25	24	1	2	3/4	2	Y	Y	5/2	Y	3	1	4	1	1/2	Y	Y
PIC16(L)F18855	(2)	8192	14	256	1024	25	24	1	2	3/4	2	Y	Y	5/2	Y	3	1	4	1	1/2	Y	Y
PIC16(L)F18856	(3)	16384	28	256	2048	25	24	1	2	3/4	2	Y	Y	5/2	Y	3	1	4	1	1/2	Y	Y
PIC16(L)F18857	(4)	32768	56	256	4096	25	24	1	2	3/4	2	Y	Y	5/2	Y	3	1	4	1	1/2	Y	Y
PIC16(L)F18875	(2)	8192	14	256	1024	36	35	1	2	3/4	2	Y	Y	5/2	Y	3	1	4	1	1/2	Y	Y
PIC16(L)F18876	(3)	16384	28	256	2048	36	35	1	2	3/4	2	Y	Y	5/2	Y	3	1	4	1	1/2	Y	Y
PIC16(L)F18877	(4)	32768	56	256	4096	36	35	1	2	3/4	2	Y	Y	5/2	Y	3	1	4	1	1/2	Y	Y

Note 1: One pin is input-only.

Data Sheet Index: (Unshaded devices are described in this document)

1: DS40001826 PIC16(L)F18854 Data Sheet, 28-Pin, Full-Featured 8-bit Microcontrollers
2: DS40001802 PIC16(L)F18855/75 Data Sheet, 28/40-Pin, Full-Featured 8-bit Microcontrollers
3: DS40001824 PIC16(L)F18856/76 Data Sheet, 28/40-Pin, Full-Featured 8-bit Microcontrollers
4: DS40001825 PIC16(L)F18857/77 Data Sheet, 28/40-Pin, Full-Featured 8-bit Microcontrollers

Note: For other small form-factor package availability and marking information, please visit **http://www.microchip.com/packaging** or contact your local sales office.

TABLE 3-6: PIC16F18855/75 MEMORY MAP BANK 16-23

	BANK 16		BANK 17		BANK 18		BANK 19		BANK 20		BANK 21		BANK 22		BANK 23	
800h	Core Registers (Table 3-2)	880h	Core Registers (Table 3-2)	900h	Core Registers (Table 3-2)	980h	Core Registers (Table 3-2)	A00h	Core Registers (Table 3-2)	A80h	Core Registers (Table 3-2)	B00h	Core Registers (Table 3-2)	B80h	Core Registers (Table 3-2)
80Bh		88Bh		90Bh		98Bh		A0Bh		A8Bh		B0Bh		B8Bh	
80Ch	WDTCON0	88Ch	CPUDOZE	90Ch	FVRCON	98Ch	—	A0Ch	Unimplemented Read as '0'	A8Ch	Unimplemented Read as '0'	B0Ch	Unimplemented Read as '0'	B8Ch	Unimplemented Read as '0'
80Dh	WDTCON1	88Dh	OSCCON1	90Dh	—	98Dh	—								
80Eh	WDTPSL	88Eh	OSCCON2	90Eh	DAC1CON0	98Eh	—								
80Fh	WDTPSH	88Fh	OSCCON3	90Fh	DAC1CON1	98Fh	CMOUT								
810h	WDTTMR	890h	OSCSTAT	910h	—	990h	CM1CON0								
811h	BORCON	891h	OSCEN	911h	—	991h	CM1CON1								
812h	VREGCON(1)	892h	OSCTUNE	912h	—	992h	CM1NSEL								
813h	PCON0	893h	OSCFRQ	913h	—	993h	CM1PSEL								
814h	CCDCON	894h	—	914h	—	994h	CM2CON0								
815h	—	895h	CLKRCON	915h	—	995h	CM2CON1								
816h	—	896h	CLKRCLK	916h	—	996h	CM2NSEL								
817h	—	897h	MDCON0	917h	—	997h	CM2PSEL								
818h	—	898h	MDCON1	918h	—	998h	—								
819h	—	899h	MDSRC	919h	—	999h	—								
81Ah	NVMADRL	89Ah	MDCARL	91Ah	—	99Ah	—								
81Bh	NVMADRH	89Bh	MDCARH	91Bh	—	99Bh	—								
81Ch	NVMDATL	89Ch	—	91Ch	—	99Ch	—								
81Dh	NVMDATH	89Dh	—	91Dh	—	99Dh	—								
81Eh	NVMCON1	89Eh	—	91Eh	—	99Eh	—								
81Fh	NVMCON2	89Fh	—	91Fh	ZCDCON	99Fh	—								
820h	Unimplemented Read as '0'	8A0h	Unimplemented Read as '0'	920h	Unimplemented Read as '0'	9A0h	Unimplemented Read as '0'								
86Fh		8EFh		96Fh		9EFh		A6Fh		AEFh		B6Fh		BEFh	
870h	Common RAM Accesses 70h – 7Fh	8F0h	Common RAM Accesses 70h – 7Fh	970h	Common RAM Accesses 70h – 7Fh	9F0h	Common RAM Accesses 70h – 7Fh	A70h	Common RAM Accesses 70h – 7Fh	AF0h	Common RAM Accesses 70h – 7Fh	B70h	Common RAM Accesses 70h – 7Fh	BF0h	Common RAM Accesses 70h – 7Fh
87Fh		8FFh		97Fh		9FFh		A7Fh		AFFh		B7Fh		BFFh	

Legend: = Unimplemented data memory locations, read as '0'.

Note 1: PIC16F18855/75 only.

TABLE 3-13: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-31 (CONTINUED)

Address	Name	PIC16(L)F18855	PIC16(L)F18875	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Bank 7													
CPU CORE REGISTERS; see Table 3-2 for specifics													
38Ch	PWM6DCL			DC<1:0>		—	—	—	—	—	—	xx-- ----	uu-- ----
38Dh	PWM6DCH			DC<9:2>								xxxx xxxx	uuuu uuuu
38Eh	PWM6CON			EN	—	OUT	POL	—	—	—	—	0-00 ----	0-00 ----
38Fh	—	—		Unimplemented								—	—
390h	PWM7DCL			DC<1:0>		—	—	—	—	—	—	xx-- ----	uu-- ----
391h	PWM7DCH			DC<9:2>								xxxx xxxx	uuuu uuuu
392h	PWM7CON			EN	—	OUT	POL	—	—	—	—	0-00 ----	0-00 ----
393h	—	—		Unimplemented								—	—
394h	—	—		Unimplemented								—	—
395h	—	—		Unimplemented								—	—
396h	—	—		Unimplemented								—	—
397h	—	—		Unimplemented								—	—
398h	—	—		Unimplemented								—	—
399h	—	—		Unimplemented								—	—
39Ah	—	—		Unimplemented								—	—
39Bh	—	—		Unimplemented								—	—
39Ch	—	—		Unimplemented								—	—
39Dh	—	—		Unimplemented								—	—
39Eh	—	—		Unimplemented								—	—
39Fh	—	—		Unimplemented								—	—

Legend: x = unknown, u = unchanged, q =depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Register present on PIC16F18855/75 devices only.

2: Unimplemented, read as '1'.

TABLE 3-13: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-31 (CONTINUED)

Address	Name	PIC16(L)F18855	PIC16(L)F18875	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Banks 15													
CPU CORE REGISTERS; see Table 3-2 for specifics													
78Ch	—	—		Unimplemented								—	—
78Dh	—	—		Unimplemented								—	—
78Eh	—	—		Unimplemented								—	—
78Fh	—	—		Unimplemented								—	—
790h	—	—		Unimplemented								—	—
791h	—	—		Unimplemented								—	—
792h	—	—		Unimplemented								—	—
793h	—	—		Unimplemented								—	—
794h	—	—		Unimplemented								—	—
795h	—	—		Unimplemented								—	—
796h	PMD0			SYSCMD	FVRMD	—	CRCMD	SCANMD	NVMMD	CLKRMD	IOCMD	00-0 0000	00-0 0000
797h	PMD1			NCOMD	TMR6MD	TMR5MD	TMR4MD	TMR3MD	TMR2MD	TMR1MD	TMR0MD	0000 0000	0000 0000
798h	PMD2			—	DACMD	ADCMD	—	—	CMP2MD	CMP1MD	ZCDMD	-00- -000	-00- -000
799h	PMD3			—	PWM7MD	PWM6MD	CCP5MD	CCP4MD	CCP3MD	CCP2MD	CCP1MD	-000 0000	-000 0000
79Ah	PMD4			—	UART1MD	MSSP2MD	MSSP1MD	—	CWG3MD	CWG2MD	CWG1MD	-000 -000	-000 -000
79Bh	PMD5			SMT2MD	SMT1MD	—	CLC4MD	CLC3MD	CLC2MD	CLC1MD	DSMMD	00-0 0000	00-0 0000
79Ch	—	—		Unimplemented								—	—
79Dh	—	—		Unimplemented								—	—
79Eh	—	—		Unimplemented								—	—
79Fh	—	—		Unimplemented								—	—

Legend: x = unknown, u = unchanged, q =depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Register present on PIC16F18855/75 devices only.

2: Unimplemented, read as '1'.

TABLE 3-13: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-31 (CONTINUED)

Address	Name	PIC16(L)F18855	PIC16(L)F18875	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Bank 29 (Continued)													
EBAh	MDSRCPPS			—	—	—	MDSRCPPS<4:0>					---0 0101	---u uuuu
EBBh	CLCIN0PPS			—	—	—	CLCIN0PPS<4:0>					---0 0000	---u uuuu
EBCh	CLCIN1PPS			—	—	—	CLCIN1PPS<4:0>					---0 0001	---u uuuu
EBDh	CLCIN2PPS			—	—	—	CLCIN2PPS<4:0>					---0 1110	---u uuuu
EBEh	CLCIN3PPS			—	—	—	CLCIN3PPS<4:0>					---0 1111	---u uuuu
EBFh	—	—		Unimplemented								—	—
EC0h	—	—		Unimplemented								—	—
EC1h	—	—		Unimplemented								—	—
EC2h	—	—		Unimplemented								—	—
EC3h	ADCACTPPS			—	—	—	ADCACTPPS<4:0>					---0 1100	---u uuuu
EC4h	—	—		Unimplemented								—	—
EC5h	SSP1CLKPPS			—	—	—	SSP1CLKPPS<4:0>					---1 0011	---u uuuu
EC6h	SSP1DATPPS			—	—	—	SSP1DATPPS<4:0>					---1 0100	---u uuuu
EC7h	SSP1SSPPS			—	—	—	SSP1SSPPS<4:0>					---0 0101	---u uuuu
EC8h	SSP2CLKPPS			—	—	—	SSP2CLKPPS<4:0>					---0 1001	---u uuuu
EC9h	SSP2DATPPS			—	—	—	SSP2DATPPS<4:0>					---0 0010	---u uuuu
ECAh	SSP2SSPPS			—	—	—	SSP2SSPPS<4:0>					---0 1000	---u uuuu
ECBh	RXPPS			—	—	—	RXPPS<4:0>					---1 0111	---u uuuu
ECCh	TXPPS			—	—	—	TXPPS<4:0>					---1 0110	---u uuuu
ECDh to EEFh	—	—		Unimplemented								—	—

Legend: x = unknown, u = unchanged, q =depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Register present on PIC16F18855/75 devices only.

2: Unimplemented, read as '1'.

3.5.1 TRADITIONAL DATA MEMORY

The traditional data memory is a region from FSR address 0x000 to FSR address 0xFFF. The addresses correspond to the absolute addresses of all SFR, GPR and common registers.

REGISTER 4-3: CONFIG3: CONFIGURATION WORD 3: WINDOWED WATCHDOG

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
WDTCCS<2:0>			WDTCWS<2:0>		
bit 13					bit 8

U-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
	WDTE<1:0>		WDTCPS<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	P = Programmable bit	x = Bit is unknown	U = Unimplemented bit, read as ‘1’
‘0’ = Bit is cleared	‘1’ = Bit is set	W = Writable bit	n = Value when blank or after Bulk Erase

bit 13-11 **WDTCCS<2:0>**: WDT Input Clock Selector bits
- 111 = Software Control
- 110 = Reserved
- .
- .
- .
- 010 = Reserved
- 001 = WDT reference clock is the MFINTOSC/16 output (31.25 kHz)
- 000 = WDT reference clock is the 31.0 kHz LFINTOSC (default value)

bit 10-8 **WDTCWS<2:0>**: WDT Window Select bits

WDTCWS	WDTWS at POR			Software control of WDTWS?	Keyed access required?
	Value	Window delay Percent of time	Window opening Percent of time		
111	111	n/a	100	Yes	No
110	111	n/a	100	No	Yes
101	101	25	75		
100	100	37.5	62.5		
011	011	50	50		
010	010	62.5	37.5		
001	001	75	25		
000	000	87.5	12.5		

bit 7 **Unimplemented**: Read as ‘1’

bit 6-5 **WDTE<1:0>**: WDT Operating mode:
- 11 = WDT enabled regardless of Sleep; SWDTEN is ignored
- 10 = WDT enabled while Sleep = 0, suspended when Sleep = 1; SWDTEN ignored
- 01 = WDT enabled/disabled by SWDTEN bit in WDTCON0
- 00 = WDT disabled, SWDTEN is ignored

REGISTER 11-7: CRCSHIFTH: CRC SHIFT HIGH BYTE REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
SHIFT<15:8>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **SHIFT<15:8>**: CRC Shifter Register bits
Reading from this register reads the CRC Shifter.

REGISTER 11-8: CRCSHIFTL: CRC SHIFT LOW BYTE REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
SHIFT<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **SHIFT<7:0>**: CRC Shifter Register bits
Reading from this register reads the CRC Shifter.

REGISTER 11-9: CRCXORH: CRC XOR HIGH BYTE REGISTER

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
X<15:8>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **X<15:8>**: XOR of Polynomial Term X_N Enable bits

REGISTER 11-10: CRCXORL: CRC XOR LOW BYTE REGISTER

R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	R/W-x/x	U-1
X<7:1>							—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-1 **XOR<7:1>**: XOR of Polynomial Term X_N Enable bits
bit 0 **Unimplemented:** Read as '1'

REGISTER 12-6: WPUA: WEAK PULL-UP PORTA REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
WPUA7	WPUA6	WPUA5	WPUA4	WPUA3	WPUA2	WPUA1	WPUA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **WPUA<7:0>**: Weak Pull-up Register bits(1)
1 = Pull-up enabled
0 = Pull-up disabled

Note 1: The weak pull-up device is automatically disabled if the pin is configured as an output.

REGISTER 12-7: ODCONA: PORTA OPEN-DRAIN CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
ODCA7	ODCA6	ODCA5	ODCA4	ODCA3	ODCA2	ODCA1	ODCA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **ODCA<7:0>:** PORTA Open-Drain Enable bits
For RA<7:0> pins, respectively
1 = Port pin operates as open-drain drive (sink current only)
0 = Port pin operates as standard push-pull drive (source and sink current)

REGISTER 12-30: CCDPC: CURRENT CONTROLLED DRIVE POSITIVE PORTC REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
CCDPC7	CCDPC6	CCDPC5	CCDPC4	CCDPC3	CCDPC2	CCDPC1	CCDPC0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **CCDPC<7:0>:** RC<7:0> Current Controlled Drive Positive Control bits(1)
- 1 = Current-controlled source enabled
- 0 = Current-controlled source disabled

Note 1: If CCDPCy is set, when CCDEN = 0 (Register 12-1), operation of the pin is undefined.

REGISTER 12-31: CCDNC: CURRENT CONTROLLED DRIVE NEGATIVE PORTC REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
CCDNC7	CCDNC6	CCDNC5	CCDNC4	CCDNC3	CCDNC2	CCDNC1	CCDNC0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **CCDNC<7:0>:** RC<7:0> Current Controlled Drive Negative Control bits(1)
- 1 = Current-controlled source enabled
- 0 = Current-controlled source disabled

Note 1: If CCDNCy is set, when CCDEN = 0 (Register 12-1), operation of the pin is undefined.

12.14.8 CURRENT-CONTROLLED DRIVE MODE CONTROL

The CCDPE and CCDNE registers (Register 12-53 and Register 12-54) control the Current-Controlled Drive mode for both the positive-going and negative-going drivers. When a CCDPE[y] or CCDNE[y] bit is set and the CCDEN bit of the CCDCON register is set, the Current-Controlled mode is enabled for the corresponding port pin. When the CCDPE[y] or CCDNE[y] bit is clear, the Current-Controlled mode for the corresponding port pin is disabled. If the CCDPE[y] or CCDNE[y] bit is set and the CCDEN bit is clear, operation of the port pin is undefined (see **Section 12.1.1 "Current-Controlled Drive"** for current-controlled use precautions).

12.14.9 PORTE FUNCTIONS AND OUTPUT PRIORITIES

Each pin defaults to the PORT latch data after Reset. Other output functions are selected with the peripheral pin select logic. See **Section 13.0 "Peripheral Pin Select (PPS) Module"** for more information.

Analog input functions, such as ADC and comparator inputs, are not shown in the peripheral pin select lists. Digital output functions may continue to control the pin when it is in Analog mode.

12.14.10 PORTE FUNCTIONS AND OUTPUT PRIORITIES

Each pin defaults to the PORT latch data after Reset. Other output functions are selected with the peripheral pin select logic. See **Section 13.0 "Peripheral Pin Select (PPS) Module"** for more information.

Analog input functions, such as ADC and comparator inputs, are not shown in the peripheral pin select lists. Digital output functions may continue to control the pin when it is in Analog mode.

REGISTER 20-2: CWGxCON1: CWGx CONTROL REGISTER 1

U-0	U-0	R-x	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	IN	—	POLD	POLC	POLB	POLA
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **IN:** CWG Input Value

bit 4 **Unimplemented:** Read as '0'

bit 3 **POLD:** CWGxD Output Polarity bit
1 = Signal output is inverted polarity
0 = Signal output is normal polarity

bit 2 **POLC:** CWGxC Output Polarity bit
1 = Signal output is inverted polarity
0 = Signal output is normal polarity

bit 1 **POLB:** CWGxB Output Polarity bit
1 = Signal output is inverted polarity
0 = Signal output is normal polarity

bit 0 **POLA:** CWGxA Output Polarity bit
1 = Signal output is inverted polarity
0 = Signal output is normal polarity

REGISTER 28-2: TxGCON: TIMER1/3/5 GATE CONTROL REGISTER

R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u	R/W/HC-0/u	R-x/x	U-0	U-0
GE	GPOL	GTM	GSPM	GGO/$\overline{\text{DONE}}$	GVAL	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	HC = Bit is cleared by hardware

bit 7 **GE:** Timer1 Gate Enable bit

If ON = 0:
This bit is ignored
If ON = 1:
1 = Timer1 counting is controlled by the Timer1 gate function
0 = Timer1 is always counting

bit 6 **GPOL:** Timer1 Gate Polarity bit

1 = Timer1 gate is active-high (Timer1 counts when gate is high)
0 = Timer1 gate is active-low (Timer1 counts when gate is low)

bit 5 **GTM:** Timer1 Gate Toggle Mode bit

1 = Timer1 Gate Toggle mode is enabled
0 = Timer1 Gate Toggle mode is disabled and toggle flip-flop is cleared
Timer1 gate flip-flop toggles on every rising edge.

bit 4 **GSPM:** Timer1 Gate Single-Pulse Mode bit

1 = Timer1 Gate Single-Pulse mode is enabled and is controlling Timer1 gate
0 = Timer1 Gate Single-Pulse mode is disabled

bit 3 **GGO/$\overline{\text{DONE}}$:** Timer1 Gate Single-Pulse Acquisition Status bit

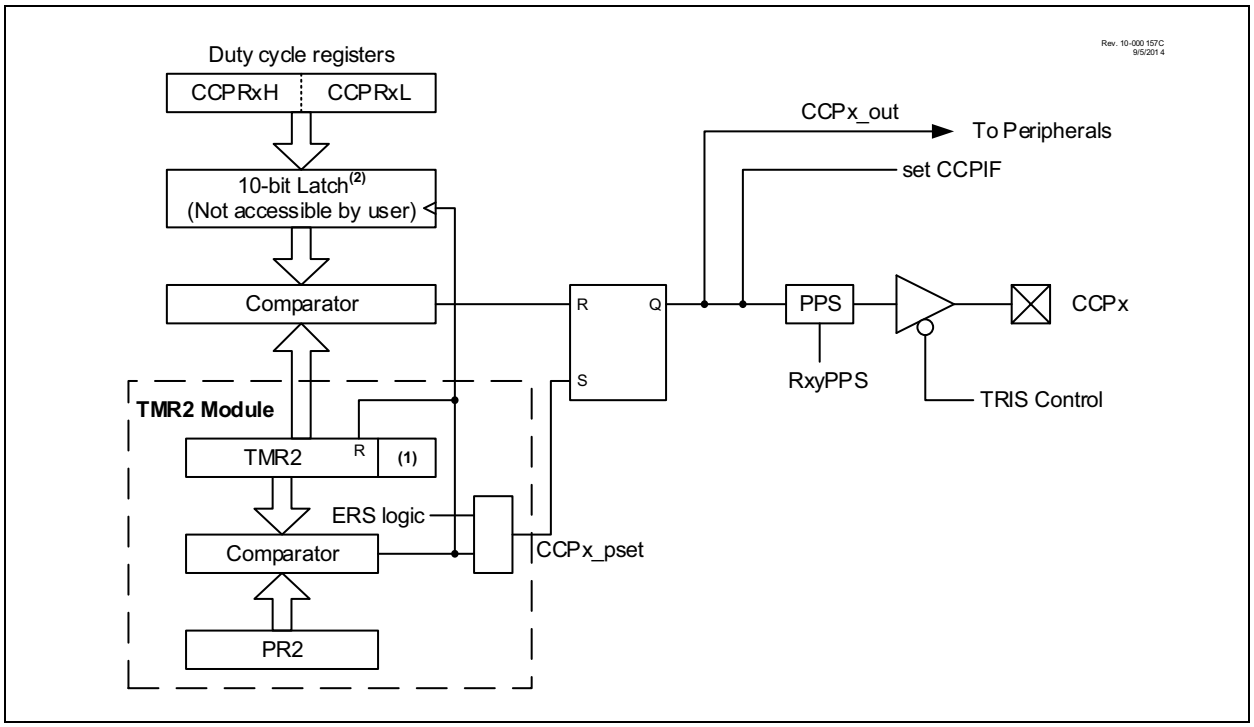
1 = Timer1 gate single-pulse acquisition is ready, waiting for an edge
0 = Timer1 gate single-pulse acquisition has completed or has not been started
This bit is automatically cleared when GSPM is cleared

bit 2 **GVAL:** Timer1 Gate Value Status bit

Indicates the current state of the Timer1 gate that could be provided to TMR1H:TMR1L
Unaffected by Timer1 Gate Enable (GE)

bit 1-0 **Unimplemented:** Read as ‘0’

FIGURE 30-4: SIMPLIFIED PWM BLOCK DIAGRAM



30.3.2 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for standard PWM operation:

1. Use the desired output pin RxyPPS control to select CCPx as the source and disable the CCPx pin output driver by setting the associated TRIS bit.
2. Load the PR2 register with the PWM period value.
3. Configure the CCP module for the PWM mode by loading the CCPxCON register with the appropriate values.
4. Load the CCPRxL register, and the CCPRxH register with the PWM duty cycle value and configure the CCPxFMT bit of the CCPxCON register to set the proper register alignment.
5. Configure and start Timer2:
   - Clear the TMR2IF interrupt flag bit of the PIR4 register. See Note below.
   - Configure the T2CKPS bits of the T2CON register with the Timer prescale value.
   - Enable the Timer by setting the TMR2ON bit of the T2CON register.
6. Enable PWM output pin:
   - Wait until the Timer overflows and the TMR2IF bit of the PIR4 register is set. See Note below.
   - Enable the CCPx pin output driver by clearing the associated TRIS bit.

Note:	In order to send a complete duty cycle and period on the first PWM output, the above steps must be included in the setup sequence. If it is not critical to start with a complete PWM signal on the first output, then step 6 may be ignored.

30.3.3 CCP/PWM CLOCK SELECTION

The PIC16F18855/75 allows each individual CCP and PWM module to select the timer source that controls the module. Each module has an independent selection.

As there are up to three 8-bit timers with auto-reload (Timer2/4/6), PWM mode on the CCP and PWM modules can use any of these timers. The CCPTMRS0 and CCPTMRS1 registers is used to select which timer is used.

31.5.6 CLOCK STRETCHING

Clock stretching occurs when a device on the bus holds the SCL line low, effectively pausing communication. The slave may stretch the clock to allow more time to handle data or prepare a response for the master device. A master device is not concerned with stretching as anytime it is active on the bus and not transferring data it is stretching. Any stretching done by a slave is invisible to the master software and handled by the hardware that generates SCL.

The CKP bit of the SSPxCON1 register is used to control stretching in software. Any time the CKP bit is cleared, the module will wait for the SCL line to go low and then hold it. Setting CKP will release SCL and allow more communication.

31.5.6.1 Normal Clock Stretching

Following an $\overline{ACK}$ if the R/$\overline{W}$ bit of SSPxSTAT is set, a read request, the slave hardware will clear CKP. This allows the slave time to update SSPxBUF with data to transfer to the master. If the SEN bit of SSPxCON2 is set, the slave hardware will always stretch the clock after the $\overline{ACK}$ sequence. Once the slave is ready; CKP is set by software and communication resumes.

Note 1: The BF bit has no effect on if the clock will be stretched or not. This is different than previous versions of the module that would not stretch the clock, clear CKP, if SSPxBUF was read before the ninth falling edge of SCL.

2: Previous versions of the module did not stretch the clock for a transmission if SSPxBUF was loaded before the ninth falling edge of SCL. It is now always cleared for read requests.

31.5.6.2 10-bit Addressing Mode

In 10-bit Addressing mode, when the UA bit is set the clock is always stretched. This is the only time the SCL is stretched without CKP being cleared. SCL is released immediately after a write to SSPxADD.

Note: Previous versions of the module did not stretch the clock if the second address byte did not match.

31.5.6.3 Byte NACKing

When AHEN bit of SSPxCON3 is set; CKP is cleared by hardware after the eighth falling edge of SCL for a received matching address byte. When DHEN bit of SSPxCON3 is set; CKP is cleared after the eighth falling edge of SCL for received data.

Stretching after the eighth falling edge of SCL allows the slave to look at the received address or data and decide if it wants to ACK the received data.

31.5.7 CLOCK SYNCHRONIZATION AND THE CKP BIT

Any time the CKP bit is cleared, the module will wait for the SCL line to go low and then hold it. However, clearing the CKP bit will not assert the SCL output low until the SCL output is already sampled low. Therefore, the CKP bit will not assert the SCL line until an external I^2C master device has already asserted the SCL line. The SCL output will remain low until the CKP bit is set and all other devices on the I^2C bus have released SCL. This ensures that a write to the CKP bit will not violate the minimum high time requirement for SCL (see Figure 31-23).

FIGURE 31-23: CLOCK SYNCHRONIZATION TIMING

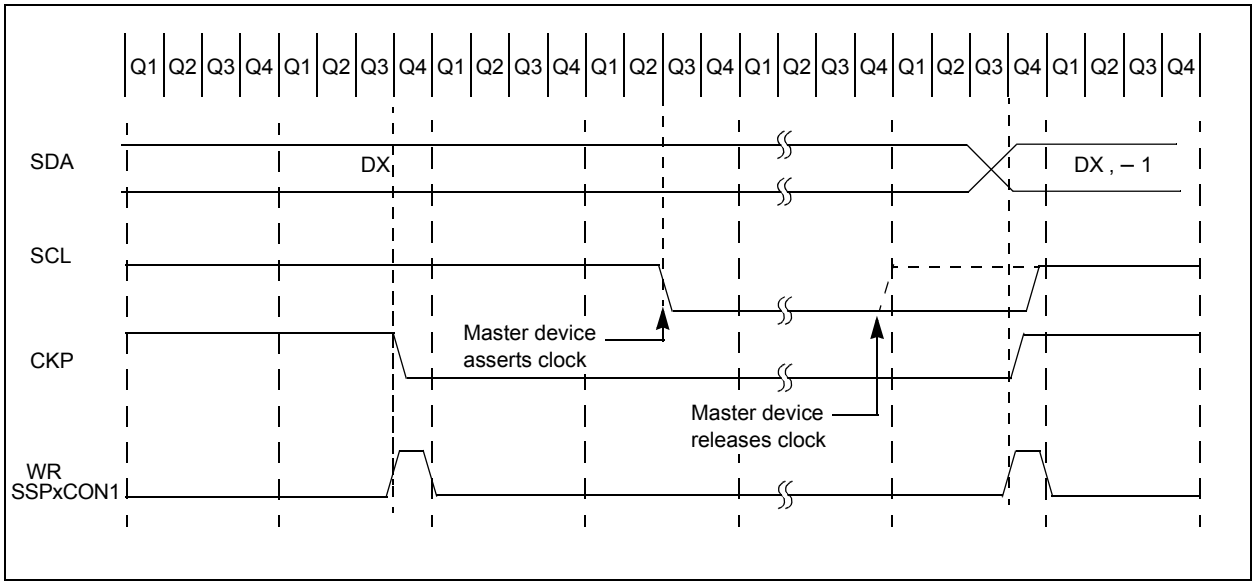
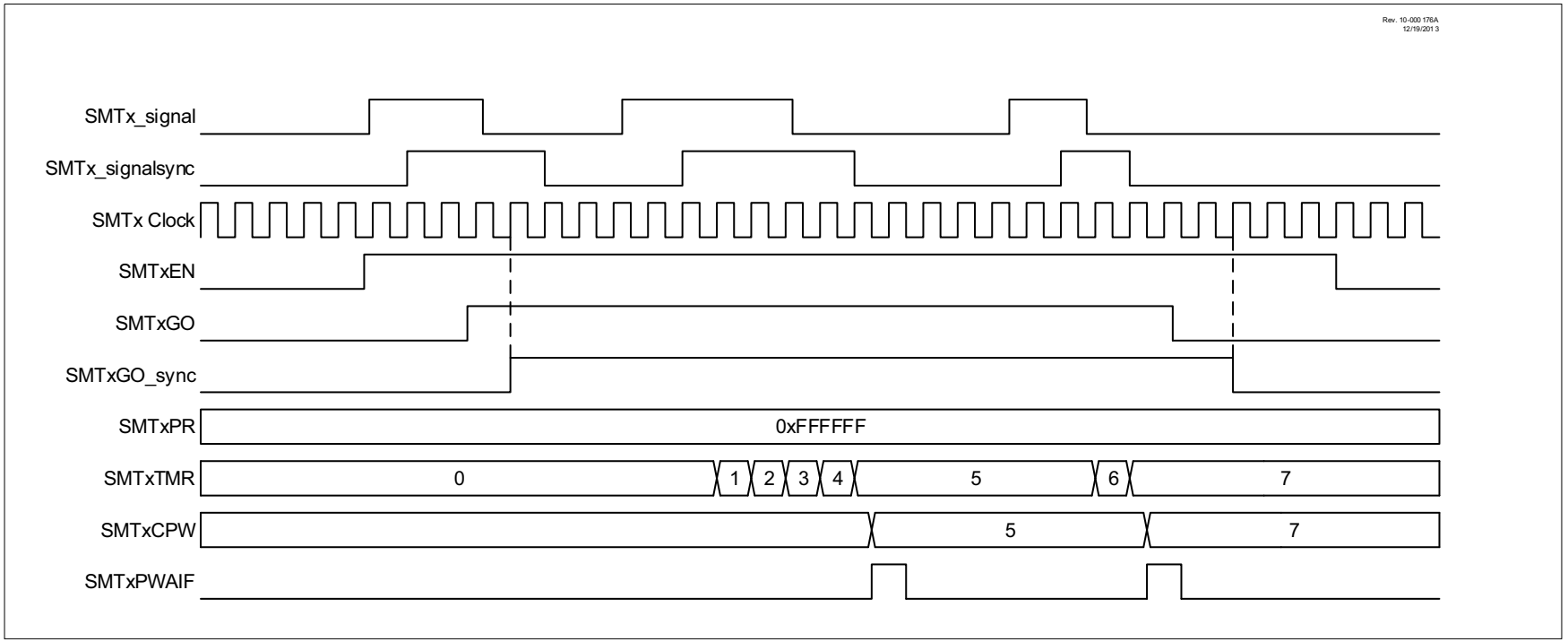


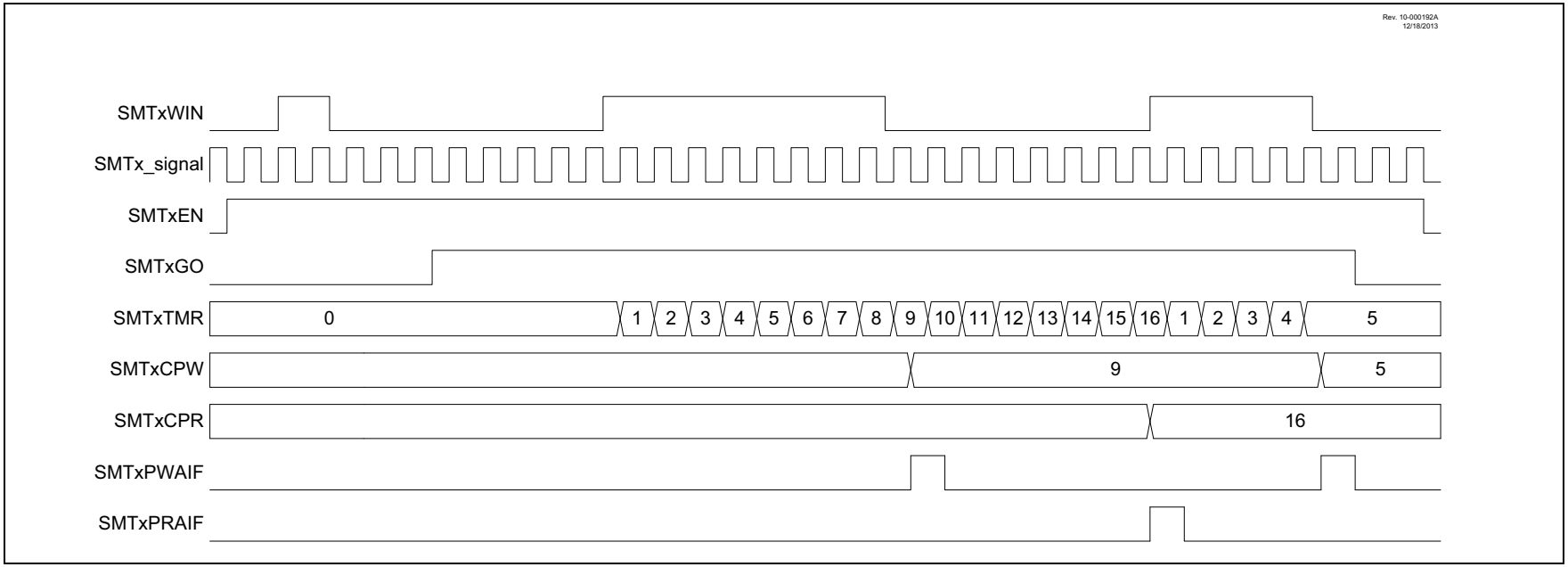
FIGURE 32-4: GATED TIMER MODE REPEAT ACQUISITION TIMING DIAGRAM



32.6.10 GATED COUNTER MODE

This mode counts pulses on the SMTx_signal input, gated by the SMTxWIN input. It begins incrementing the timer upon seeing a rising edge of the SMTxWIN input and updates the SMTxCPW register upon a falling edge on the SMTxWIN input. See Figure 32-19 and Figure 32-20.

FIGURE 32-21: WINDOWED COUNTER MODE REPEAT ACQUISITION TIMING DIAGRAM



35.0 IN-CIRCUIT SERIAL PROGRAMMING™ (ICSP™)

ICSP™ programming allows customers to manufacture circuit boards with unprogrammed devices. Programming can be done after the assembly process, allowing the device to be programmed with the most recent firmware or a custom firmware. Five pins are needed for ICSP™ programming:

- ICSPCLK
- ICSPDAT
- $\overline{MCLR}/V_{PP}$
- V_{DD}
- V_{SS}

In Program/Verify mode the program memory, User IDs and the Configuration Words are programmed through serial communications. The ICSPDAT pin is a bidirectional I/O used for transferring the serial data and the ICSPCLK pin is the clock input. For more information on ICSP™ refer to the **"***PIC16(L)F1783XX Memory Programming Specification***"** (DS400001738).

35.1 High-Voltage Programming Entry Mode

The device is placed into High-Voltage Programming Entry mode by holding the ICSPCLK and ICSPDAT pins low then raising the voltage on $\overline{MCLR}/V_{PP}$ to V_{IHH}.

35.2 Low-Voltage Programming Entry Mode

The Low-Voltage Programming Entry mode allows the PIC® Flash MCUs to be programmed using V_{DD} only, without high voltage. When the LVP bit of Configuration Words is set to '1', the low-voltage ICSP programming entry is enabled. To disable the Low-Voltage ICSP mode, the LVP bit must be programmed to '0'.

Entry into the Low-Voltage Programming Entry mode requires the following steps:

1. $\overline{MCLR}$ is brought to V_{IL}.
2. A 32-bit key sequence is presented on ICSPDAT, while clocking ICSPCLK.

Once the key sequence is complete, $\overline{MCLR}$ must be held at V_{IL} for as long as Program/Verify mode is to be maintained.

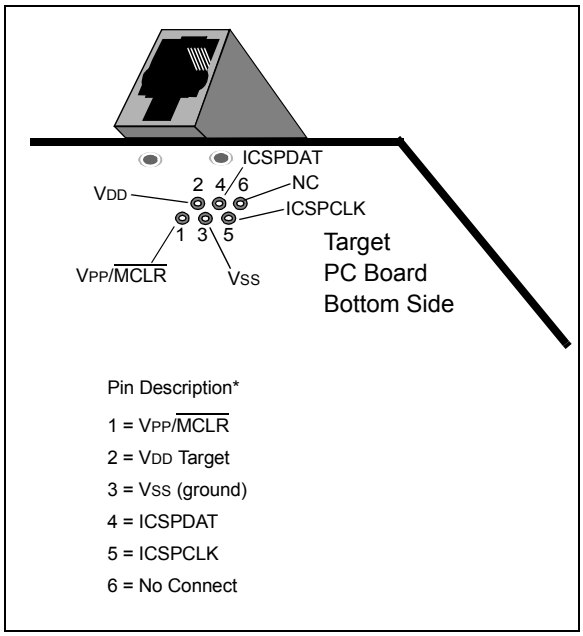
If low-voltage programming is enabled (LVP = 1), the $\overline{MCLR}$ Reset function is automatically enabled and cannot be disabled. See **Section 5.4 "MCLR"** for more information.

The LVP bit can only be reprogrammed to '0' by using the High-Voltage Programming mode.

35.3 Common Programming Interfaces

Connection to a target device is typically done through an ICSP™ header. A commonly found connector on development tools is the RJ-11 in the 6P6C (6-pin, 6-connector) configuration. See Figure 35-1.

FIGURE 35-1: ICD RJ-11 STYLE CONNECTOR INTERFACE



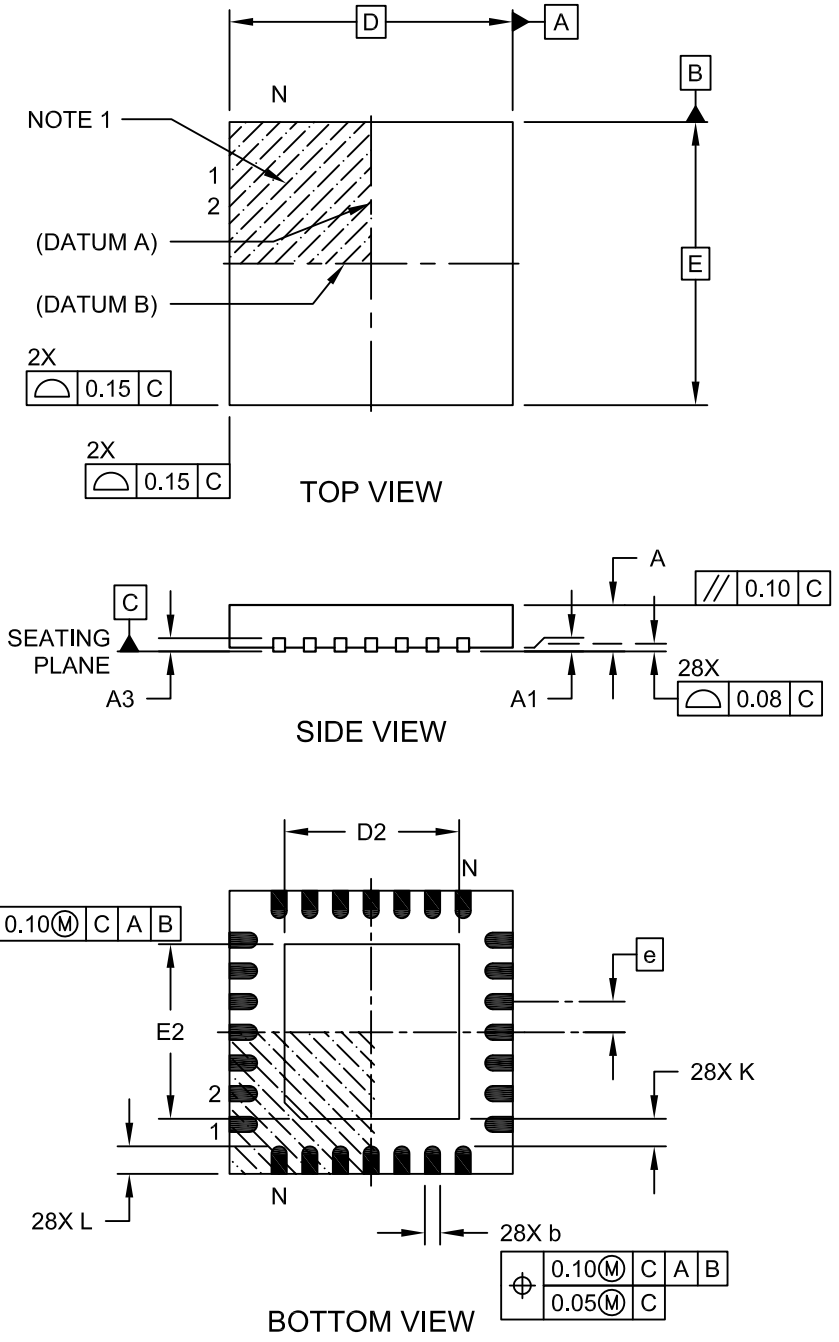
Another connector often found in use with the PICkit™ programmers is a standard 6-pin header with 0.1 inch spacing. Refer to Figure 35-2.

For additional interface recommendations, refer to your specific device programmer manual prior to PCB design.

It is recommended that isolation devices be used to separate the programming pins from other circuitry. The type of isolation is highly dependent on the specific application and may include devices such as resistors, diodes, or even jumpers. See Figure 35-3 for more information.

28-Lead Plastic Quad Flat, No Lead Package (ML) - 6x6 mm Body [QFN]
With 0.55 mm Terminal Length

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-105C Sheet 1 of 2