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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	EBI/EMI, I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	78
Program Memory Size	128KB (64K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-VFBGA
Supplier Device Package	100-VFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega128a1u-c7ur

1. Ordering Information

Ordering code	Flash (bytes)	EEPROM (bytes)	SRAM (bytes)	Speed (MHz)	Power supply	Package (1)(2)(3)	Temp.
ATxmega128A1U-AU	128K + 8K	2K	8K	32	1.6 - 3.6V	100A	-40°C - 85°C
ATxmega128A1U-AUR(4)	128K + 8K	2K	8K				
ATxmega64A1U-AU	64K + 4K	2K	4K				
ATxmega64A1U-AUR(4)	64K + 4K	2K	4K				
ATxmega128A1U-CU	128K + 8K	2K	8K			100C1	
ATxmega128A1U-CUR(4)	128K + 8K	2K	8K				
ATxmega64A1U-CU	64K + 4K	2K	4K				
ATxmega64A1U-CUR(4)	64K + 4K	2K	4K				
ATxmega128A1U-C7U	128K + 8K	2K	8K			100C2	
ATxmega128A1U-C7UR(4)	128K + 8K	2K	8K				
ATxmega64A1U-C7U	64K + 4K	2K	4K				
ATxmega64A1U-C7UR(4)	64K + 4K	2K	4K				
ATxmega128A1U-AN	128K + 8K	2K	8K			100A	-40°C - 105°C
ATxmega128A1U-ANR(4)	128K + 8K	2K	8K				
ATxmega64A1U-AN	64K + 4K	2K	4K				
ATxmega64A1U-ANR(4)	64K + 4K	2K	4K				

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For packaging information, see "Packaging information" on page 71.
4. Tape and Reel.

Package Type	
100A	100-lead, 14 x 14 x 1.0mm, 0.5mm lead pitch, thin profile plastic quad flat package (TQFP)
100C1	100-ball, 9 x 9 x 1.2mm body, ball pitch 0.80mm, chip ball grid array (CBGA)
100C2	100-ball, 7 x 7 x 1.0mm body, ball pitch 0.65mm, very thin fine-pitch ball grid array (VFBGA)

Typical Applications

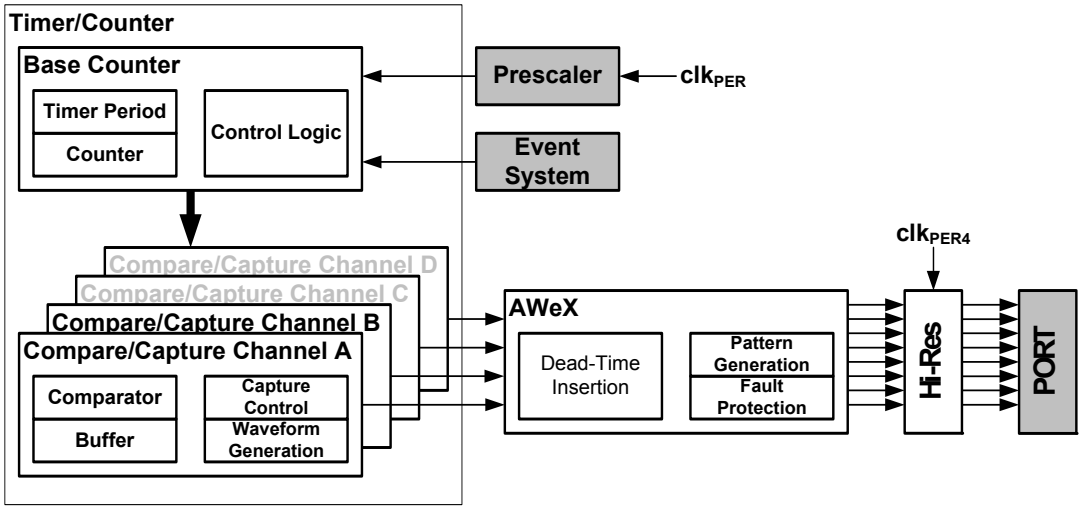
Industrial control	Climate control	Low power battery applications
Factory automation	RF and ZigBee®	Power tools
Building control	USB connectivity	HVAC
Board control	Sensor control	Utility metering
White goods	Optical	Medical applications

Some timer/counters have extensions to enable more specialized waveform and frequency generation. The advanced waveform extension (AWeX) is intended for motor control and other power control applications. It enables low- and high-side output with dead-time insertion, as well as fault protection for disabling and shutting down external drivers. It can also generate a synchronized bit pattern across the port pins.

The advanced waveform extension can be enabled to provide extra and more advanced features for the Timer/Counter. This is only available for Timer/Counter 0. See "“AWeX – Advanced Waveform Extension” on page 37 for more details.

The high-resolution (hi-res) extension can be used to increase the waveform output resolution by four or eight times by using an internal clock source running up to four times faster than the peripheral clock. See “Hi-Res – High Resolution Extension” on page 38 for more details.

Figure 16-1. Overview of a timer/counter (TC) and closely related peripherals.



PORTC, PORTD, PORTE and PORTF each has one timer/counter 0 and one timer/counter1. Notation of these timer/counters are TCC0 (timer/counter C0), TCC1, TCD0, TCD1, TCE0, TCE1, TCF0, and TCF1, respectively.

17. TC2 – Time/Counter Type 2

17.1 Features

- Eight eight-bit timer/counters
  - Four Low-byte timer/counters
  - Four High-byte timer/counters
- Up to eight compare channels in each timer/counter 2
  - Four compare channels for the low-byte timer/counter
  - Four compare channels for the high-byte timer/counter
- Waveform generation
  - Single slope pulse width modulation
- Timer underflow interrupts/events
- One compare match interrupt/event per compare channel for the low-byte timer/counter
- Can be used with the event system for count control
- Can be used to trigger DMA transactions

17.2 Overview

There are four Timer/counter 2. These are realized when a Timer/counter 0 is set in split mode. It is then a system of two eight-bit timer/counters, each with four compare channels. This results in eight configurable pulse width modulation (PWM) channels with individually controlled duty cycles, and is intended for applications that require a high number of PWM channels.

The two eight-bit timer/counters in this system are referred to as the low-byte timer/counter and high-byte timer/counter, respectively. The difference between them is that only the low-byte timer/counter can be used to generate compare match interrupts, events and DMA triggers.

The two eight-bit timer/counters have a shared clock source and separate period and compare settings. They can be clocked and timed from the peripheral clock, with optional prescaling, or from the event system. The counters are always counting down.

PORTC, PORTD, PORTE and PORTF each has one Timer/Counter 2. Notation of these are TCC2 (Time/Counter C2), TCD2, TCE2 and TCF2, respectively.

A DAC conversion is automatically started when new data to be converted are available. Events from the event system can also be used to trigger a conversion, and this enables synchronized and timed conversions between the DAC and other peripherals, such as a timer/counter. The DMA controller can be used to transfer data to the DAC.

The DAC has high drive strength, and is capable of driving both resistive and capacitive loads, aswell as loads which combine both. A low-power mode is available, which will reduce the drive strength of the output.

Internal and external voltage references can be used. The DAC output is also internally available for use as input to the analog comparator or ADC.

PORTA and PORTB each has one DAC. Notation of these peripherals are DACA and DACB, respectively.

31. AC – Analog Comparator

31.1 Features

- Four Analog Comparators
- Selectable propagation delay versus current consumption
- Selectable hysteresis
  - No
  - Small
  - Large
- Analog comparator output available on pin
- Flexible input selection
  - All pins on the port
  - Output from the DAC
  - Bandgap reference voltage
  - A 64-level programmable voltage scaler of the internal AV_{CC} voltage
- Interrupt and event generation on:
  - Rising edge
  - Falling edge
  - Toggle
- Window function interrupt and event generation on:
  - Signal above window
  - Signal inside window
  - Signal below window
- Constant current source with configurable output pin selection

31.2 Overview

The analog comparator (AC) compares the voltage levels on two inputs and gives a digital output based on this comparison. The analog comparator may be configured to generate interrupt requests and/or events upon several different combinations of input change.

Two important properties of the analog comparator's dynamic behavior are: hysteresis and propagation delay. Both of these parameters may be adjusted in order to achieve the optimal operation for each application.

The input selection includes analog port pins, several internal signals, and a 64-level programmable voltage scaler. The analog comparator output state can also be output on a pin for use by external devices.

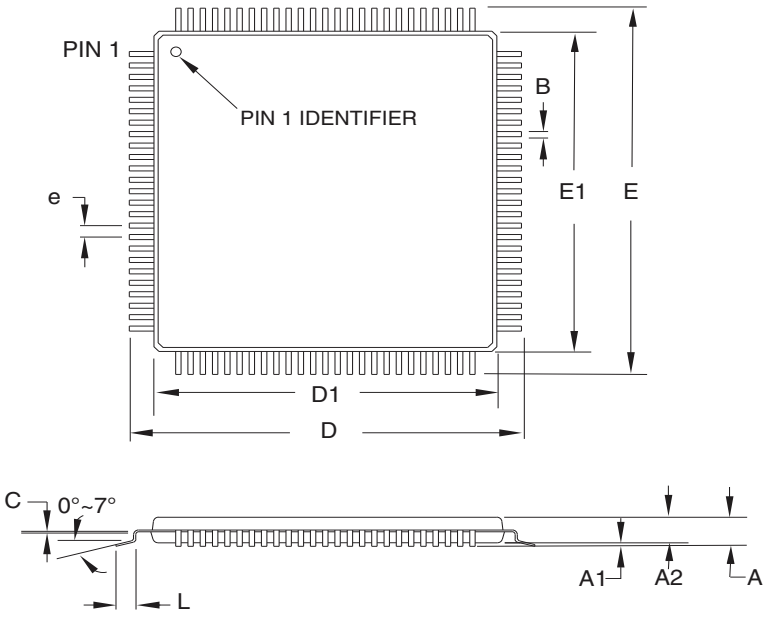
A constant current source can be enabled and output on a selectable pin. This can be used to replace, for example, external resistors used to charge capacitors in capacitive touch sensing applications.

The analog comparators are always grouped in pairs on each port. These are called analog comparator 0 (AC0) and analog comparator 1 (AC1). They have identical behavior, but separate control registers. Used as pair, they can be set in window mode to compare a signal to a voltage range instead of a voltage level.

PORTA and PORTB each has one AC pair. Notations are ACA and ACB, respectively.

36. Packaging information

36.1 100A



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	15.75	16.00	16.25	
D1	13.90	14.00	14.10	Note 2
E	15.75	16.00	16.25	
E1	13.90	14.00	14.10	Note 2
B	0.17	–	0.27	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.50 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation AED.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.08mm maximum.

2014-02-05

	TITLE	DRAWING NO.	REV.
Atmel Package Drawing Contact: packagedrawings@atmel.com	**100A**, 100-lead, 14 x 14mm Body Size, 1.0mm Body Thickness, 0.5mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	100A	E

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{CL}	Clock Low Time	V_{CC} = 1.6 - 1.8V	4.5			ns
		V_{CC} = 2.7 - 3.6V	2.4			
t_{CR}	Rise Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			1.5	ns
		V_{CC} = 2.7 - 3.6V			1.0	
t_{CF}	Fall Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			1.5	ns
		V_{CC} = 2.7 - 3.6V			1.0	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Notes: 1. System Clock Prescalers must be set so that maximum CPU clock frequency for device is not exceeded.
2. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

37.1.14.7 External 16MHz crystal oscillator and XOSC characteristics

Table 37-29. External 16MHz crystal oscillator and XOSC characteristics.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Cycle to cycle jitter	FRQRANGE=0			<10		ns
		FRQRANGE=1, 2, 3			<1		
	Frequency error	FRQRANGE=0			<0.5		%
		FRQRANGE=1			<0.05		
		FRQRANGE=2			<0.005		
		FRQRANGE=3			<0.005		
	Duty cycle	FRQRANGE=0			50		
		FRQRANGE=1			50		
		FRQRANGE=2			50		
		FRQRANGE=3			50		

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
R_Q	Negative impedance[1]	FRQRANGE=0	0.4MHz resonator, CL=100pF		13k		Ω
			1MHz crystal, CL=20pF		9k		
			2MHz crystal, CL=20pF		2.2k		
		FRQRANGE=1	1MHz crystal, CL=20pF		2.3k		
			2MHz crystal, CL=20pF		8k		
			9MHz crystal, CL=20pF		200		
		FRQRANGE=2	8MHz crystal, CL=20pF		225		
			9MHz crystal, CL=20pF		300		
			12MHz crystal, CL=10pF		175		
		FRQRANGE=3	8MHz crystal, CL=20pF		340		
			9MHz crystal, CL=20pF		400		
			12MHz crystal, CL=10pF		330		
			12MHz crystal, CL=12pF		230		
			16MHz crystal, CL=10pF		115		
	ESR	SF = safety factor				$\min(R_Q)/SF$	kΩ
	Start-up time	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF		1.0		ms
		XOSCPWR=0, FRQRANGE=1	2MHz crystal, CL=20pF		2.6		
		XOSCPWR=0, FRQRANGE=2	8MHz crystal, CL=20pF		0.8		
		XOSCPWR=0, FRQRANGE=3	12MHz crystal, CL=20pF		1.0		
		XOSCPWR=1, FRQRANGE=3	16MHz crystal, CL=20pF		1.4		
C_{XTAL1}	Parasitic capacitance XTAL1 pin				6		pF
C_{XTAL2}	Parasitic capacitance XTAL2 pin				10		
C_{LOAD}	Parasitic capacitance load				3.8		

Note: 1. Numbers for negative impedance are not tested in production but guaranteed from design and characterization.

37.1.15 SPI Characteristics

Figure 37-5. SPI timing requirements in master mode.

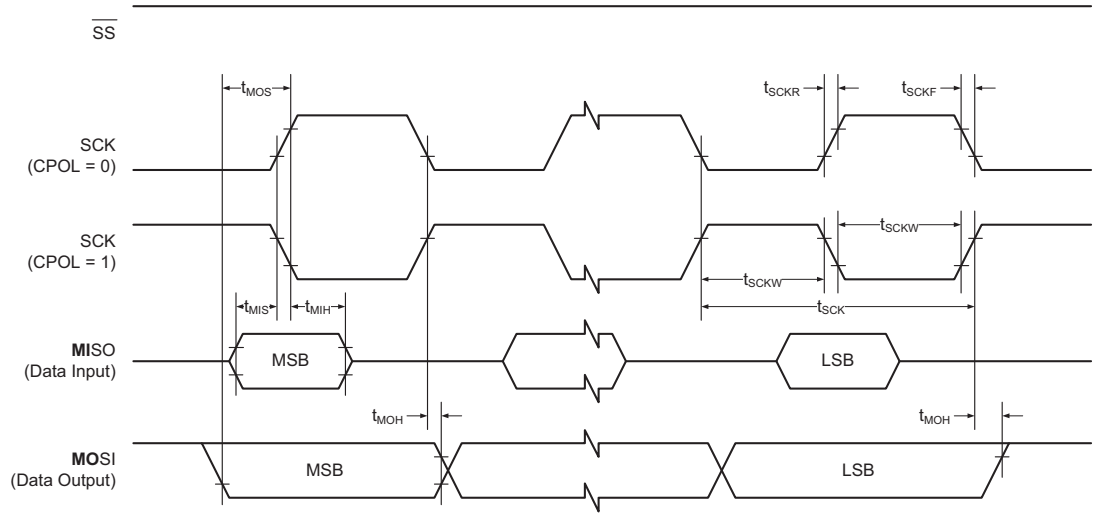
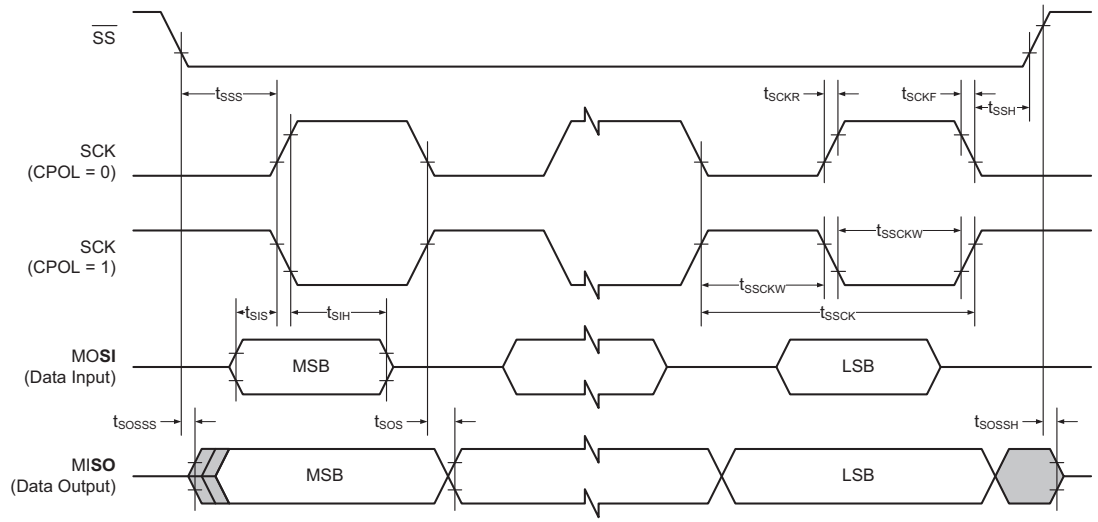


Figure 37-6. SPI timing requirements in slave mode.



Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Gain Error	1x gain, normal mode			-0.7		%
		8x gain, normal mode			-3.0		
		64x gain, normal mode			-4.8		
	Offset Error, input referred	1x gain, normal mode			0.4		mV
		8x gain, normal mode			0.4		
		64x gain, normal mode			0.4		
	Noise	1x gain, normal mode	V_{CC} = 3.6V Ext. V_{REF}		0.6		mV rms
		8x gain, normal mode			2.0		
		64x gain, normal mode			11		

Note: 1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% input voltage range.

37.2.7 DAC Characteristics

Table 37-46. Power supply, reference and output range.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
AV_{CC}	Analog supply voltage		V_{CC}- 0.3		V_{CC}+ 0.3	
AV_{REF}	External reference voltage		1.0		V_{CC}- 0.6	V
$R_{channel}$	DC output impedance				50	Ω
	Linear output voltage range		0.15		AV_{CC}-0.15	V
R_{AREF}	Reference input resistance			>10		MΩ
CAREF	Reference input capacitance	Static load		7		pF
	Minimum resistance load		1			kΩ
	Maximum capacitance load				100	pF
		1000Ω serial resistance			1	nF
	Output sink/source	Operating within accuracy specification			AV_{CC}/1000	mA
		Safe operation			10	

Table 37-47. Clock and timing.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
f_{DAC}	Conversion rate	C_{load}=100pF, maximum step size	Normal mode	0		1000	ksps
			Low power mode			500	

37.2.15 SPI Characteristics

Figure 37-12.SPI timing requirements in master mode.

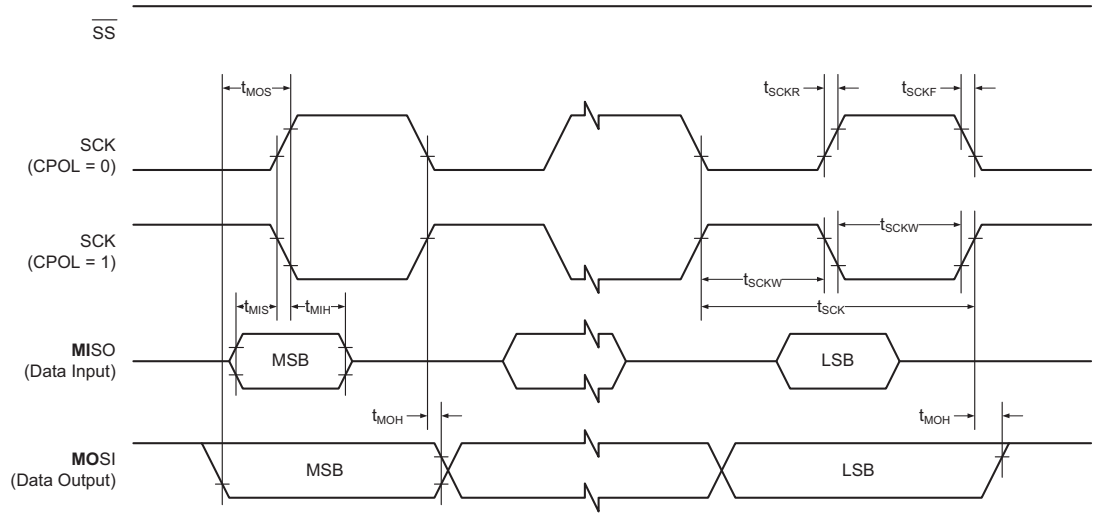


Figure 37-13.SPI timing requirements in slave mode.

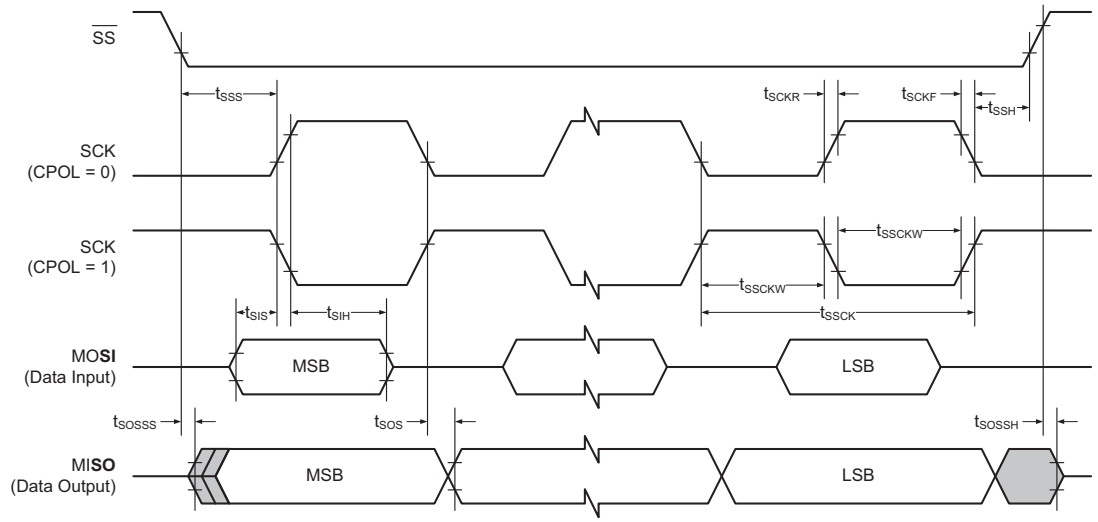


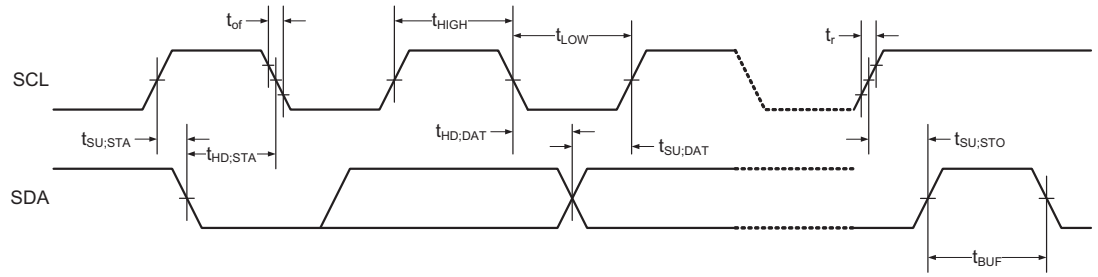
Table 37-67. EBI SDRAM characteristics and requirements.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$t_{ClkPER2}$	SDRAM clock period		$0.5*t_{ClkPER}$			ns
t_{AH}	SDRAM address hold time			$0.5*t_{ClkPER2}$		
t_{AS}	SDRAM address setup time			$0.5*t_{ClkPER2}$		
t_{CH}	SDRAM clock high-level width			$0.5*t_{ClkPER2}$		
t_{CL}	SDRAM clock low-level width			$0.5*t_{ClkPER2}$		
t_{CKH}	SDRAM CKE hold time			$0.5*t_{ClkPER2}$		
t_{CKS}	SDRAM CKE setup time			$0.5*t_{ClkPER2}$		
t_{CMH}	SDRAM CS, RAS, CAS, WE, DQM hold time			$0.5*t_{ClkPER2}$		
t_{CMS}	SDRAM CS, RAS, CAS, WE, DQM setup time			$0.5*t_{ClkPER2}$		
t_{DRH}	SDRAM data in hold after CLK high		0			
t_{AC}	SDRAM access time from CLK				t_{ClkPER}-5	
t_{DWH}	SDRAM data out hold after CLK high			$0.5*t_{ClkPER2}$		
t_{DWS}	SDRAM data out setup before CLK high			$0.5*t_{ClkPER2}$		

37.2.17 Two-Wire Interface Characteristics

Table 37-68 on page 119 describes the requirements for devices connected to the Two-Wire Interface Bus. The Atmel AVR XMEGA Two-Wire Interface meets or exceeds these requirements under the noted conditions. Timing symbols refer to Figure 37-14.

Figure 37-14.Two-Wire Interface bus timing.



38. Typical Characteristics

38.1 ATxmega64A1U

38.1.1 Current consumption

38.1.1.1 Active mode supply current

Figure 38-1. Active supply current vs. frequency.
f_{SYS} = 0 - 1MHz external clock, T = 25°C.

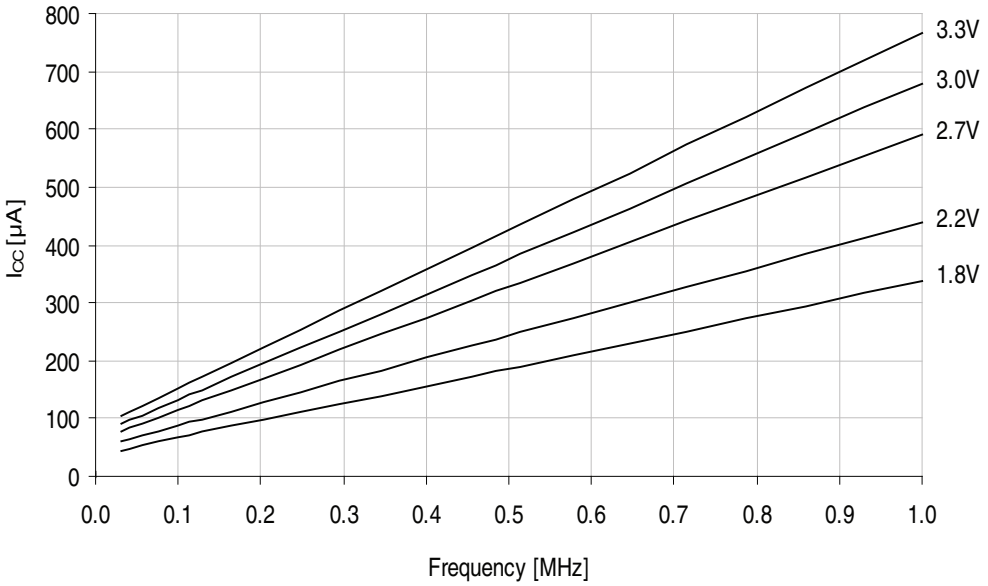


Figure 38-2. Active supply current vs. frequency.
f_{SYS} = 1 - 32MHz external clock, T = 25°C.

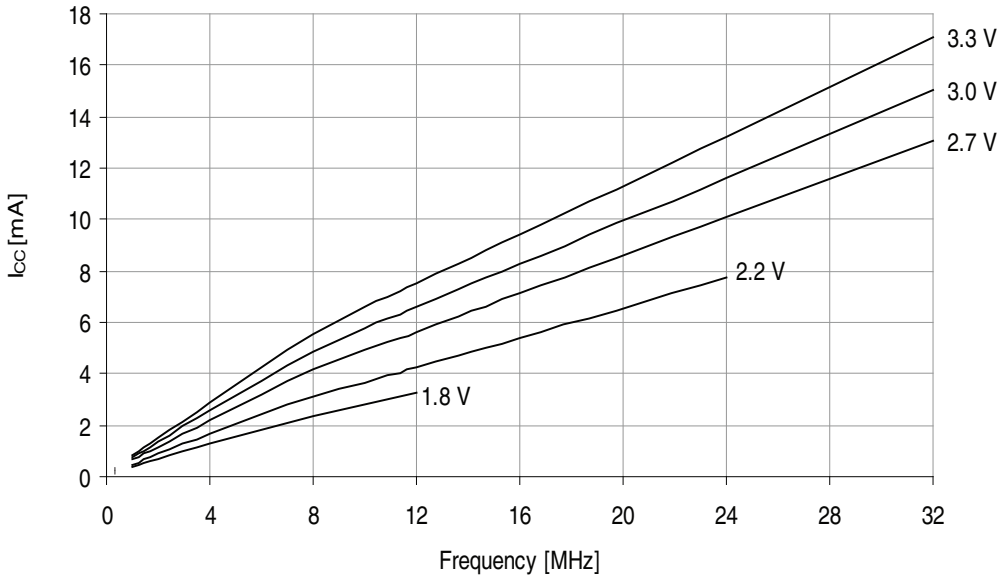


Figure 38-29.I/O pin output voltage vs. sink current.

V_{CC} = 3.3V.

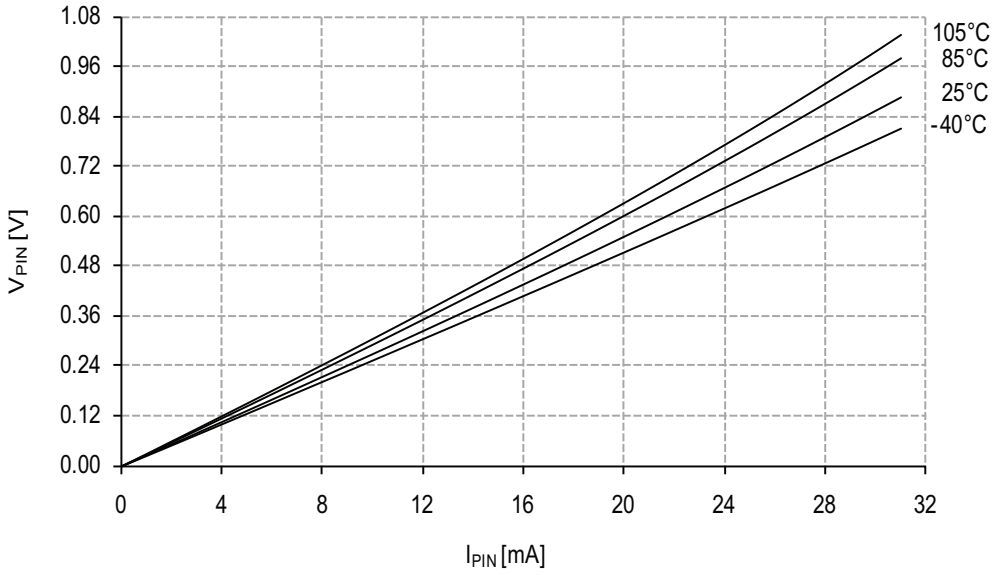


Figure 38-30.I/O pin output voltage vs. sink current.

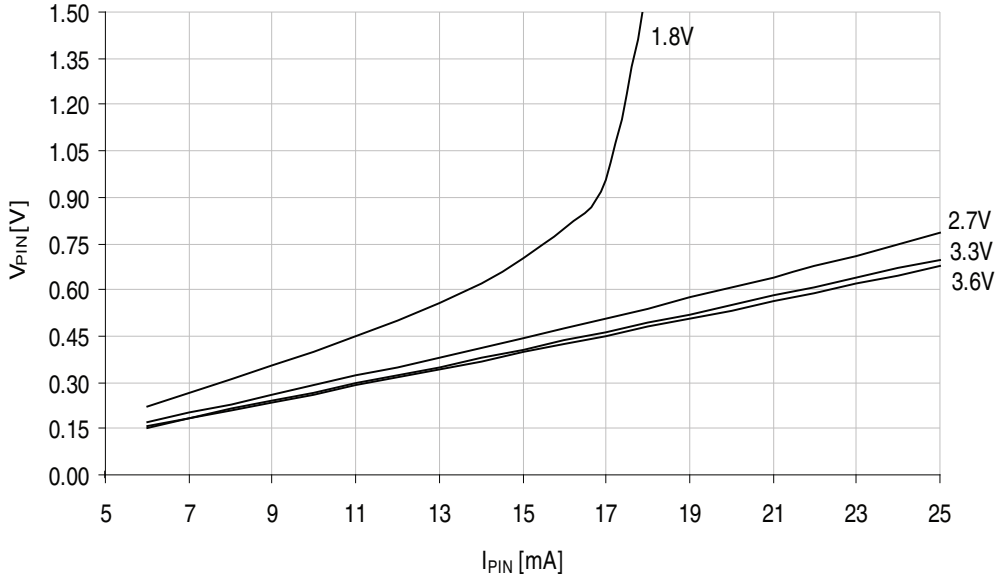


Figure 38-95.Idle mode supply current vs. V_{CC}.

f_{SYS} = 32MHz internal oscillator prescaled to 8MHz.

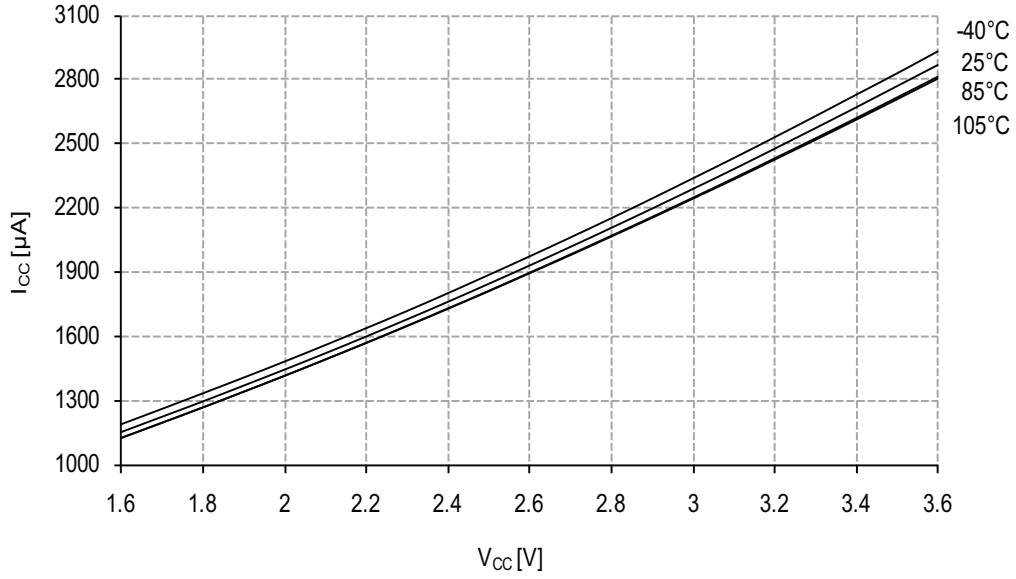


Figure 38-96.Idle mode current vs. V_{CC}.

f_{SYS} = 32MHz internal oscillator.

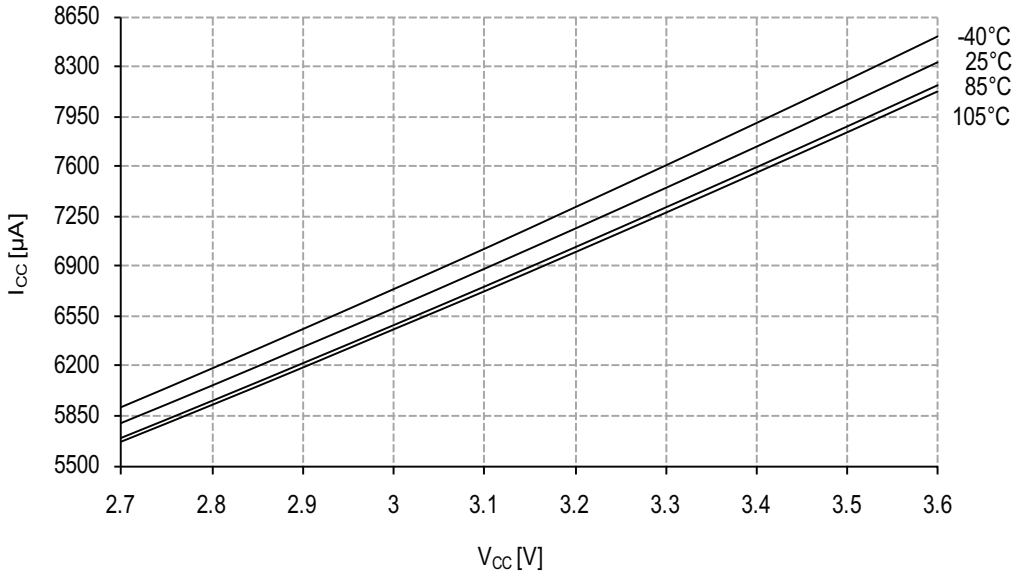
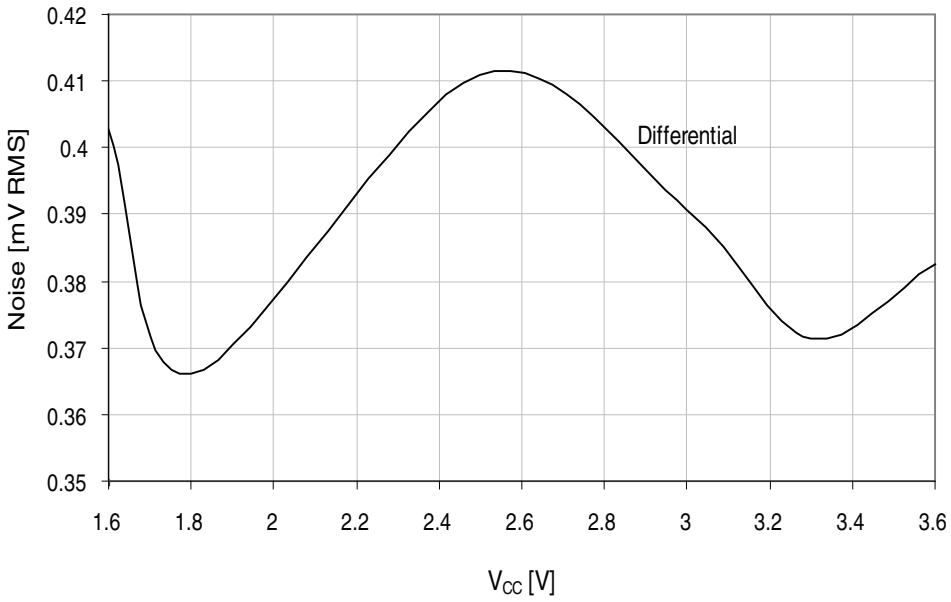


Figure 38-129.Noise vs. V_{CC}.

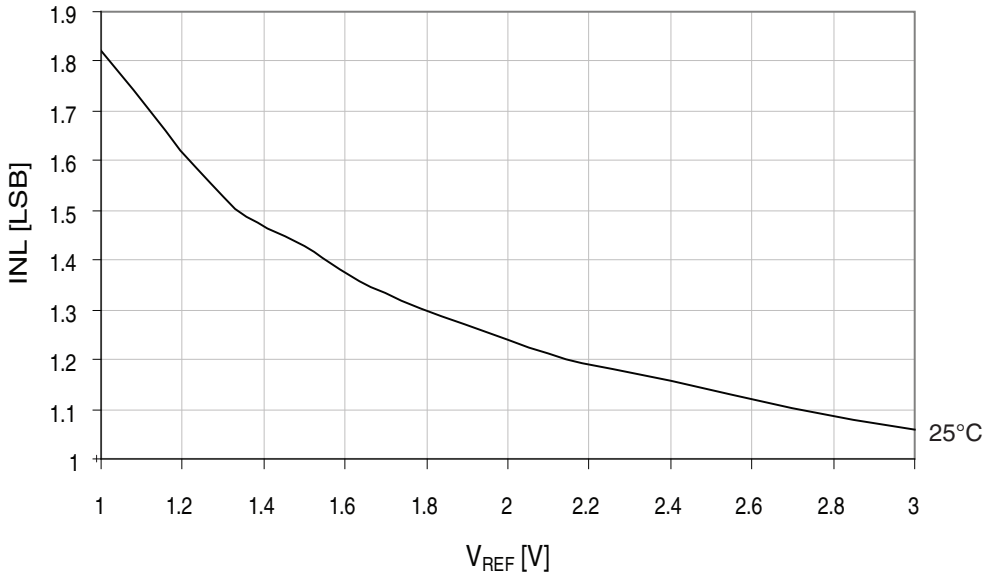
T = 25°C, V_{REF} = external 1.0V, ADC sampling speed = 500ksps.



38.2.4 DAC Characteristics

Figure 38-130.DAC INL error vs. V_{REF}.

V_{CC} = 3.6V, external reference, room temperature.



38.2.7 BOD Characteristics

Figure 38-141.BOD thresholds vs. temperature.

BOD level = 1.6V.

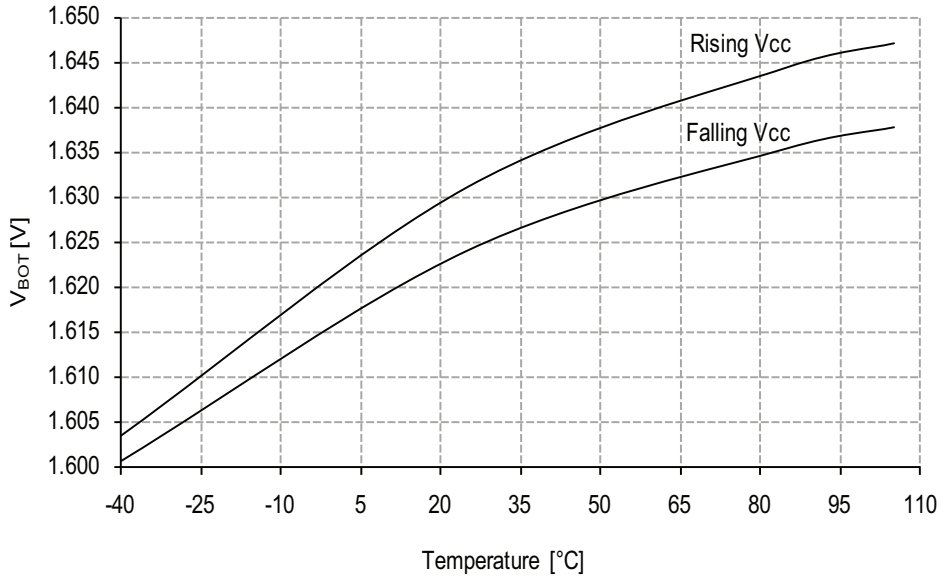
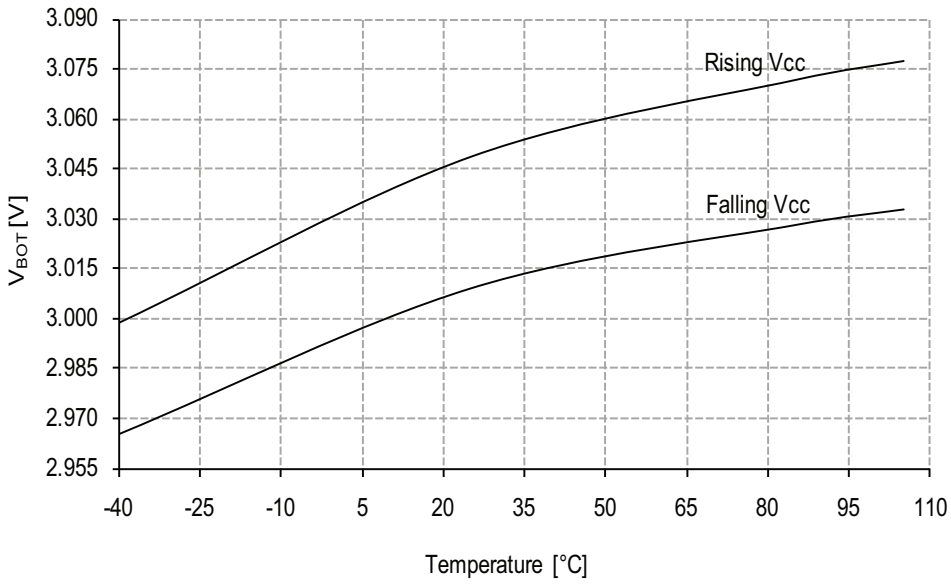


Figure 38-142.BOD thresholds vs. temperature.

BOD level = 3.0V.



38.2.9 Power-on Reset Characteristics

Figure 38-149.Power-on reset current consumption vs. V_{CC}.

BOD level = 3.0V, enabled in continuous mode.

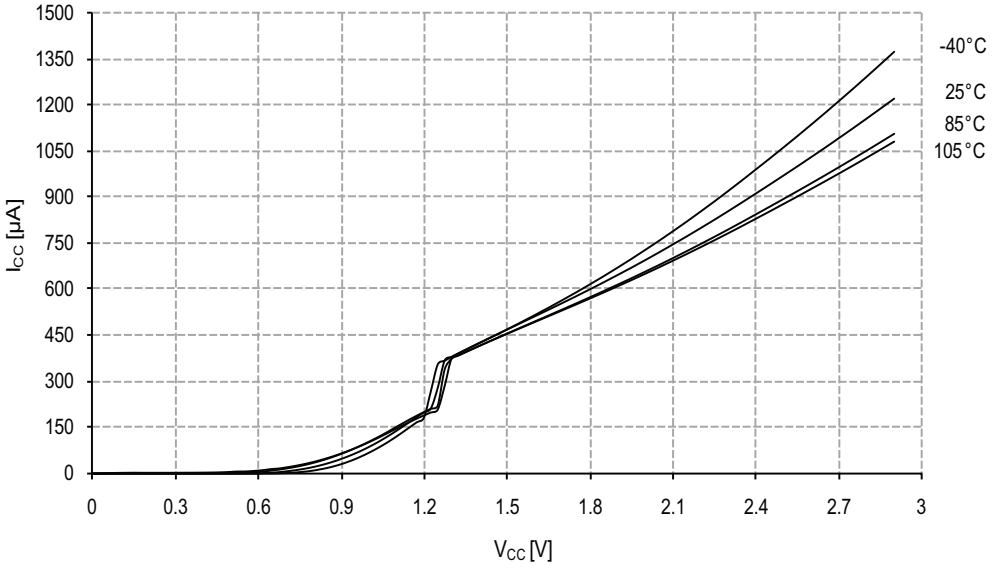
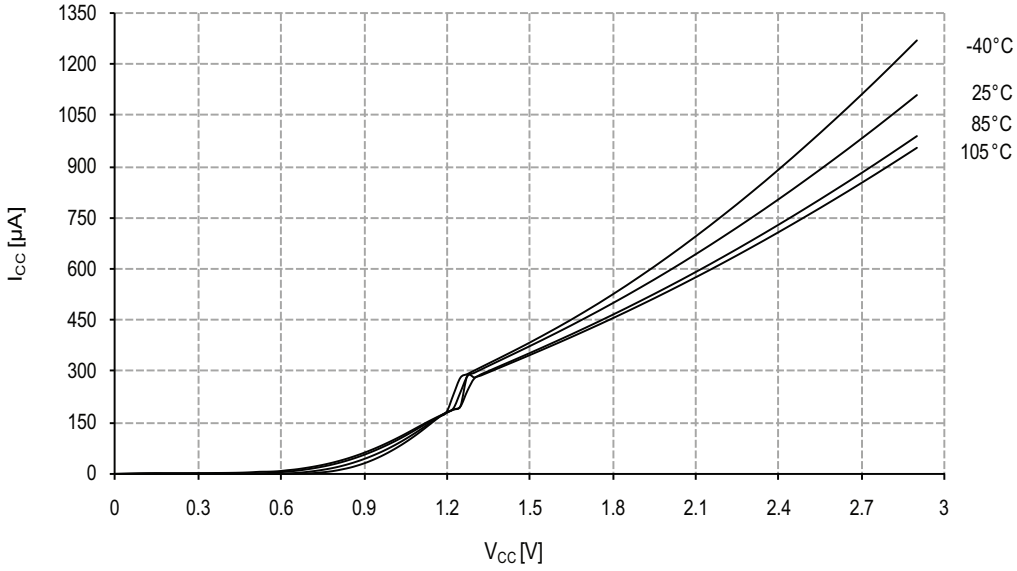


Figure 38-150.Power-on reset current consumption vs. V_{CC}.

BOD level = 3.0V, enabled in sampled mode.



38.2.10.5 32MHz internal oscillator calibrated to 48MHz

Figure 38-161. 48MHz internal oscillator frequency vs. temperature.

DFLL disabled.

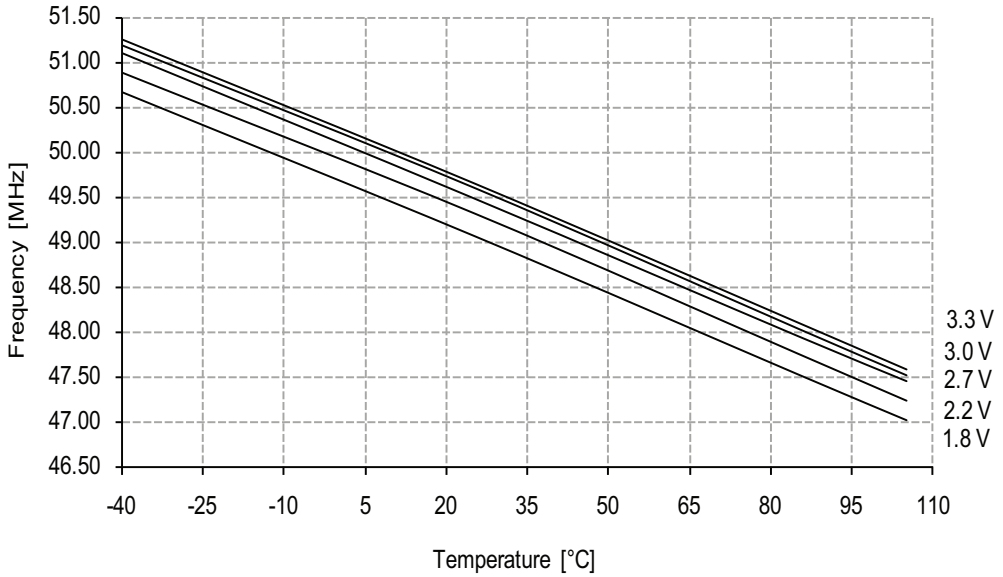
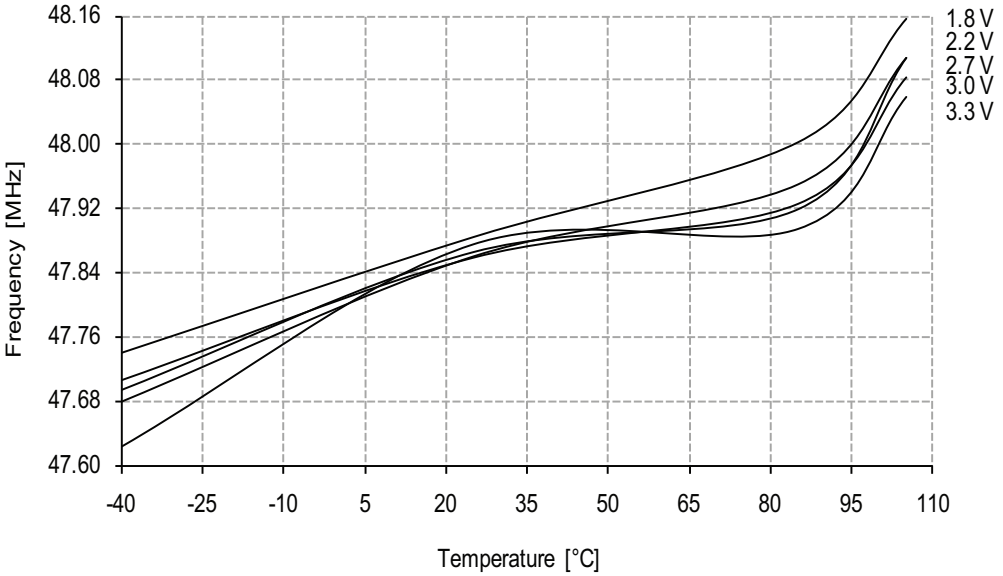


Figure 38-162. 48MHz internal oscillator frequency vs. temperature.

DFLL enabled, from the 32.768kHz internal oscillator.



7.	Added electrical characterization for “ATxmega64A1U” on page 74.
8.	Updated Table 37-29 on page 89 and Table 37-63 on page 112. Added ESR and start-up time parameters.
9.	Added typical characteristics for “ATxmega64A1U” on page 120.

40.6 8385D – 07/2012

1.	Updated Table 7-2 on page 15. Devices are respectively ATxmega64A1U and ATxmega128A1U.

40.7 8385C – 07/2012

1.	Updated Table 7-1 on page 13. Device ID for ATxmega128A1U is 4C97. Device ID for ATxmega64A1U is 4E96.
2.	Updated the package “100C2” on page 73. The ball rows are A-K (without I).
3.	Updated the whole datasheet using the Atmel new updated datasheet template that includes Atmel new logo and new registered TM.

40.8 8385B – 03/2012

1.	Added “Electrical Characteristics” on page 74.
2.	Added “Typical Characteristics” on page 120.
3.	Updated “Errata” on page 202.
4.	Used Atmel new datasheet template that includes Atmel new addresses on the last page.

40.9 8385A – 11/2011

1.	Initial revision.