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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	EBI/EMI, I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	78
Program Memory Size	128KB (64K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-CBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega128a1u-cn

Six of the 32 registers can be used as three 16-bit address register pointers for data space addressing, enabling efficient address calculations. One of these address pointers can also be used as an address pointer for lookup tables in flash program memory.

7. Memories

7.1 Features

- Flash program memory
  - One linear address space
  - In-system programmable
  - Self-programming and boot loader support
  - Application section for application code
  - Application table section for application code or data storage
  - Boot section for application code or boot loader code
  - Separate read/write protection lock bits for all sections
  - Built in fast CRC check of a selectable flash program memory section
- Data memory
  - One linear address space
  - Single-cycle access from CPU
  - SRAM
  - EEPROM
    - Byte and page accessible
    - Optional memory mapping for direct load and store
  - I/O memory
    - Configuration and status registers for all peripherals and modules
    - 16 bit-accessible general purpose register for global variables or flags
  - External memory support
    - SRAM
    - SDRAM
    - Memory mapped external hardware
  - Bus arbitration
    - Deterministic priority handling between CPU, DMA controller, and other bus masters
  - Separate buses for SRAM, EEPROM, I/O memory and external memory
    - Simultaneous bus access for CPU and DMA controller
- Production signature row memory for factory programmed data
  - ID for each microcontroller device type
  - Serial number for each device
  - Calibration bytes for factory calibrated peripherals
- User signature row
  - One flash page in size
  - Can be read and written from software
  - Content is kept after chip erase

7.2 Overview

The Atmel AVR architecture has two main memory spaces, the program memory and the data memory. Executable code can reside only in the program memory, while data can be stored in the program memory and the data memory. The data memory includes the internal SRAM, and EEPROM for nonvolatile data storage. All memory spaces are linear and require no memory bank switching. Nonvolatile memory (NVM) spaces can be locked for further write and read/write operations. This prevents unrestricted access to the application software.

A separate memory section contains the fuse bytes. These are used for configuring important system functions, and can only be written by an external programmer.

11.3.3 Power-save Mode

Power-save mode is identical to power down, with one exception. If the real-time counter (RTC) is enabled, it will keep running during sleep, and the device can also wake up from either an RTC overflow or compare match interrupt.

11.3.4 Standby Mode

Standby mode is identical to power down, with the exception that the enabled system clock sources are kept running while the CPU, peripheral, and RTC clocks are stopped. This reduces the wake-up time.

11.3.5 Extended Standby Mode

Extended standby mode is identical to power-save mode, with the exception that the enabled system clock sources are kept running while the CPU and peripheral clocks are stopped. This reduces the wake-up time.

16. TC0/1 – 16-bit Timer/Counter Type 0 and 1

16.1 Features

- Eight 16-bit timer/counters
  - Four timer/counters of type 0
  - Four timer/counters of type 1
- 32-bit timer/counter support by cascading two timer/counters
- Up to four compare or capture (CC) channels
  - Four CC channels for timer/counters of type 0
  - Two CC channels for timer/counters of type 1
- Double buffered timer period setting
- Double buffered capture or compare channels
- Waveform generation:
  - Frequency generation
  - Single-slope pulse width modulation
  - Dual-slope pulse width modulation
- Input capture:
  - Input capture with noise cancelling
  - Frequency capture
  - Pulse width capture
  - 32-bit input capture
- Timer overflow and error interrupt events
- One compare match or input capture interrupt event per CC channel
- Can be used with event system for:
  - Quadrature decoding
  - Count and direction control
  - Capture
- Can be used with DMA and trigger DMA transactions
- High-resolution extension
  - Increases frequency and waveform resolution by 4x (2-bit) or 8x (3-bit)
- Advanced waveform extension
  - Low and high-side output with programmable dead-time insertion (DTI)
  - Event controlled fault protection for safe disabling of external drivers

16.2 Overview

Atmel AVR XMEGA devices have a set of eight flexible 16-bit timer/counters (TC). Their capabilities include accurate program execution timing, frequency and waveform generation, and input capture with time and frequency measurement of digital signals. Two timer/counters can be cascaded to create a 32-bit timer/counter with optional 32-bit capture.

A timer/counter consists of a base counter and a set of compare or capture (CC) channels. The base counter can be used to count clock cycles or events. It has direction control and period setting that can be used for timing. The CC channels can be used together with the base counter to do compare match control, frequency generation, and pulse width waveform modulation, as well as various input capture operations. A timer/counter can be configured for either capture or compare functions, but cannot perform both at the same time.

A timer/counter can be clocked and timed from the peripheral clock with optional prescaling or from the event system. The event system can also be used for direction control and capture trigger or to synchronize operations.

There are two differences between timer/counter type 0 and type 1. Timer/counter 0 has four CC channels, and timer/counter 1 has two CC channels. All information related to CC channels 3 and 4 is valid only for timer/counter 0. Only Timer/Counter 0 has the split mode feature that split it into 2 8-bit Timer/Counters with four compare channels each.

19. Hi-Res – High Resolution Extension

19.1 Features

- Increases waveform generator resolution up to 8x (three bits)
- Supports frequency, single-slope PWM and dual-slope PWM generation
- Supports the AWeX when this is used for the same timer/counter

19.2 Overview

The high-resolution (hi-res) extension can be used to increase the resolution of the waveform generation output from a timer/counter by four or eight. It can be used for a timer/counter doing frequency, single-slope PWM, or dual-slope PWM generation. It can also be used with the AWeX if this is used for the same timer/counter.

The hi-res extension uses the peripheral 4x clock (Clk_{PER4}). The system clock prescalers must be configured so the peripheral 4x clock frequency is four times higher than the peripheral and CPU clock frequency when the hi-res extension is enabled.

There are four hi-res extensions that each can be enabled for each timer/counters pair on PORTC, PORTD, PORTE and PORTF. The notation of these peripherals are HIRESC, HIRESD, HIRESE and HIRESF, respectively.

26. AES and DES Crypto Engine

26.1 Features

- Data Encryption Standard (DES) CPU instruction
- Advanced Encryption Standard (AES) crypto module
- DES Instruction
  - Encryption and decryption
  - DES supported
  - Encryption/decryption in 16 CPU clock cycles per 8-byte block
- AES crypto module
  - Encryption and decryption
  - Supports 128-bit keys
  - Supports XOR data load mode to the state memory
  - Encryption/decryption in 375 clock cycles per 16-byte block

26.2 Overview

The Advanced Encryption Standard (AES) and Data Encryption Standard (DES) are two commonly used standards for cryptography. These are supported through an AES peripheral module and a DES CPU instruction, and the communication interfaces and the CPU can use these for fast, encrypted communication and secure data storage.

DES is supported by an instruction in the AVR CPU. The 8-byte key and 8-byte data blocks must be loaded into the register file, and then the DES instruction must be executed 16 times to encrypt/decrypt the data block.

The AES crypto module encrypts and decrypts 128-bit data blocks with the use of a 128-bit key. The key and data must be loaded into the key and state memory in the module before encryption/decryption is started. It takes 375 peripheral clock cycles before the encryption/decryption is done. The encrypted/encrypted data can then be read out, and an optional interrupt can be generated. The AES crypto module also has DMA support with transfer triggers when encryption/decryption is done and optional auto-start of encryption/decryption when the state memory is fully loaded.

29. ADC – 12-bit Analog to Digital Converter

29.1 Features

- Two Analog to Digital Converters
- 12-bit resolution
- Up to two million samples per second
  - Two inputs can be sampled simultaneously using ADC and 1x gain stage
  - Four inputs can be sampled within 1.5µs
  - Down to 2.5µs conversion time with 8-bit resolution
  - Down to 3.5µs conversion time with 12-bit resolution
- Differential and single-ended input
  - Up to 16 single-ended inputs
  - 16x4 differential inputs without gain
  - 8x4 differential input with gain
- Built-in differential gain stage
  - 1/2x, 1x, 2x, 4x, 8x, 16x, 32x, and 64x gain options
- Single, continuous and scan conversion options
- Four internal inputs
  - Internal temperature sensor
  - DAC output
  - AV_{CC} voltage divided by 10
  - 1.1V bandgap voltage
- Four conversion channels with individual input control and result registers
  - Enable four parallel configurations and results
- Internal and external reference options
- Compare function for accurate monitoring of user defined thresholds
- Optional event triggered conversion for accurate timing
- Optional DMA transfer of conversion results
- Optional interrupt/event on compare result

29.2 Overview

The ADC converts analog signals to digital values. There are two Analog to Digital Converters (ADCs) modules that can be operated simultaneously, individually or synchronized.

The ADC has 12-bit resolution and is capable of converting up to two million samples per second (msps). The input selection is flexible, and both single-ended and differential measurements can be done. For differential measurements, an optional gain stage is available to increase the dynamic range. In addition, several internal signal inputs are available. The ADC can provide both signed and unsigned results.

This is a pipelined ADC that consists of several consecutive stages. The pipelined design allows a high sample rate at a low system clock frequency. It also means that a new input can be sampled and a new ADC conversion started while other ADC conversions are still ongoing. This removes dependencies between sample rate and propagation delay.

The ADC has four conversion channels (0-3) with individual input selection, result registers, and conversion start control. The ADC can then keep and use four parallel configurations and results, and this will ease use for applications with high data throughput or for multiple modules using the ADC independently. It is possible to use DMA to move ADC results directly to memory or peripherals when conversions are done.

Both internal and external reference voltages can be used. An integrated temperature sensor is available for use with the ADC. The output from the DAC, $AV_{CC}/10$ and the bandgap voltage can also be measured by the ADC.

The ADC has a compare function for accurate monitoring of user defined thresholds with minimum software intervention required.

A DAC conversion is automatically started when new data to be converted are available. Events from the event system can also be used to trigger a conversion, and this enables synchronized and timed conversions between the DAC and other peripherals, such as a timer/counter. The DMA controller can be used to transfer data to the DAC.

The DAC has high drive strength, and is capable of driving both resistive and capacitive loads, aswell as loads which combine both. A low-power mode is available, which will reduce the drive strength of the output.

Internal and external voltage references can be used. The DAC output is also internally available for use as input to the analog comparator or ADC.

PORTA and PORTB each has one DAC. Notation of these peripherals are DACA and DACB, respectively.

37. Electrical Characteristics

All typical values are measured at T = 25°C unless other temperature condition is given. All minimum and maximum values are valid across operating temperature and voltage unless other conditions are given.

Note: For devices that are not available yet, preliminary values in this datasheet are based on simulations, and/or characterization of similar AVR XMEGA microcontrollers. After the device is characterized the final values will be available, hence existing values can change. Missing minimum and maximum values will be available after the device is characterized.

37.1 ATxmega64A1U

37.1.1 Absolute Maximum Ratings

Stresses beyond those listed in Table 37-1 on page 74 under may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 37-1. Absolute maximum ratings.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		-0.3		4	V
I_{VCC}	Current into a V_{CC} pin				200	mA
I_{GND}	Current out of a Gnd pin				200	
V_{PIN}	Pin voltage with respect to Gnd and V_{CC}		-0.5		V_{CC}+0.5	V
I_{PIN}	I/O pin sink/source current		-25		25	mA
T_A	Storage temperature		-65		150	°C
T_j	Junction temperature				150	

37.1.2 General Operating Ratings

The device must operate within the ratings listed in Table 37-2 in order for all other electrical characteristics and typical characteristics of the device to be valid.

Table 37-2. General operating conditions.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		1.60		3.6	V
AV_{CC}	Analog supply voltage		1.60		3.6	
T_A	Temperature range		-40		85	°C
T_j	Junction temperature		-40		105	

37.2.3 Current consumption

Table 37-38. Current consumption for Active mode and sleep modes.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{CC}	Active power consumption(1)	32kHz, Ext. Clk	V_{CC} = 1.8V		50		µA
			V_{CC} = 3.0V		95		
		1MHz, Ext. Clk	V_{CC} = 1.8V		350		
			V_{CC} = 3.0V		700		
		2MHz, Ext. Clk	V_{CC} = 1.8V		650	700	
			V_{CC} = 3.0V		1.2	1.4	mA
		32MHz, Ext. Clk			15	20	
	Idle power consumption(1)	32kHz, Ext. Clk	V_{CC} = 1.8V		3.5		µA
			V_{CC} = 3.0V		6.4		
		1MHz, Ext. Clk	V_{CC} = 1.8V		109		
			V_{CC} = 3.0V		200		
		2MHz, Ext. Clk	V_{CC} = 1.8V		290	380	
			V_{CC} = 3.0V		476	650	
		32MHz, Ext. Clk			6.6	9.2	mA
	Power-down power consumption	T = 25°C	V_{CC} = 1.8V		0.1	1.0	µA
		T = 25°C	V_{CC} = 3.0V		0.1	1.0	
		T = 85°C			1.7	5.0	
		T = 105°C			6.0	10	
		WDT and sampled BOD enabled, T = 25°C	V_{CC} = 3.0V		1.3	3.0	
		WDT and sampled BOD enabled, T = 85°C			3.1	10	
		WDT and sampled BOD enabled, T = 105°C			7.0	12	
	Power-save power consumption(2)	RTC on ULP clock, WDT and sampled BOD enabled, T = 25°C	V_{CC} = 1.8V		1.2		
			V_{CC} = 3.0V		1.3		
		RTC on 1.024kHz low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.7	2.0	
			V_{CC} = 3.0V		0.8	2.0	
		RTC from low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.9	3.0	
			V_{CC} = 3.0V		1.0	3.0	
	Reset power consumption	Current through $\overline{\text{RESET}}$ pin subtracted	V_{CC} = 3.0V		914		

Notes: 1. All Power Reduction Registers set.
2. Maximum limits are based on characterization, and not tested in production.

Table 37-44. Accuracy characteristics.

Symbol	Parameter	Condition[2]		Min.	Typ.	Max.	Units
RES	Resolution	Programmable to 12-bit		11	11.5	12	Bits
INL[1]	Integral non-linearity	500ksps, differential mode	V_{CC}-1.0V < V_{REF}< V_{CC}-0.6V		±1.2	±2	lsb
			All V_{REF}		±1.5	±3	
		2000ksps, differential mode	V_{CC}-1.0V < V_{REF}< V_{CC}-0.6V		±1.0	±2	
			All V_{REF}		±1.5	±3	
		single ended mode			±1.5	±4	
DNL[1]	Differential non-linearity	guaranteed monotonic			<±0.5	<±1	
	Offset Error				-1		mV
		Temperature drift			<0.01		mV/K
		Operating voltage drift			<0.6		mV/V
	Gain Error	Differential mode	External reference		-1		mV
			AV_{CC}/1.6		10		
			AV_{CC}/2.0		8		
			Bandgap		±5		
		Temperature drift			<0.02		mV/K
		Operating voltage drift			<0.5		mV/V
	Noise	Differential mode, shorted input 2msps, V_{CC} = 3.6V, Clk_{PER} = 16MHz			0.4		mV rms

Notes: 1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% input voltage range.
2. Unless otherwise noted all linearity, offset and gain error numbers are valid under the condition that external V_{REF} is used.

Table 37-45. Gain stage characteristics.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
R_{in}	Input resistance	Switched in normal mode			4.0		kΩ
C_{sample}	Input capacitance	Switched in normal mode			4.4		pF
	Signal range	Gain stage output		0		V_{CC}- 0.6	V
	Propagation delay	ADC conversion rate			1		Clk_{ADC} cycles
	Sample rate	Same as ADC		100		1000	kHz
INL[1]	Integral Non-Linearity	500ksps	All gain settings		±1.5	±3	lsb

37.2.14.3 Calibrated and tunable 32MHz internal oscillator characteristics

Table 37-58. 32MHz internal oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Tunable frequency range	DFLL can tune to this frequency over voltage and temperature	30		35	MHz
	Factory calibrated frequency			32		
	Factory calibration accuracy	T = 85°C, V_{CC}= 3.0V	-1.5		1.5	%
	DFLL calibration step size			0.24		

37.2.14.4 32kHz Internal ULP Oscillator characteristics

Table 37-59. 32kHz internal ULP oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Output frequency			32		kHz
	Accuracy		-30		30	%

37.2.14.5 Internal Phase Locked Loop (PLL) characteristics

Table 37-60. Internal PLL characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{IN}	Input frequency	Output frequency must be within f_{OUT}	0.4		64	MHz
f_{OUT}	Output frequency[1]	V_{CC}= 1.6V	20		32	
		V_{CC}= 2.7V	20		96	
		V_{CC}= 3.6V	20		128	
	Duty cycle			50		%
	Start-up lock time	f_{OUT} = 48MHz		18		µs
	Re-lock time	$f_{OUT-init}$ = 10MHz, $f_{OUT-end}$ = 64MHz		17		

Note: 1. The maximum output frequency vs. supply voltage is linear between 1.8V and 2.7V, and can never be higher than four times the maximum CPU frequency.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
R_Q	Negative impedance[1]	FRQRANGE=0	0.4MHz resonator, CL=100pF		13k		Ω
			1MHz crystal, CL=20pF		9k		
			2MHz crystal, CL=20pF		2.2k		
		FRQRANGE=1	1MHz crystal, CL=20pF		2.3k		
			2MHz crystal, CL=20pF		8k		
			9MHz crystal, CL=20pF		200		
		FRQRANGE=2	8MHz crystal, CL=20pF		225		
			9MHz crystal, CL=20pF		300		
			12MHz crystal, CL=10pF		175		
		FRQRANGE=3	8MHz crystal, CL=20pF		340		
			9MHz crystal, CL=20pF		400		
			12MHz crystal, CL=10pF		330		
			12MHz crystal, CL=12pF		230		
			16MHz crystal, CL=10pF		115		
	ESR	SF = safety factor				$\min(R_Q)/SF$	kΩ
	Start-up time	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF		1.0		ms
		XOSCPWR=0, FRQRANGE=1	2MHz crystal, CL=20pF		2.6		
		XOSCPWR=0, FRQRANGE=2	8MHz crystal, CL=20pF		0.8		
		XOSCPWR=0, FRQRANGE=3	12MHz crystal, CL=20pF		1.0		
		XOSCPWR=1, FRQRANGE=3	16MHz crystal, CL=20pF		1.4		
C_{XTAL1}	Parasitic capacitance XTAL1 pin				6		pF
C_{XTAL2}	Parasitic capacitance XTAL2 pin				10		
C_{LOAD}	Parasitic capacitance load				3.8		

Note: 1. Numbers for negative impedance are not tested in production but guaranteed from design and characterization.

38.1.2.2 Output Voltage vs. Sink/Source Current

Figure 38-23.I/O pin output voltage vs. source current.

V_{CC} = 1.8V.

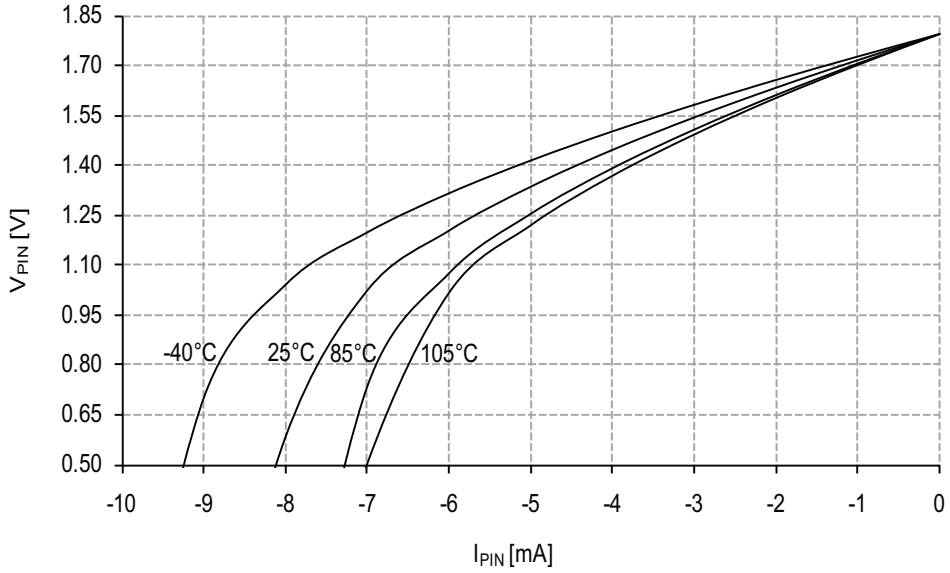
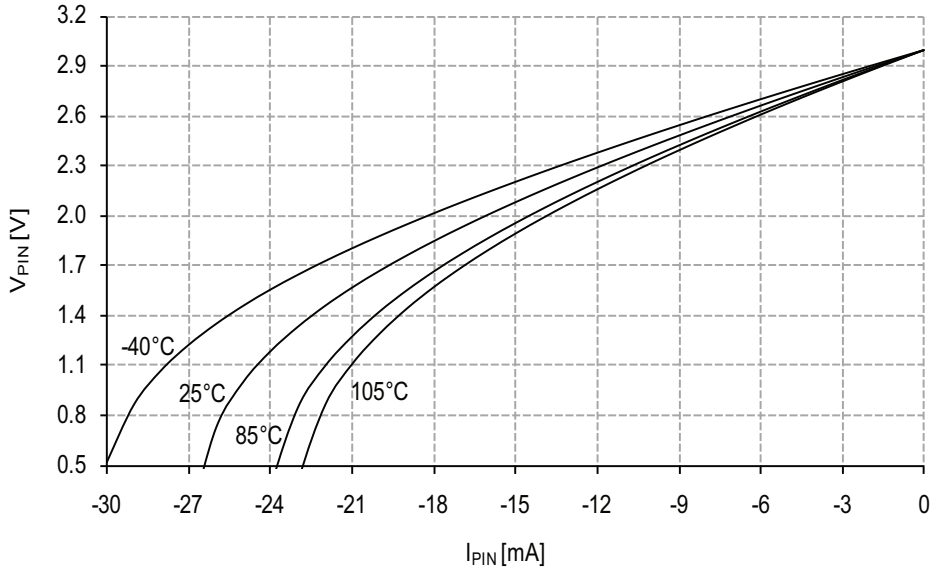


Figure 38-24.I/O pin output voltage vs. source current.

V_{CC} = 3.0V.



38.1.8 External Reset Characteristics

Figure 38-61.Minimum Reset pin pulse width vs. V_{CC}.

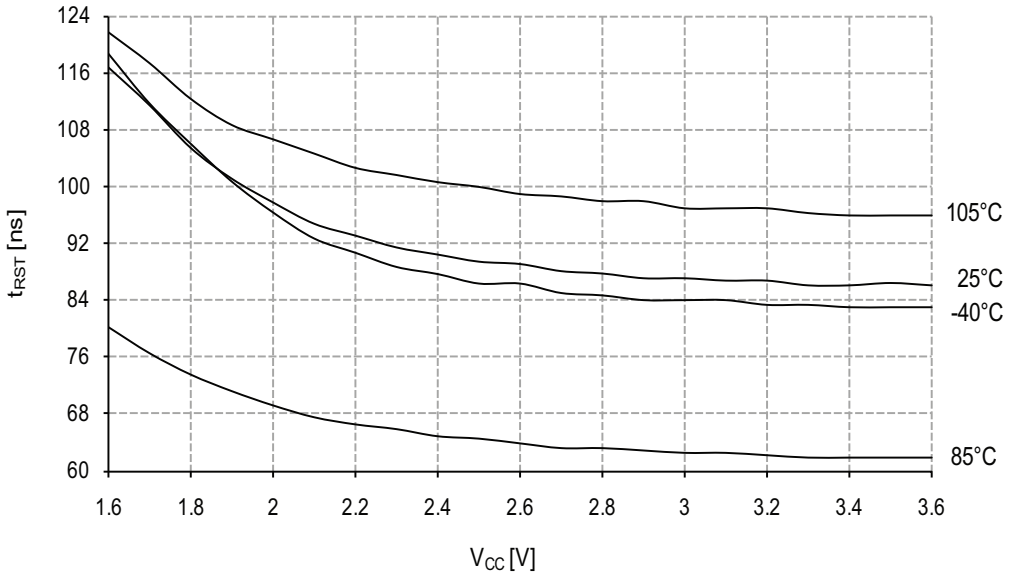


Figure 38-62.Reset pin pull-up resistor current vs. reset pin voltage.
V_{CC} = 1.8V.

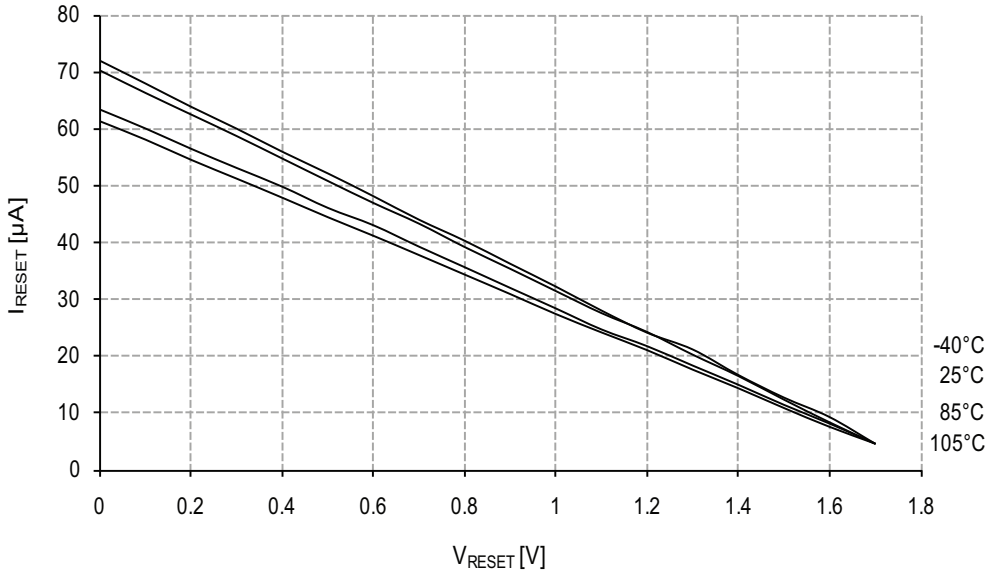


Figure 38-65.Reset pin input threshold voltage vs. V_{CC}.

V_{IH} - Reset pin read as "1".

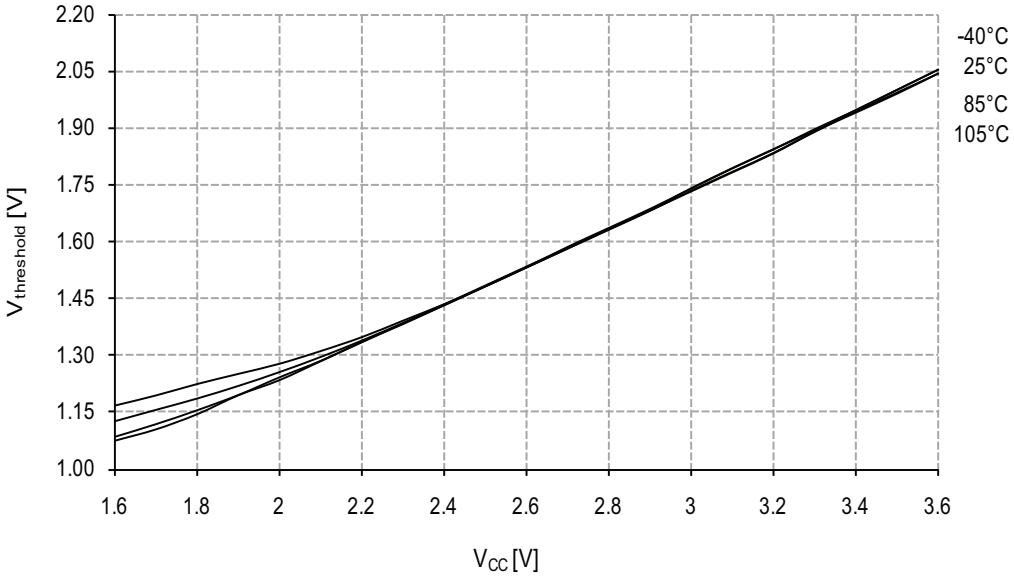


Figure 38-66.Reset pin input threshold voltage vs. V_{CC}.

V_{IL} - Reset pin read as "0".

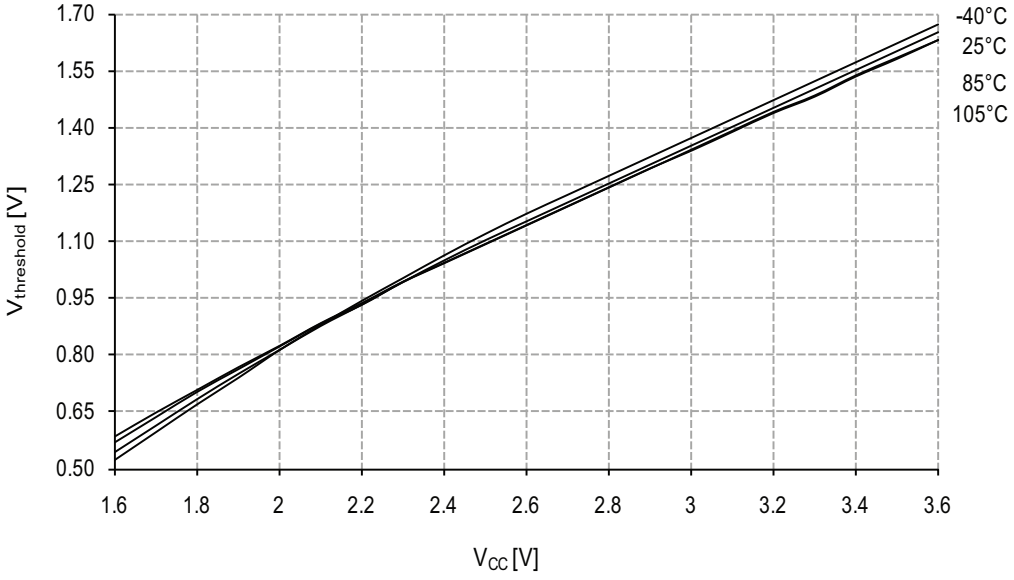


Figure 38-107.I/O pin output voltage vs. source current.

V_{CC} = 3.3V.

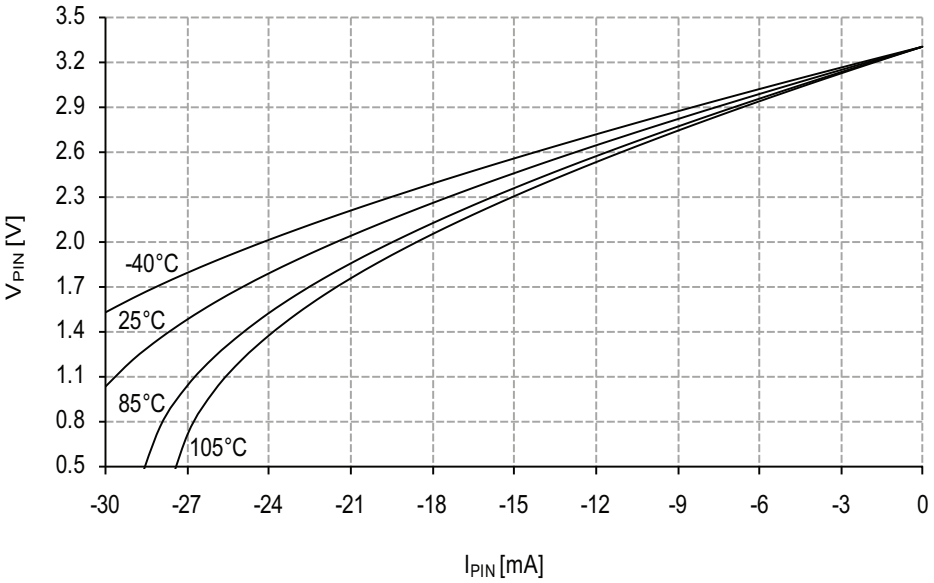
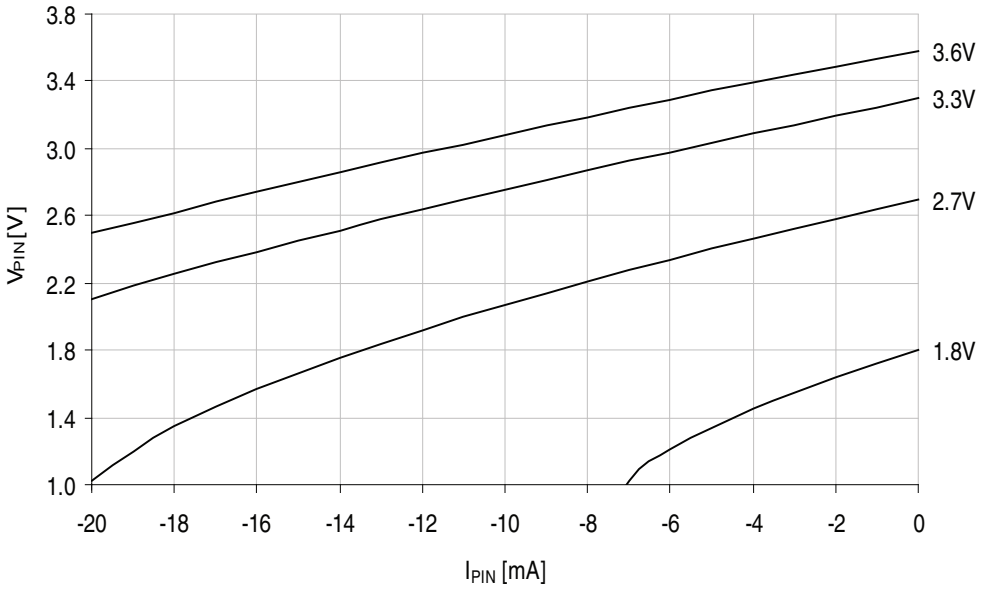


Figure 38-108.I/O pin output voltage vs. source current.



Problem fix/Workaround

Use the ADC in single ended signed mode.

15. **ADC has increased linearity error when using the gain stage above 500ksps**

The INL error for gain stage is increased to above 20LSB for sampling speed exceeding 500 ksps.

Problem fix/Workaround

None.

16. **DAC Offset calibration range too small when using AVCC as reference**

If using AVCC as reference, the DAC offset calibration will not totally remove the offset error. Offset could be up to 100LSB after calibration.

Problem fix/Workaround

Offset adjustment must be partly handled in software.

17. **DAC clock noise**

The system clock is visible as clock noise on the output of the DAC. Peak to peak noise is in the range 0.7mV - 1.6mV at 2MHz and 0.05mV to 0.1mV at 32MHz. If external clock is used as system clock, the noise is up to three times higher.

Problem fix/Workaround

Add external low-pass filter to remove the noise.

18. **Internal 1V reference has noise at low temperature**

The internal 1.0V reference for the ADC and DAC has increased noise at low temperatures. The noise can result in INL numbers up to +/- 20 LSB at temperatures below 0C.

Problem fix/Workaround

For the ADC, use oversampling to reduce noise. For the DAC use external filter to reduce the noise.

39.1.2 Rev. A – K

Not sampled.

39.2 ATxmega128A1U

39.2.1 Rev. L

- Register ANAINIT in MCUR will always read as zero
- Enabling DFLL with illegal reference oscillator will lock the DFLL
- XOSCPWR configuration is non-functional
- Configuration of PGM and CWCM is not as described in XMEGA AU Manual
- AWEX PWM output after fault restarted with wrong values
- RTC Counter value not correctly read after sleep
- RTC clock output option is non-functional
- USB, when receiving 1023 byte length isochronous frame, it will corrupt 1024th SRAM location
- USB endpoint table is 16-byte alignment
- USB Auto ZLP feature is non-functional
- Disabling the USART transmitter does not automatically set the TxD pin direction to input
- TWI, SDAHOLD configuration in the TWI CTRL register is one bit
- ADC has increased INL error in when used in SE unsigned mode at low temperatures
- ADC is non-functional in SE unsigned mode with VREF below 1.8V
- ADC has increased linearity error when using the gain stage above 500ksps
- DAC Offset calibration range too small when using AVCC as reference
- DAC clock noise
- Internal 1V reference has noise at low temperature

1 Register ANAINIT in MCUR will always read as zero

The ANAINIT register in the MCUR module will always be read as zero even if written to a value. The actual content of the register is correct.

Problem fix/Workaround

Do not use software that reads these registers to get the Analog Initialization configuration.

2. Enabling DFLL with illegal reference oscillator will lock the clock system

If external crystal is selected as reference for DFLL, but no crystal is connected and DFLL is enabled, the DFLL will be locked until reset is issued.

Problem fix/Workaround

Do not enable DFLL before reference clock is present, enabled and ready.

3. XOSCPWR configuration is non-functional

The Crystal oscillator drive (XOSCPWR) option in the XOSC Control register is non-functional.

Problem fix/Workaround

None.

4. Configuration of PGM and CWCM is not as described in XMEGA AU Manual

Configuration of common waveform channel mode (CWCM) and pattern generation mode (PGM), is not as described in the XMEGA AU manual.

15. **ADC has increased linearity error when using the gain stage above 500ksps**

The INL error for gain stage is increased to above 20LSB for sampling speed exceeding 500 ksps.

Problem fix/Workaround

None.

16. **DAC Offset calibration range too small when using AVCC as reference**

If using AVCC as reference, the DAC offset calibration will not totally remove the offset error. Offset could be up to 100LSB after calibration.

Problem fix/Workaround

Offset adjustment must be partly handled in software.

17. **DAC clock noise**

The system clock is visible as clock noise on the output of the DAC. Peak to peak noise is in the range 0.7mV - 1.6mV at 2MHz and 0.05mV to 0.1mV at 32MHz. If external clock is used as system clock, the noise is up to three times higher.

Problem fix/Workaround

Add external low-pass filter to remove the noise.

18. **Internal 1V reference has noise at low temperature**

The internal 1.0V reference for the ADC and DAC has increased noise at low temperatures. The noise can result in INL numbers up to +/- 20 LSB at temperatures below 0C.

Problem fix/Workaround

For the ADC, use oversampling to reduce noise. For the DAC use external filter to reduce the noise.

39.2.2 Rev. A – K

Not sampled.

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