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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

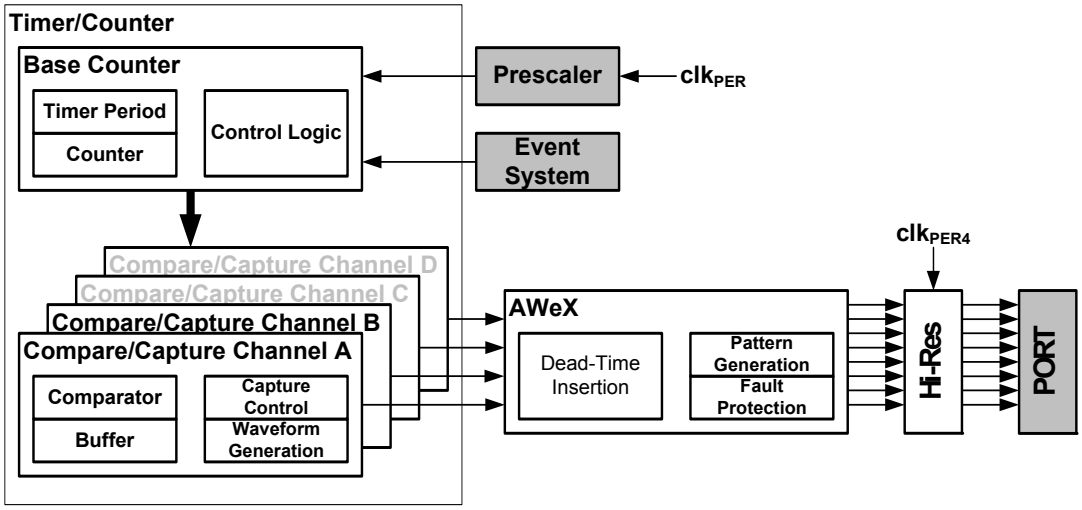
Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	EBI/EMI, I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	78
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega64a1u-an

Some timer/counters have extensions to enable more specialized waveform and frequency generation. The advanced waveform extension (AWeX) is intended for motor control and other power control applications. It enables low- and high-side output with dead-time insertion, as well as fault protection for disabling and shutting down external drivers. It can also generate a synchronized bit pattern across the port pins.

The advanced waveform extension can be enabled to provide extra and more advanced features for the Timer/Counter. This is only available for Timer/Counter 0. See "“AWeX – Advanced Waveform Extension” on page 37 for more details.

The high-resolution (hi-res) extension can be used to increase the waveform output resolution by four or eight times by using an internal clock source running up to four times faster than the peripheral clock. See “Hi-Res – High Resolution Extension” on page 38 for more details.

Figure 16-1. Overview of a timer/counter (TC) and closely related peripherals.



PORTC, PORTD, PORTE and PORTF each has one timer/counter 0 and one timer/counter1. Notation of these timer/counters are TCC0 (timer/counter C0), TCC1, TCD0, TCD1, TCE0, TCE1, TCF0, and TCF1, respectively.

19. Hi-Res – High Resolution Extension

19.1 Features

- Increases waveform generator resolution up to 8x (three bits)
- Supports frequency, single-slope PWM and dual-slope PWM generation
- Supports the AWeX when this is used for the same timer/counter

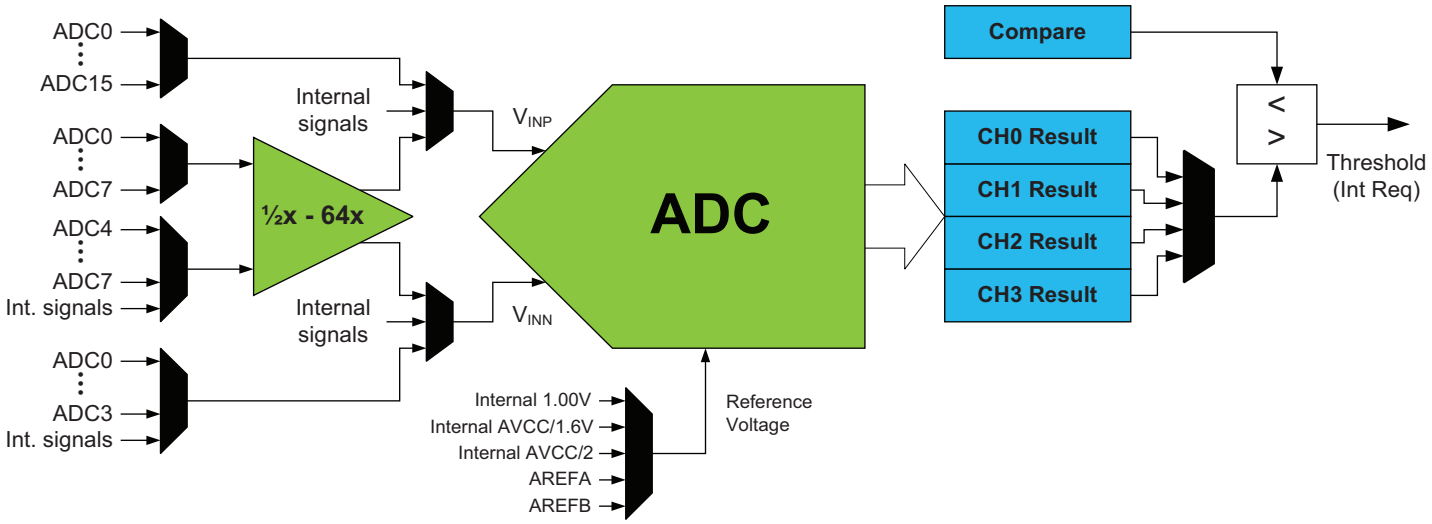
19.2 Overview

The high-resolution (hi-res) extension can be used to increase the resolution of the waveform generation output from a timer/counter by four or eight. It can be used for a timer/counter doing frequency, single-slope PWM, or dual-slope PWM generation. It can also be used with the AWeX if this is used for the same timer/counter.

The hi-res extension uses the peripheral 4x clock (Clk_{PER4}). The system clock prescalers must be configured so the peripheral 4x clock frequency is four times higher than the peripheral and CPU clock frequency when the hi-res extension is enabled.

There are four hi-res extensions that each can be enabled for each timer/counters pair on PORTC, PORTD, PORTE and PORTF. The notation of these peripherals are HIRESC, HIRESD, HIRESE and HIRESF, respectively.

Figure 29-1. ADC overview.



Two inputs can be sampled simultaneously as both the ADC and the gain stage include sample and hold circuits, and the gain stage has 1x gain setting.

Four inputs can be sampled within 1.5µs without any intervention by the application.

The ADC may be configured for 8- or 12-bit result, reducing the minimum conversion time (propagation delay) from 3.5µs for 12-bit to 2.5µs for 8-bit result.

ADC conversion results are provided left- or right adjusted with optional ‘1’ or ‘0’ padding. This eases calculation when the result is represented as a signed integer (signed 16-bit number).

PORTA and PORTB each has one ADC. Notation of these peripherals are ADCA and ADCB, respectively.

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ICALL		Indirect Call to (Z)	PC(15:0) ← Z, PC(21:16) ← 0	None	2 / 3 (1)
EICALL		Extended Indirect Call to (Z)	PC(15:0) ← Z, PC(21:16) ← EIND	None	3 (1)
CALL	k	call Subroutine	PC ← k	None	3 / 4 (1)
RET		Subroutine Return	PC ← STACK	None	4 / 5 (1)
RETI		Interrupt Return	PC ← STACK	I	4 / 5 (1)
CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) PC ← PC + 2 or 3	None	1 / 2 / 3
CP	Rd,Rr	Compare	Rd - Rr	Z,C,N,V,S,H	1
CPC	Rd,Rr	Compare with Carry	Rd - Rr - C	Z,C,N,V,S,H	1
CPI	Rd,K	Compare with Immediate	Rd - K	Z,C,N,V,S,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b) = 0) PC ← PC + 2 or 3	None	1 / 2 / 3
SBRS	Rr, b	Skip if Bit in Register Set	if (Rr(b) = 1) PC ← PC + 2 or 3	None	1 / 2 / 3
SBIC	A, b	Skip if Bit in I/O Register Cleared	if (I/O(A,b) = 0) PC ← PC + 2 or 3	None	2 / 3 / 4
SBIS	A, b	Skip if Bit in I/O Register Set	If (I/O(A,b) =1) PC ← PC + 2 or 3	None	2 / 3 / 4
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then PC ← PC + k + 1	None	1 / 2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC ← PC + k + 1	None	1 / 2
BREQ	k	Branch if Equal	if (Z = 1) then PC ← PC + k + 1	None	1 / 2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC ← PC + k + 1	None	1 / 2
BRCS	k	Branch if Carry Set	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRLO	k	Branch if Lower	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRMI	k	Branch if Minus	if (N = 1) then PC ← PC + k + 1	None	1 / 2
BRPL	k	Branch if Plus	if (N = 0) then PC ← PC + k + 1	None	1 / 2
BRGE	k	Branch if Greater or Equal, Signed	if (N ⊕ V= 0) then PC ← PC + k + 1	None	1 / 2
BRLT	k	Branch if Less Than, Signed	if (N ⊕ V= 1) then PC ← PC + k + 1	None	1 / 2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then PC ← PC + k + 1	None	1 / 2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC ← PC + k + 1	None	1 / 2
BRTS	k	Branch if T Flag Set	if (T = 1) then PC ← PC + k + 1	None	1 / 2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC ← PC + k + 1	None	1 / 2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC ← PC + k + 1	None	1 / 2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC ← PC + k + 1	None	1 / 2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC ← PC + k + 1	None	1 / 2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC ← PC + k + 1	None	1 / 2
Data transfer instructions					
MOV	Rd, Rr	Copy Register	Rd ← Rr	None	1
MOVW	Rd, Rr	Copy Register Pair	Rd+1:Rd ← Rr+1:Rr	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1

37.1.6 ADC characteristics

Table 37-8. Power supply, reference and input range.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
AV_{CC}	Analog supply voltage		V_{CC}- 0.3		V_{CC}+ 0.3	V
V_{REF}	Reference voltage		1.0		AV_{CC}- 0.6	
R_{in}	Input resistance	Switched		5.0		kΩ
C_{in}	Input capacitance	Switched		5.0		pF
R_{AREF}	Reference input resistance	(leakage only)		>10		MΩ
C_{AREF}	Reference input capacitance	Static load		7		pF
V_{IN}	Input range		-0.1		AV_{CC}+0.1	V
	Conversion range	Differential mode, Vinp - Vinn	$-V_{REF}$		V_{REF}	
V_{IN}	Conversion range	Single ended unsigned mode, Vinp	-ΔV		V_{REF}-ΔV	
ΔV	Fixed offset voltage			190		lsb

Table 37-9. Clock and timing.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{ADC}	ADC Clock frequency	Maximum is 1/4 of peripheral clock frequency	100		2000	kHz
		Measuring internal signals	100		125	
f_{ADC}	Sample rate	Current limitation (CURRLIMIT) off	100		2000	ksps
		CURRLIMIT = LOW	100		1500	
		CURRLIMIT = MEDIUM	100		1000	
		CURRLIMIT = HIGH	100		500	
	Sampling time	1/2 Clk_{ADC} cycle	0.25		5	µs
	Conversion time (latency)	(RES+2)/2+(GAIN !=0) RES (Resolution) = 8 or 12	5		8	Clk_{ADC} cycles
	Start-up time	ADC clock cycles		12	24	Clk_{ADC} cycles
	ADC settling time	After changing reference or input mode		7	7	Clk_{ADC} cycles
		After ADC flush		1	1	

37.1.14.3 Calibrated and tunable 32MHz internal oscillator characteristics

Table 37-24. 32MHz internal oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Tunable frequency range	DFLL can tune to this frequency over voltage and temperature	30		35	MHz
	Factory calibrated frequency			32		
	Factory calibration accuracy	T = 85°C, V_{CC}= 3.0V	-1.5		1.5	%
	DFLL calibration step size			0.24		

37.1.14.4 32kHz Internal ULP Oscillator characteristics

Table 37-25. 32kHz internal ULP oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Output frequency			32		kHz
	Accuracy		-30		30	%

37.1.14.5 Internal Phase Locked Loop (PLL) characteristics

Table 37-26. Internal PLL characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{IN}	Input frequency	Output frequency must be within f_{OUT}	0.4		64	MHz
f_{OUT}	Output frequency[1]	V_{CC}= 1.6V	20		32	
		V_{CC}= 2.7V	20		96	
		V_{CC}= 3.6V	20		128	
	Duty cycle			50		%
	Start-up lock time	f_{OUT} = 48MHz		18		µs
	Re-lock time	$f_{OUT-init}$ = 10MHz, $f_{OUT-end}$ = 64MHz		17		

Note: 1. The maximum output frequency vs. supply voltage is linear between 1.8V and 2.7V, and can never be higher than four times the maximum CPU frequency.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{CL}	Clock Low Time	V_{CC} = 1.6 - 1.8V	4.5			ns
		V_{CC} = 2.7 - 3.6V	2.4			
t_{CR}	Rise Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			1.5	ns
		V_{CC} = 2.7 - 3.6V			1.0	
t_{CF}	Fall Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			1.5	ns
		V_{CC} = 2.7 - 3.6V			1.0	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Notes: 1. System Clock Prescalers must be set so that maximum CPU clock frequency for device is not exceeded.
2. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

37.1.14.7 External 16MHz crystal oscillator and XOSC characteristics

Table 37-29. External 16MHz crystal oscillator and XOSC characteristics.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Cycle to cycle jitter	FRQRANGE=0			<10		ns
		FRQRANGE=1, 2, 3			<1		
	Frequency error	FRQRANGE=0			<0.5		%
		FRQRANGE=1			<0.05		
		FRQRANGE=2			<0.005		
		FRQRANGE=3			<0.005		
	Duty cycle	FRQRANGE=0			50		
		FRQRANGE=1			50		
		FRQRANGE=2			50		
		FRQRANGE=3			50		

37.2 ATxmega128A1U

37.2.1 Absolute Maximum Ratings

Stresses beyond those listed in Table 37-35 on page 97 under may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 37-35. Absolute maximum ratings.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		-0.3		4	V
I_{VCC}	Current into a V_{CC} pin				200	mA
I_{GND}	Current out of a Gnd pin				200	
V_{PIN}	Pin voltage with respect to Gnd and V_{CC}		-0.5		V_{CC}+0.5	V
I_{PIN}	I/O pin sink/source current		-25		25	mA
T_A	Storage temperature		-65		150	°C
T_j	Junction temperature				150	

37.2.2 General Operating Ratings

The device must operate within the ratings listed in Table 37-36 in order for all other electrical characteristics and typical characteristics of the device to be valid.

Table 37-36. General operating conditions.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		1.60		3.6	V
AV_{CC}	Analog supply voltage		1.60		3.6	
T_A	Temperature range		-40		85	°C
T_j	Junction temperature		-40		105	

Table 37-37. Operating voltage and frequency.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{CPU}	CPU clock frequency	V_{CC} = 1.6V	0		12	MHz
		V_{CC} = 1.8V	0		12	
		V_{CC} = 2.7V	0		32	
		V_{CC} = 3.6V	0		32	

The maximum CPU clock frequency depends on V_{CC}. As shown in Figure 37-8 the Frequency vs. V_{CC} curve is linear between 1.8V < V_{CC} < 2.7V.

37.2.6 ADC characteristics

Table 37-42. Power supply, reference and input range.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
AV_{CC}	Analog supply voltage		V_{CC}- 0.3		V_{CC}+ 0.3	V
V_{REF}	Reference voltage		1		AV_{CC}- 0.6	
R_{in}	Input resistance	Switched		5.0		kΩ
C_{in}	Input capacitance	Switched		5.0		pF
R_{AREF}	Reference input resistance	(leakage only)		>10		MΩ
C_{AREF}	Reference input capacitance	Static load		7		pF
V_{IN}	Input range		-0.1		AV_{CC}+0.1	V
	Conversion range	Differential mode, Vinp - Vinn	$-V_{REF}$		V_{REF}	
V_{IN}	Conversion range	Single ended unsigned mode, Vinp	-ΔV		V_{REF}-ΔV	
ΔV	Fixed offset voltage			190		LSB

Table 37-43. Clock and timing.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{ADC}	ADC Clock frequency	Maximum is 1/4 of peripheral clock frequency	100		2000	kHz
		Measuring internal signals	100		125	
f_{ADC}	Sample rate	Current limitation (CURRLIMIT) off	100		2000	ksps
		CURRLIMIT = LOW	100		1500	
		CURRLIMIT = MEDIUM	100		1000	
		CURRLIMIT = HIGH	100		500	
	Sampling time	1/2 Clk_{ADC} cycle	0.25		5	µs
	Conversion time (latency)	(RES+2)/2+(GAIN !=0) RES (Resolution) = 8 or 12	5		8	Clk_{ADC} cycles
	Start-up time	ADC clock cycles		12	24	Clk_{ADC} cycles
	ADC settling time	After changing reference or input mode		7	7	Clk_{ADC} cycles
		After ADC flush		1	1	

37.2.15 SPI Characteristics

Figure 37-12.SPI timing requirements in master mode.

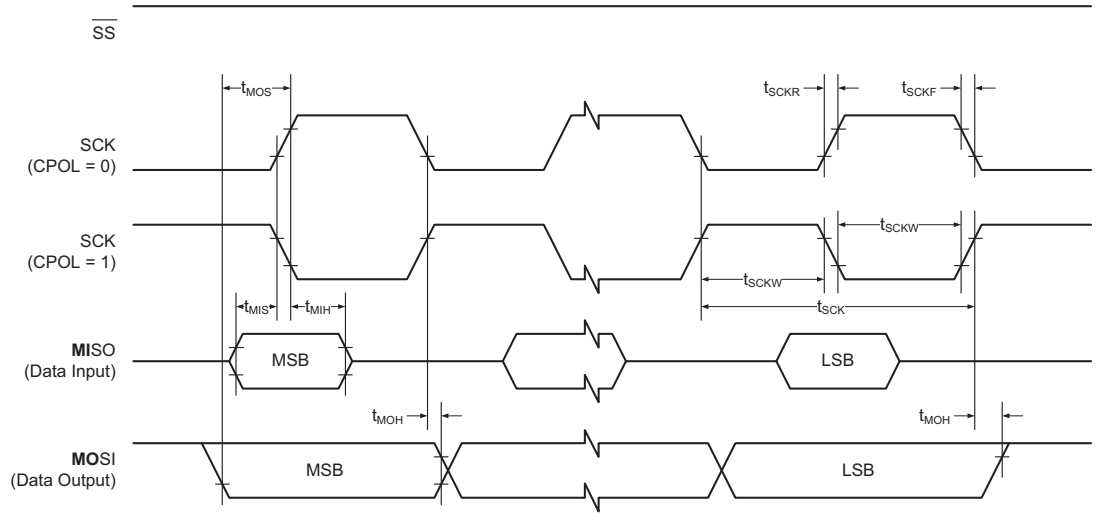


Figure 37-13.SPI timing requirements in slave mode.

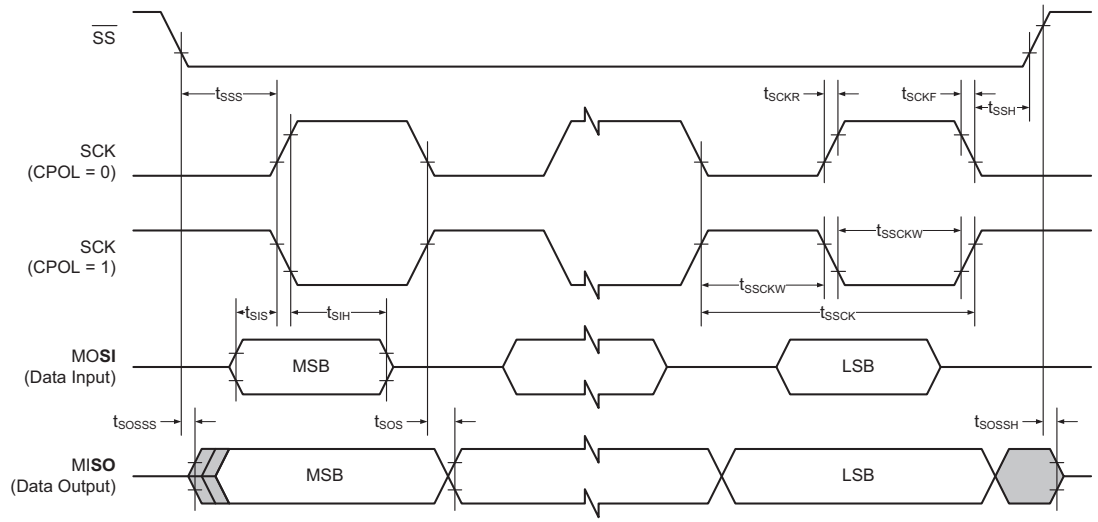


Table 37-65. SPI timing characteristics and requirements.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{SCK}	SCK period	Master		(See Table 21-4 in XMEGA AU Manual)		ns
t_{SCKW}	SCK high/low width	Master		0.5*SCK		
t_{SCKR}	SCK rise time	Master		2.7		
t_{SCKF}	SCK fall time	Master		2.7		
t_{MIS}	MISO setup to SCK	Master		11		
t_{MIH}	MISO hold after SCK	Master		0		
t_{MOS}	MOSI setup SCK	Master		0.5*SCK		
t_{MOH}	MOSI hold after SCK	Master		1		
	SCK to out high	Master		1		
t_{SSCK}	Slave SCK period	Slave	$4*t_{ClkPER}$			
t_{SSCKW}	SCK high/low width	Slave	$2*t_{ClkPER}$			
t_{SSCKR}	SCK rise time	Slave			1600	
t_{SSCKF}	SCK fall time	Slave			1600	
t_{SIS}	MOSI setup to SCK	Slave	3			
t_{SIH}	MOSI hold after SCK	Slave	t_{SCK}			
t_{SSS}	$\overline{SS}$ setup to SCK	Slave	20			
t_{SSH}	$\overline{SS}$ hold after SCK	Slave	20			
t_{SOS}	MISO setup SCK	Slave		8		
t_{SOH}	MISO hold after SCK	Slave		13		
t_{SOSS}	MISO setup after $\overline{SS}$ low	Slave		11		
t_{SOSH}	MISO hold after $\overline{SS}$ high	Slave		8		

Figure 38-5. Active mode supply current vs. V_{CC}.

f_{SYS} = 2MHz internal oscillator.

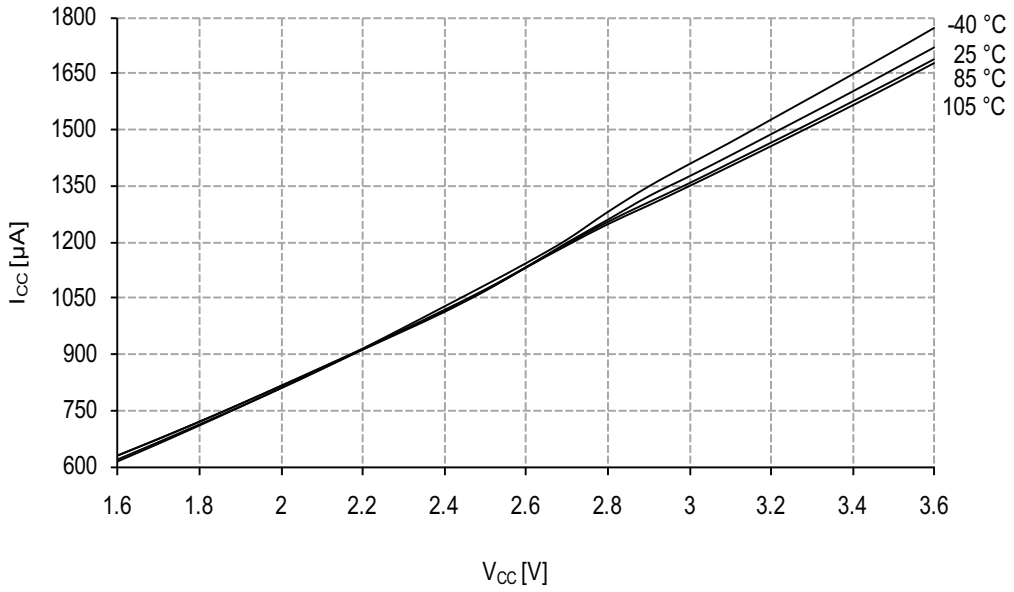


Figure 38-6. Active mode supply current vs. V_{CC}.

f_{SYS} = 32MHz internal oscillator prescaled to 8MHz.

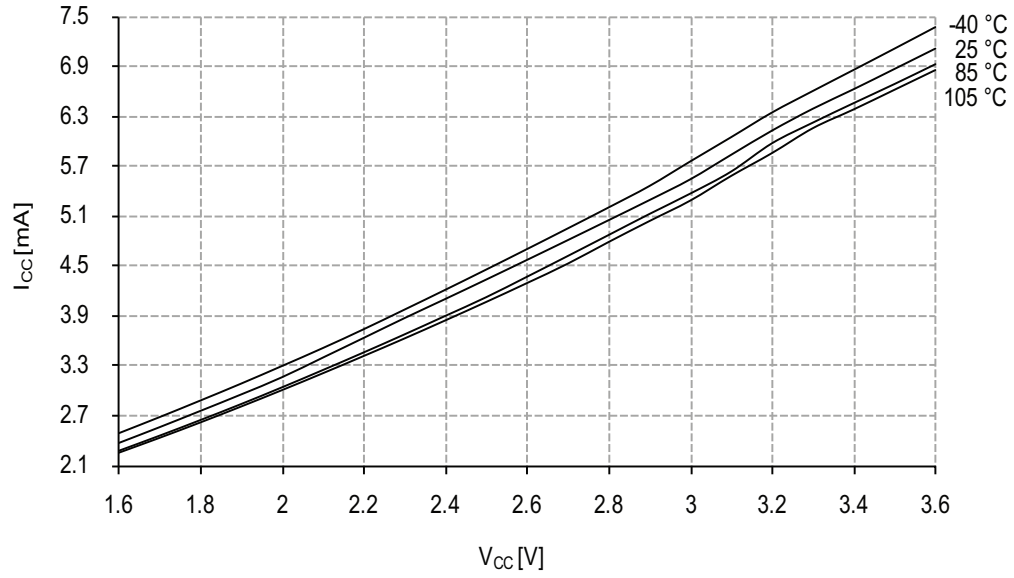
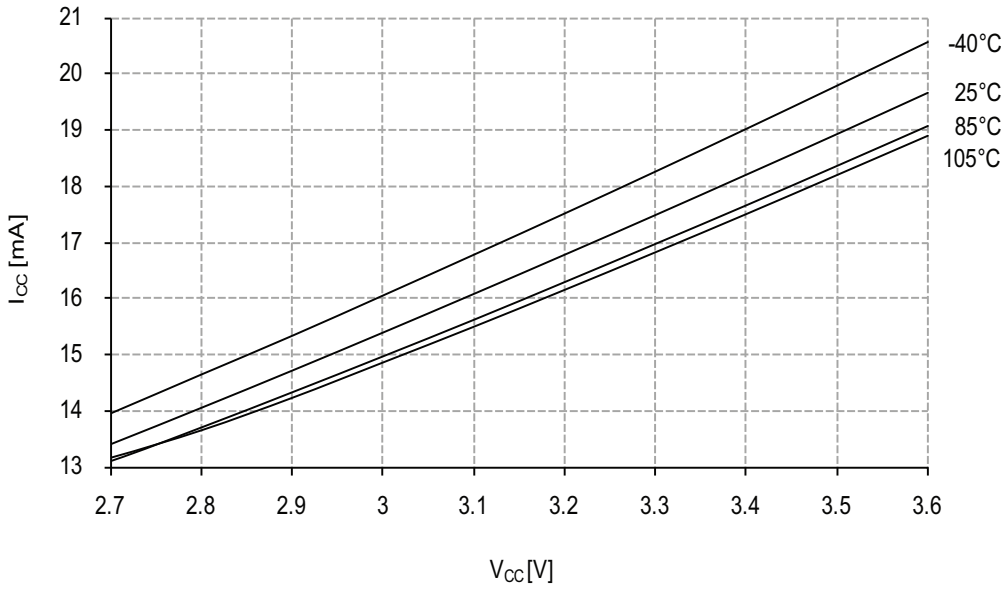


Figure 38-7. Active mode supply current vs. V_{CC}.

f_{SYS} = 32MHz internal oscillator.



38.1.1.2 Idle mode supply current

Figure 38-8. Idle mode supply current vs. frequency.

f_{SYS} = 0 - 1MHz external clock, T = 25°C.

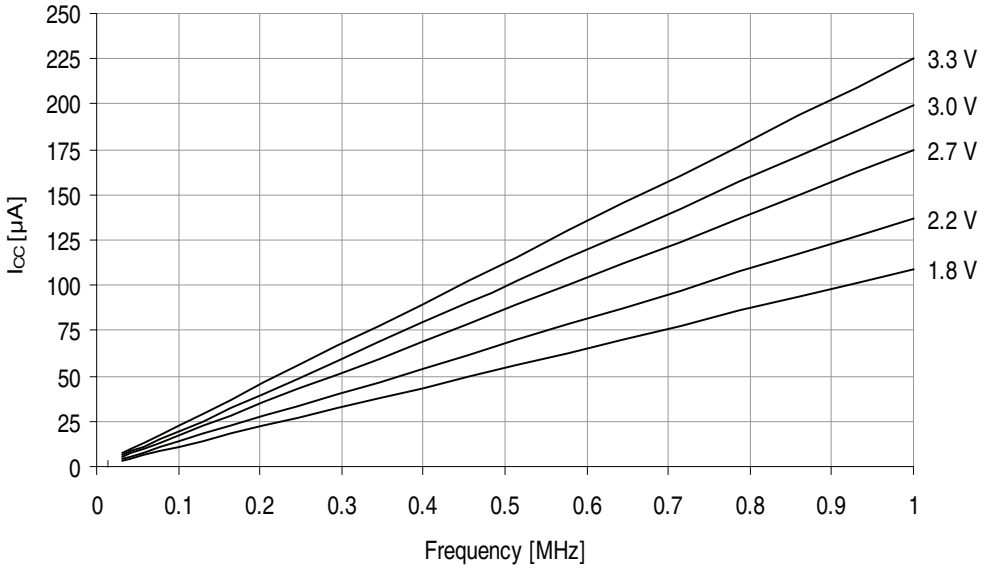


Figure 38-55.Analog comparator current source vs. calibration value.

Temperature = 25°C.

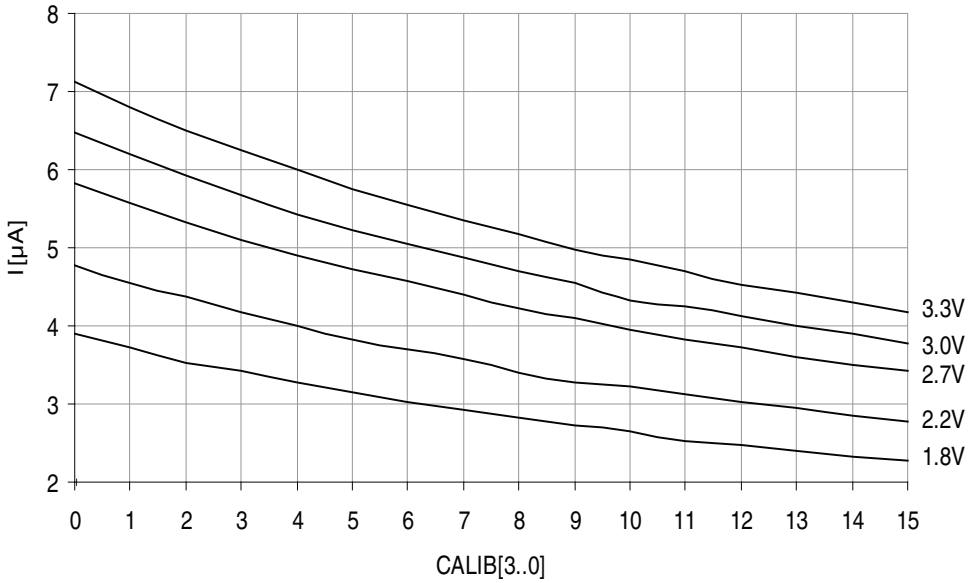
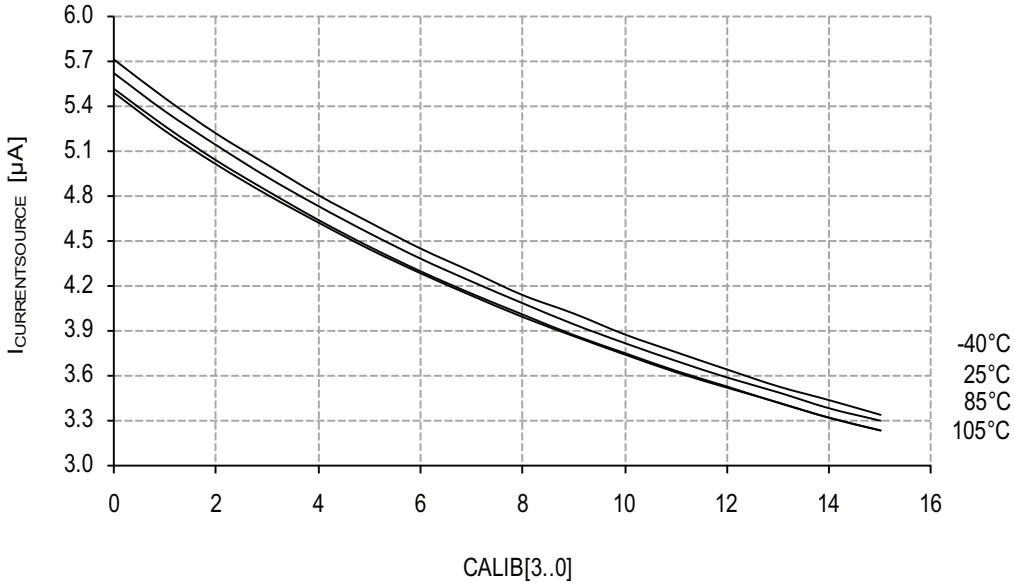


Figure 38-56.Analog comparator current source vs. calibration value.

V_{CC} = 3.0V.



38.1.9 Power-on Reset Characteristics

Figure 38-67.Power-on reset current consumption vs. V_{CC}.

BOD level = 3.0V, enabled in continuous mode.

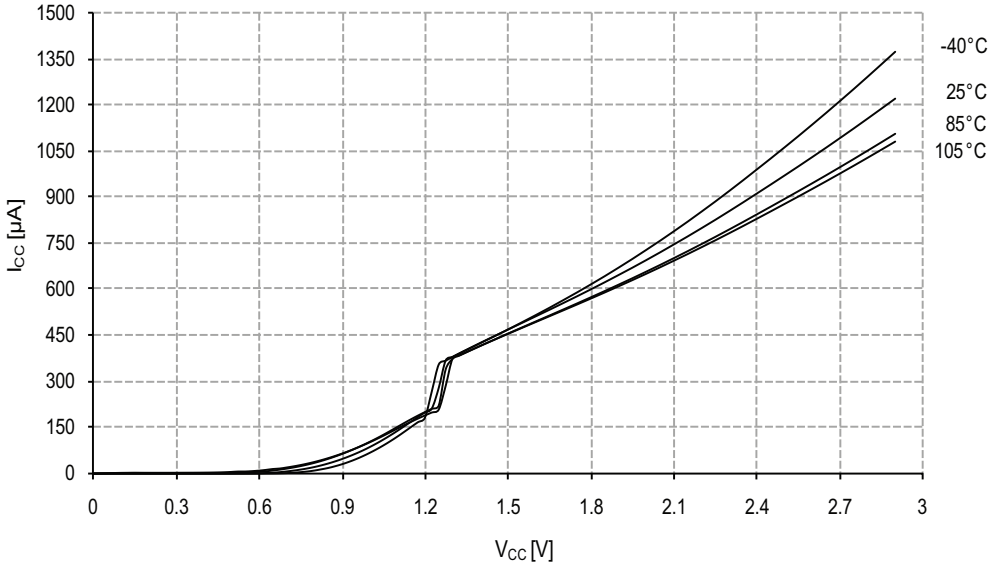


Figure 38-68.Power-on reset current consumption vs. V_{CC}.

BOD level = 3.0V, enabled in sampled mode.

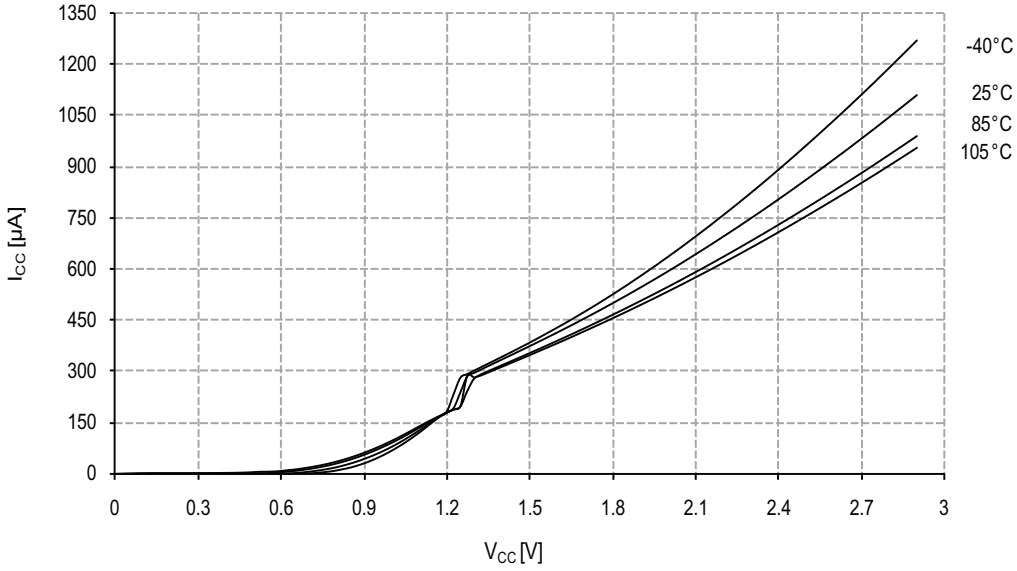


Figure 38-77. 32MHz internal oscillator CALA calibration step size.

V_{CC} = 3.0V.

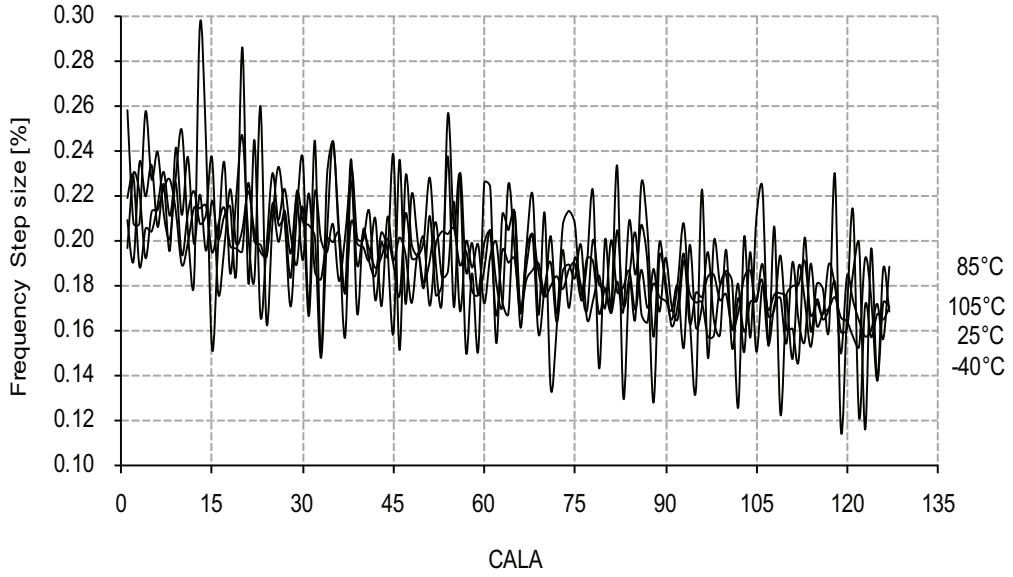
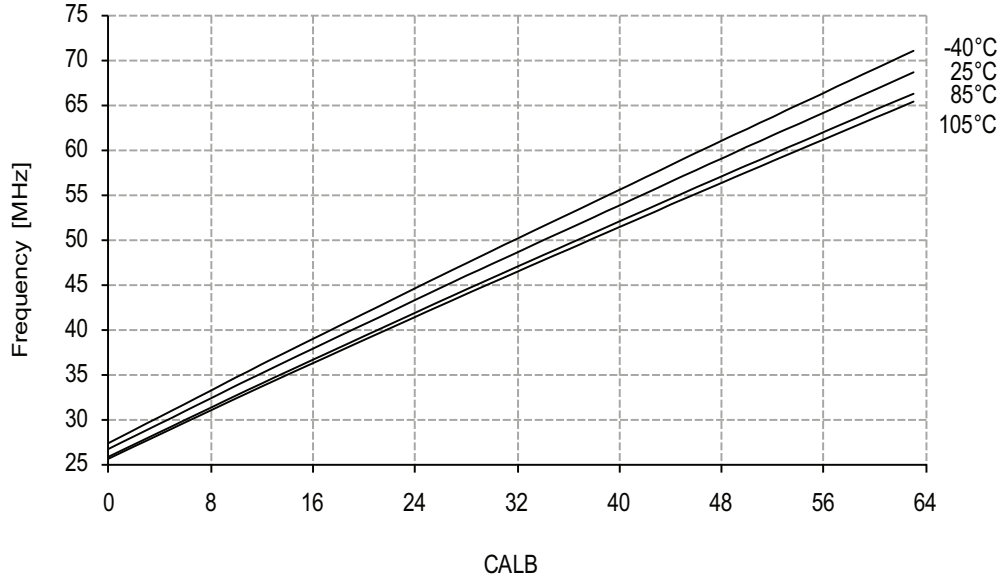


Figure 38-78. 32MHz internal oscillator frequency vs. CALB calibration value.

V_{CC} = 3.0V, DFLL disabled.



38.2 ATxmega128A1U

38.2.1 Current consumption

38.2.1.1 Active mode supply current

Figure 38-83. Active supply current vs. frequency.

f_{SYS} = 0 - 1MHz external clock, T = 25°C.

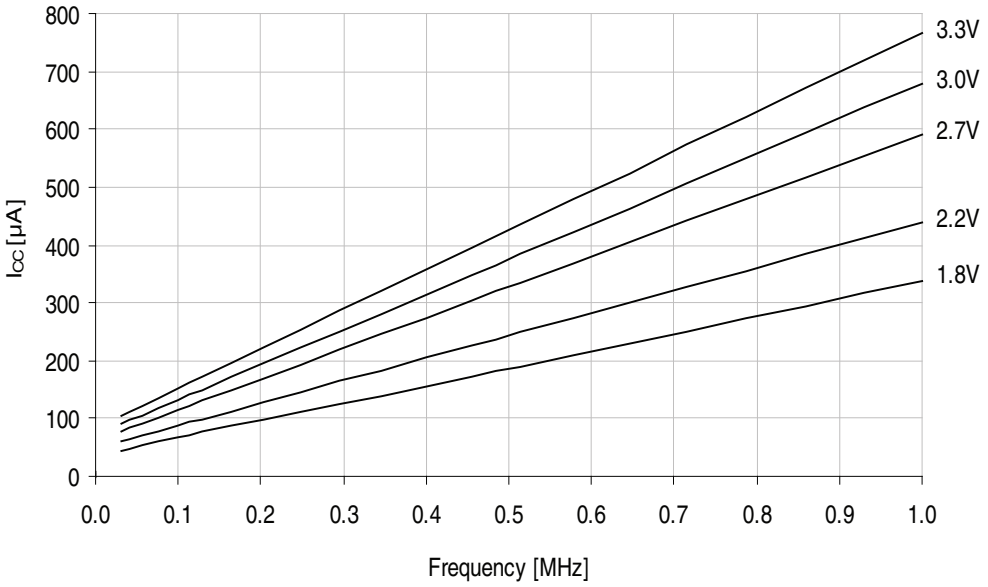


Figure 38-84. Active supply current vs. frequency.

f_{SYS} = 1 - 32MHz external clock, T = 25°C.

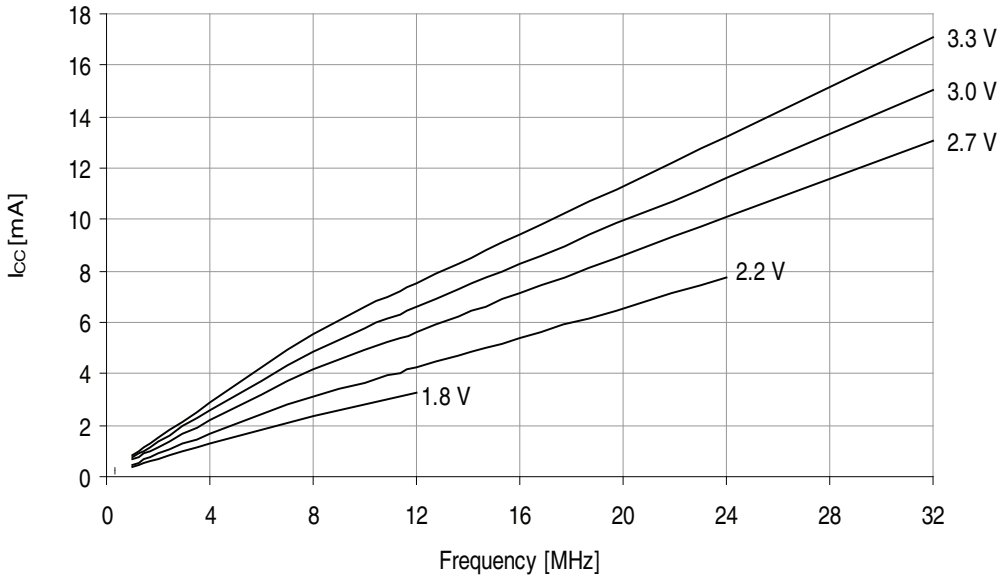


Figure 38-91.Idle mode supply current vs. frequency.

f_{SYS} = 1 - 32MHz external clock, T = 25°C.

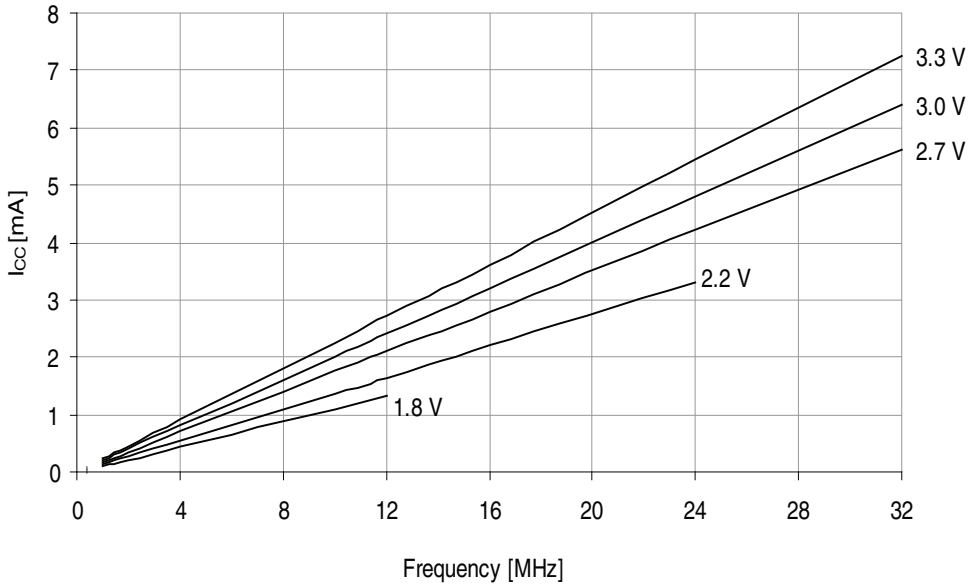


Figure 38-92.Idle mode supply current vs. V_{CC}.

f_{SYS} = 32.768kHz internal oscillator.

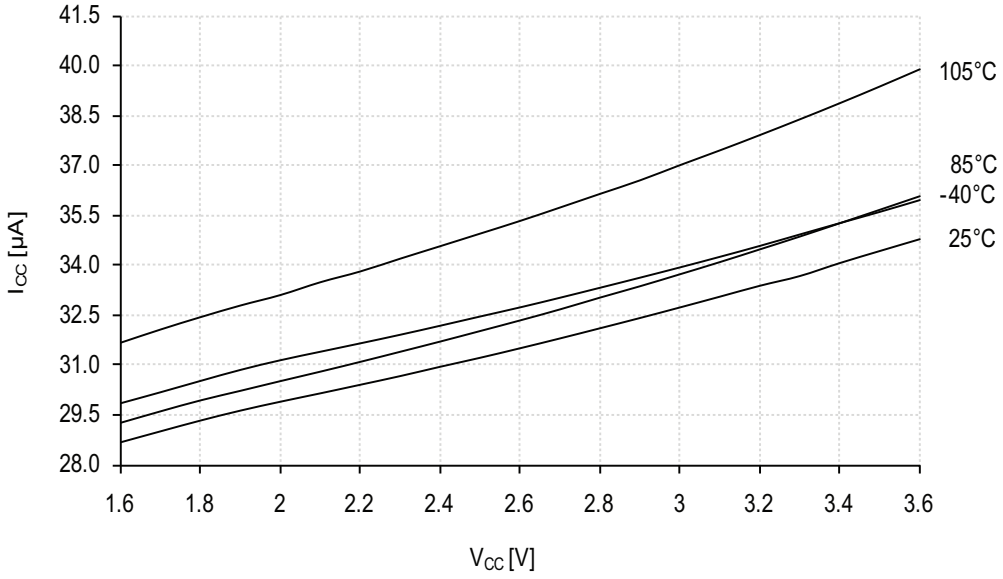


Figure 38-111.I/O pin output voltage vs. sink current.

V_{CC} = 3.3V.

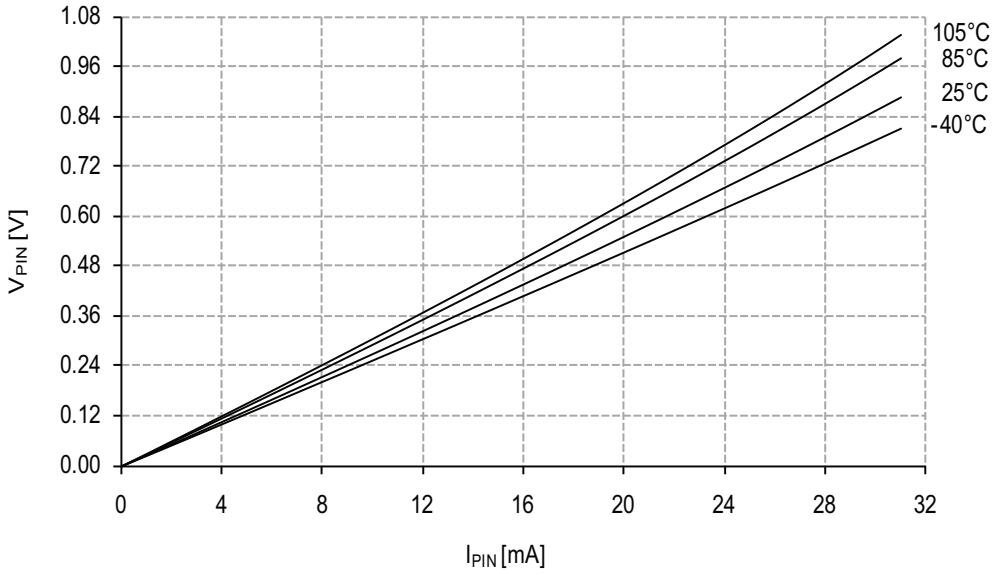


Figure 38-112.I/O pin output voltage vs. sink current.

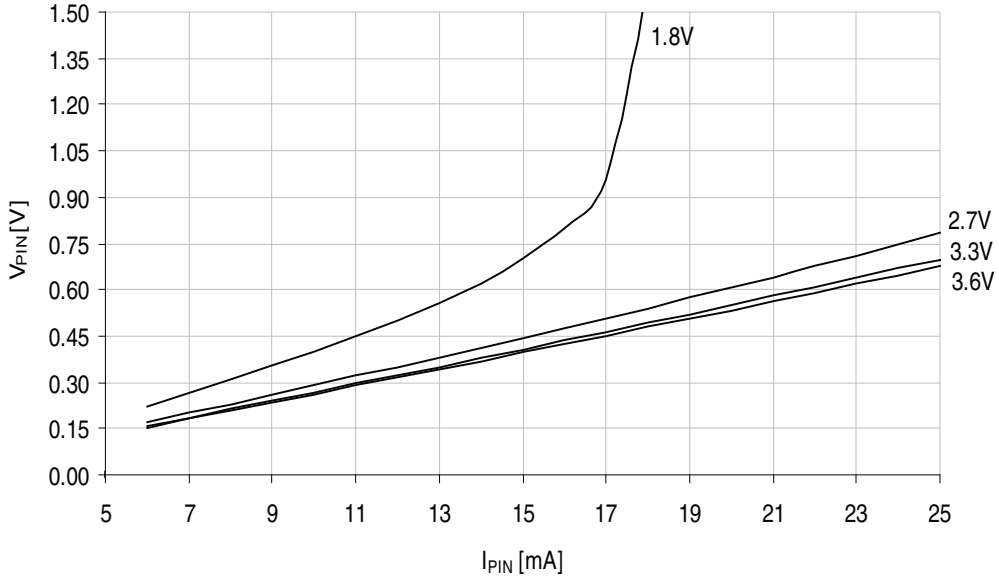


Figure 38-115.I/O pin input threshold voltage vs. V_{CC}.

V_{IL} I/O pin read as "0".

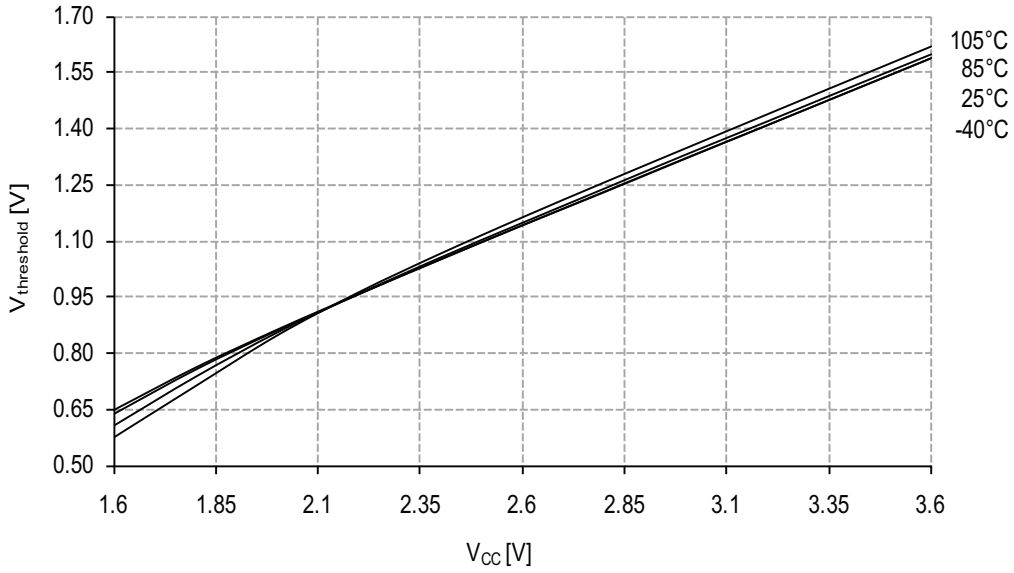


Figure 38-116.I/O pin input hysteresis vs. V_{CC}.