Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	EBI/EMI, I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	78
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega64a1u-anr

11. Power Management and Sleep Modes

11.1 Features

- Power management for adjusting power consumption and functions
- Five sleep modes
  - Idle
  - Power down
  - Power save
  - Standby
  - Extended standby
- Power reduction register to disable clock and turn off unused peripherals in active and idle modes

11.2 Overview

Various sleep modes and clock gating are provided in order to tailor power consumption to application requirements. This enables the Atmel AVR XMEGA microcontroller to stop unused modules to save power.

All sleep modes are available and can be entered from active mode. In active mode, the CPU is executing application code. When the device enters sleep mode, program execution is stopped and interrupts or a reset is used to wake the device again. The application code decides which sleep mode to enter and when. Interrupts from enabled peripherals and all enabled reset sources can restore the microcontroller from sleep to active mode.

In addition, power reduction registers provide a method to stop the clock to individual peripherals from software. When this is done, the current state of the peripheral is frozen, and there is no power consumption from that peripheral. This reduces the power consumption in active mode and idle sleep modes and enables much more fine-tuned power management than sleep modes alone.

11.3 Sleep Modes

Sleep modes are used to shut down modules and clock domains in the microcontroller in order to save power. XMEGA microcontrollers have five different sleep modes tuned to match the typical functional stages during application execution. A dedicated sleep instruction (SLEEP) is available to enter sleep mode. Interrupts are used to wake the device from sleep, and the available interrupt wake-up sources are dependent on the configured sleep mode. When an enabled interrupt occurs, the device will wake up and execute the interrupt service routine before continuing normal program execution from the first instruction after the SLEEP instruction. If other, higher priority interrupts are pending when the wake-up occurs, their interrupt service routines will be executed according to their priority before the interrupt service routine for the wake-up interrupt is executed. After wake-up, the CPU is halted for four cycles before execution starts.

The content of the register file, SRAM and registers are kept during sleep. If a reset occurs during sleep, the device will reset, start up, and execute from the reset vector.

11.3.1 Idle Mode

In idle mode the CPU and nonvolatile memory are stopped (note that any ongoing programming will be completed), but all peripherals, including the interrupt controller, event system and DMA controller are kept running. Any enabled interrupt will wake the device.

11.3.2 Power-down Mode

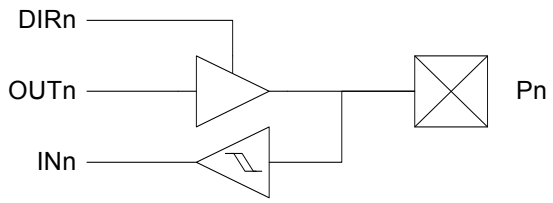
In power-down mode, all clocks, including the real-time counter clock source, are stopped. This allows operation only of asynchronous modules that do not require a running clock. The only interrupts that can wake up the MCU are the two-wire interface address match interrupt, asynchronous port interrupts, and the USB resume interrupt.

15.3 Output Driver

All port pins (Pn) have programmable output configuration. The port pins also have configurable slew rate limitation to reduce electromagnetic emission.

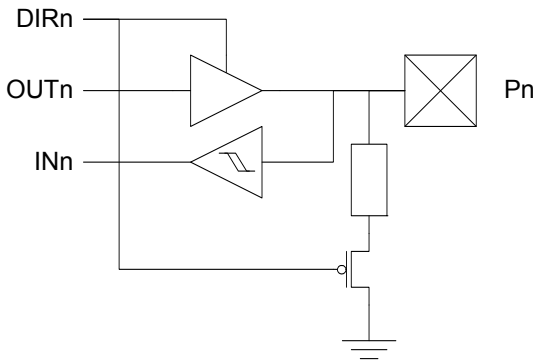
15.3.1 Push-pull

Figure 15-1. I/O configuration - Totem-pole.



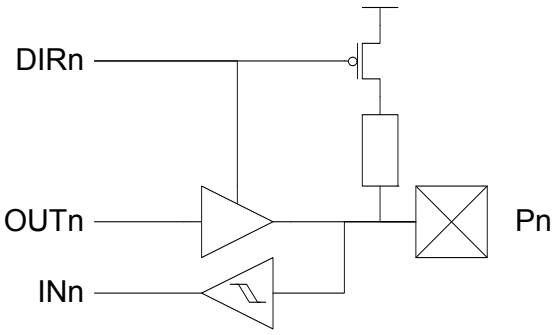
15.3.2 Pull-down

Figure 15-2. I/O configuration - Totem-pole with pull-down (on input).



15.3.3 Pull-up

Figure 15-3. I/O configuration - Totem-pole with pull-up (on input).

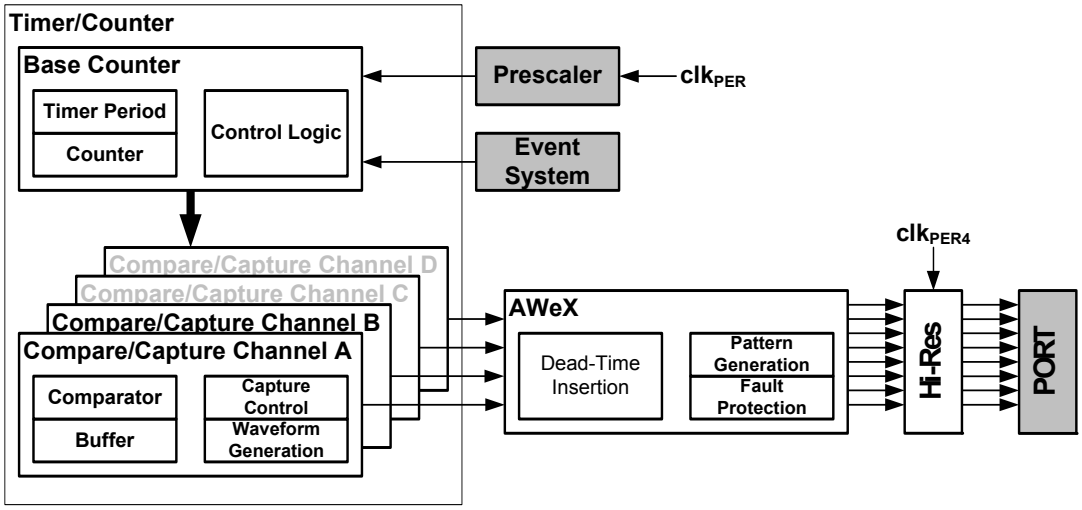


Some timer/counters have extensions to enable more specialized waveform and frequency generation. The advanced waveform extension (AWeX) is intended for motor control and other power control applications. It enables low- and high-side output with dead-time insertion, as well as fault protection for disabling and shutting down external drivers. It can also generate a synchronized bit pattern across the port pins.

The advanced waveform extension can be enabled to provide extra and more advanced features for the Timer/Counter. This is only available for Timer/Counter 0. See "“AWeX – Advanced Waveform Extension” on page 37 for more details.

The high-resolution (hi-res) extension can be used to increase the waveform output resolution by four or eight times by using an internal clock source running up to four times faster than the peripheral clock. See “Hi-Res – High Resolution Extension” on page 38 for more details.

Figure 16-1. Overview of a timer/counter (TC) and closely related peripherals.



PORTC, PORTD, PORTE and PORTF each has one timer/counter 0 and one timer/counter1. Notation of these timer/counters are TCC0 (timer/counter C0), TCC1, TCD0, TCD1, TCE0, TCE1, TCF0, and TCF1, respectively.

26. AES and DES Crypto Engine

26.1 Features

- Data Encryption Standard (DES) CPU instruction
- Advanced Encryption Standard (AES) crypto module
- DES Instruction
  - Encryption and decryption
  - DES supported
  - Encryption/decryption in 16 CPU clock cycles per 8-byte block
- AES crypto module
  - Encryption and decryption
  - Supports 128-bit keys
  - Supports XOR data load mode to the state memory
  - Encryption/decryption in 375 clock cycles per 16-byte block

26.2 Overview

The Advanced Encryption Standard (AES) and Data Encryption Standard (DES) are two commonly used standards for cryptography. These are supported through an AES peripheral module and a DES CPU instruction, and the communication interfaces and the CPU can use these for fast, encrypted communication and secure data storage.

DES is supported by an instruction in the AVR CPU. The 8-byte key and 8-byte data blocks must be loaded into the register file, and then the DES instruction must be executed 16 times to encrypt/decrypt the data block.

The AES crypto module encrypts and decrypts 128-bit data blocks with the use of a 128-bit key. The key and data must be loaded into the key and state memory in the module before encryption/decryption is started. It takes 375 peripheral clock cycles before the encryption/decryption is done. The encrypted/encrypted data can then be read out, and an optional interrupt can be generated. The AES crypto module also has DMA support with transfer triggers when encryption/decryption is done and optional auto-start of encryption/decryption when the state memory is fully loaded.

28. EBI – External Bus Interface

28.1 Features

- Supports SRAM up to:
  - 512KB using 2- or 3-port EBI configuration
  - 16MB using 3- or 4-port EBI configuration
- Supports SDRAM up to:
  - 128Mb using 3- or 4-port EBI configuration
  - 4-bit SDRAM with 3-port EBI configuration
  - 4- or 8-bit SDRAM with 4-port EBI configuration
- Four software configurable chip selects
- Software configurable wait state insertion
- Can run from the 2x peripheral clock frequency for fast access
- Simultaneous SRAM and SDRAM support with 4-port EBI configuration

28.2 Overview

The External Bus Interface (EBI) is used to connect external peripherals and memory for accessthrough the data memory space. When the EBI is enabled, data address space outside the internal SRAM becomes available using dedicated EBI pins.

The EBI can interface external SRAM, SDRAM, and peripherals, such as LCD displays and other memory mapped devices.

The address space for the external memory is selectable from 256 bytes (8-bit) up to 16MB (24-bit). Various multiplexing modes for address and data lines can be selected for optimal use of pins when more or fewer pins are available for the EBI. The complete memory will be mapped into one linear data address space continuing from the end of the internal SRAM.

The EBI has four chip selects, each with separate configuration. Each can be configured for SRAM, SRAM low pin count (LPC), or SDRAM.

The EBI is clocked from the fast, 2x peripheral clock, running up to two times faster than the CPU.

Four-bit and eight-bit SDRAM are supported, and SDRAM configurations, such as CAS latency and refresh rate, are configurable in software.

Table 37-10. Accuracy characteristics.

Symbol	Parameter	Condition[2]		Min.	Typ.	Max.	Units
RES	Resolution	Programmable to 12-bit		11	11.5	12	Bits
INL[1]	Integral non-linearity	500ksps, differential mode	V_{CC}-1.0V < V_{REF}< V_{CC}-0.6V		±1.2	±2	lsb
			All V_{REF}		±1.5	±3	
		2000ksps, differential mode	V_{CC}-1.0V < V_{REF}< V_{CC}-0.6V		±1.0	±2	
			All V_{REF}		±1.5	±3	
		single ended mode			±1.5	±4	
DNL[1]	Differential non-linearity	guaranteed monotonic			<±0.5	<±1	
	Offset Error				-1		mV
		Temperature drift			<0.01		mV/K
		Operating voltage drift			<0.6		mV/V
	Gain Error	Differential mode	External reference		-1		mV
			AV_{CC}/1.6		10		
			AV_{CC}/2.0		8		
			Bandgap		±5		
		Temperature drift			<0.02		mV/K
		Operating voltage drift			<0.5		mV/V
	Noise	Differential mode, shorted input 2msps, V_{CC} = 3.6V, Clk_{PER} = 16MHz			0.4		mV rms

Notes: 1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% input voltage range.
2. Unless otherwise noted all linearity, offset and gain error numbers are valid under the condition that external V_{REF} is used.

Table 37-11. Gain stage characteristics.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
R_{in}	Input resistance	Switched in normal mode			4.0		kΩ
C_{sample}	Input capacitance	Switched in normal mode			4.4		pF
	Signal range	Gain stage output		0		V_{CC}- 0.6	V
	Propagation delay	ADC conversion rate			1		Clk_{ADC} cycles
	Sample rate	Same as ADC		100		1000	kHz
INL[1]	Integral Non-Linearity	500ksps	All gain settings		±1.5	±3	lsb

37.1.11 External Reset Characteristics

Table 37-18. External reset characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{EXT}	Minimum reset pulse width			86	1000	ns
V_{RST}	Reset threshold voltage (V_{IH})	V_{CC} = 2.7 - 3.6V		0.60*V_{CC}		V
		V_{CC} = 1.6 - 2.7V		0.60*V_{CC}		
	Reset threshold voltage (V_{IL})	V_{CC} = 2.7 - 3.6V		0.40*V_{CC}		
		V_{CC} = 1.6 - 2.7V		0.40*V_{CC}		

37.1.12 Power-on Reset Characteristics

Table 37-19. Power-on reset characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{POT-} (1)	POR threshold voltage falling V_{CC}	V_{CC} falls faster than 1V/ms	0.4	1.0		V
		V_{CC} falls at 1V/ms or slower	0.8	1.0		
V_{POT+}	POR threshold voltage rising V_{CC}			1.3	1.59	

Note: 1. V_{POT-} values are only valid when BOD is disabled. When BOD is enabled V_{POT-} = V_{POT+}.

37.1.13 Flash and EEPROM Memory Characteristics

Table 37-20. Endurance and data retention.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Flash	Write/Erase cycles	25°C	10K			Cycle
			85°C	10K			
			105°C	2K			
		Data retention	25°C	100			Year
			85°C	25			
			105°C	10			
	EEPROM	Write/Erase cycles	25°C	100K			Cycle
			85°C	100K			
			105°C	30K			
		Data retention	25°C	100			Year
			85°C	25			
			105°C	10			

37.1.15 SPI Characteristics

Figure 37-5. SPI timing requirements in master mode.

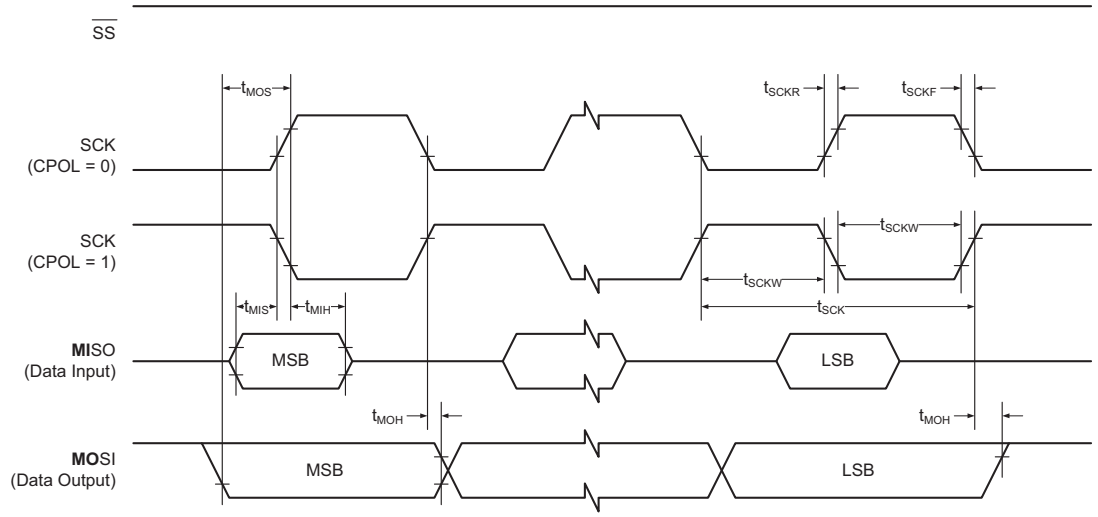
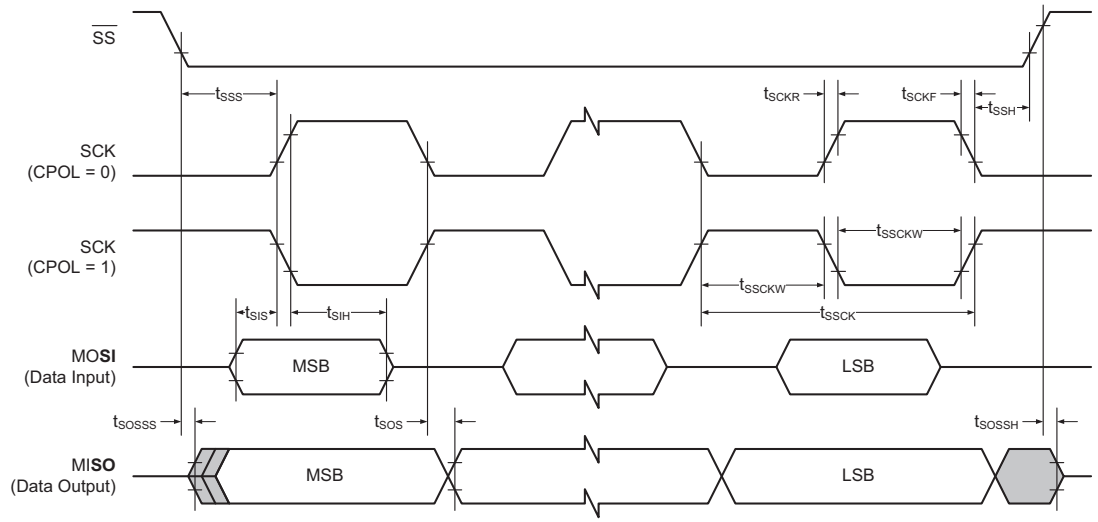


Figure 37-6. SPI timing requirements in slave mode.



37.1.16 EBI characteristics

Table 37-32. EBI SRAM characteristics and requirements.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$t_{ClkPER2}$	SRAM clock period		0.5*t_{ClkPER}			
t_{ALH}	SRAM address hold after ALE low			$t_{ClkPER2}$		
t_{ALS}	SRAM address setup before ALE low (read and write)			$t_{ClkPER2}$		
t_{ALW}	SRAM ALE width			$t_{ClkPER2}$		
t_{ARH}	SRAM address hold after RE high			$t_{ClkPER2}$		
t_{ARS}	SRAM address setup before RE high			$t_{ClkPER2}$		
t_{AWH}	SRAM address hold after WE high			$t_{ClkPER2}$		
t_{AWS}	SRAM Address setup before WE high			$t_{ClkPER2}$		
t_{DRH}	SRAM data hold after RE high		0			
t_{DRS}	SRAM data setup to RE high	3.0V		12		
t_{DRS}	SRAM data setup to RE high	2.7V, 85°C	17			ns
t_{DRS}	SRAM data setup to RE high	1.6V, 85°C	27			
t_{DWH}	SRAM data hold after WE high			$t_{ClkPER2}$		
t_{DWS}	SRAM data setup to WE high			$t_{ClkPER2}$		
t_{RW}	SRAM read enable pulse width			$t_{ClkPER2}$*S_{RWS}		
t_{WW}	SRAM write enable pulse width			$t_{ClkPER2}$*S_{RWS}		
t_{CH}	SRAM chip select hold after RE/WE high			$t_{ClkPER2}$		
t_{CRS}	SRAM chip select setup to RE low or ALE high			0		
t_{CWS}	SRAM chip select setup to WE low (no ALE)			$t_{ClkPER2}$		

Table 37-48. Accuracy characteristics.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
RES	Input resolution					12	Bits
INL[1]	Integral non-linearity	V_{REF}= Ext 1.0V	V_{CC} = 1.6V		±2.0	±3	lsb
			V_{CC} = 3.6V		±1.5	±2.5	
		V_{REF}=AV_{CC}	V_{CC} = 1.6V		±2.0	±4	
			V_{CC} = 3.6V		±1.5	±4	
		V_{REF}=INT1V	V_{CC} = 1.6V		±5.0		
			V_{CC} = 3.6V		±5.0		
DNL[1]	Differential non-linearity	V_{REF}=Ext 1.0V	V_{CC} = 1.6V		±1.5	3.0	
			V_{CC} = 3.6V		±0.6	1.5	
		V_{REF}=AV_{CC}	V_{CC} = 1.6V		±1.0	3.5	
			V_{CC} = 3.6V		±0.6	1.5	
		V_{REF}=INT1V	V_{CC} = 1.6V		±4.5		
			V_{CC} = 3.6V		±4.5		
	Gain error	After calibration			<4		
	Gain calibration step size				4		
	Gain calibration drift	V_{REF}= Ext 1.0V			<0.2		mV/K
	Offset error	After calibration			<1		lsb
	Offset calibration step size				1		

Note: 1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% output voltage range.

37.2.8 Analog Comparator Characteristics

Table 37-49. Analog Comparator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{off}	Input offset voltage			<±10		mV
I_{lk}	Input leakage current			<1		nA
	Input voltage range		-0.1		AV_{CC} +0.1	V
V_{hys1}	Hysteresis, none			0		mV
V_{hys2}	Hysteresis, small	mode = High Speed (HS)		22		
		mode = Low Power (LP)		30		
V_{hys3}	Hysteresis, large	mode = HS		43		
		mode = LP		60		

37.2.11 External Reset Characteristics

Table 37-52. External reset characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{EXT}	Minimum reset pulse width			86	1000	ns
V_{RST}	Reset threshold voltage (V_{IH})	V_{CC} = 2.7 - 3.6V		0.60*V_{CC}		V
		V_{CC} = 1.6 - 2.7V		0.60*V_{CC}		
	Reset threshold voltage (V_{IL})	V_{CC} = 2.7 - 3.6V		0.40*V_{CC}		
		V_{CC} = 1.6 - 2.7V		0.40*V_{CC}		

37.2.12 Power-on Reset Characteristics

Table 37-53. Power-on reset characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{POT-} (1)	POR threshold voltage falling V_{CC}	V_{CC} falls faster than 1V/ms	0.4	1.0		V
		V_{CC} falls at 1V/ms or slower	0.8	1.0		
V_{POT+}	POR threshold voltage rising V_{CC}			1.3	1.59	

Note: 1. V_{POT-} values are only valid when BOD is disabled. When BOD is enabled V_{POT-} = V_{POT+}.

37.2.13 Flash and EEPROM Memory Characteristics

Table 37-54. Endurance and data retention.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Flash	Write/Erase cycles	25°C	10K			Cycle
			85°C	10K			
			105°C	2K			
		Data retention	25°C	100			Year
			85°C	25			
			105°C	10			
	EEPROM	Write/Erase cycles	25°C	100K			Cycle
			85°C	100K			
			105°C	30K			
		Data retention	25°C	100			Year
			85°C	25			
			105°C	10			

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{CL}	Clock Low Time	V_{CC} = 1.6 - 1.8V	4.5			ns
		V_{CC} = 2.7 - 3.6V	2.4			
t_{CR}	Rise Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			1.5	ns
		V_{CC} = 2.7 - 3.6V			1.0	
t_{CF}	Fall Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			1.5	ns
		V_{CC} = 2.7 - 3.6V			1.0	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Notes: 1. System Clock Prescalers must be set so that maximum CPU clock frequency for device is not exceeded.
2. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

37.2.14.7 External 16MHz crystal oscillator and XOSC characteristics

Table 37-63. External 16MHz crystal oscillator and XOSC characteristics.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Cycle to cycle jitter	FRQRANGE=0			<10		ns
		FRQRANGE=1, 2, 3			<1		
	Frequency error	FRQRANGE=0			<0.5		%
		FRQRANGE=1			<0.05		
		FRQRANGE=2			<0.005		
		FRQRANGE=3			<0.005		
	Duty cycle	FRQRANGE=0			50		
		FRQRANGE=1			50		
		FRQRANGE=2			50		
		FRQRANGE=3			50		

Table 37-67. EBI SDRAM characteristics and requirements.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$t_{ClkPER2}$	SDRAM clock period		$0.5*t_{ClkPER}$			ns
t_{AH}	SDRAM address hold time			$0.5*t_{ClkPER2}$		
t_{AS}	SDRAM address setup time			$0.5*t_{ClkPER2}$		
t_{CH}	SDRAM clock high-level width			$0.5*t_{ClkPER2}$		
t_{CL}	SDRAM clock low-level width			$0.5*t_{ClkPER2}$		
t_{CKH}	SDRAM CKE hold time			$0.5*t_{ClkPER2}$		
t_{CKS}	SDRAM CKE setup time			$0.5*t_{ClkPER2}$		
t_{CMH}	SDRAM CS, RAS, CAS, WE, DQM hold time			$0.5*t_{ClkPER2}$		
t_{CMS}	SDRAM CS, RAS, CAS, WE, DQM setup time			$0.5*t_{ClkPER2}$		
t_{DRH}	SDRAM data in hold after CLK high		0			
t_{AC}	SDRAM access time from CLK				t_{ClkPER}-5	
t_{DWH}	SDRAM data out hold after CLK high			$0.5*t_{ClkPER2}$		
t_{DWS}	SDRAM data out setup before CLK high			$0.5*t_{ClkPER2}$		

37.2.17 Two-Wire Interface Characteristics

Table 37-68 on page 119 describes the requirements for devices connected to the Two-Wire Interface Bus. The Atmel AVR XMEGA Two-Wire Interface meets or exceeds these requirements under the noted conditions. Timing symbols refer to Figure 37-14.

Figure 37-14.Two-Wire Interface bus timing.

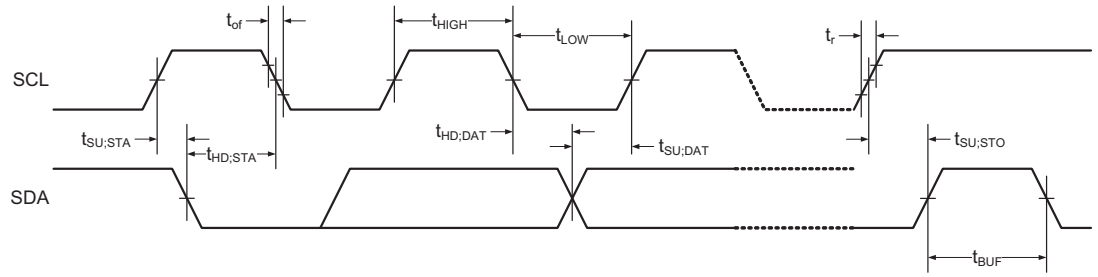


Figure 38-11.Idle mode supply current vs. V_{CC}.

f_{SYS} = 1MHz external clock.

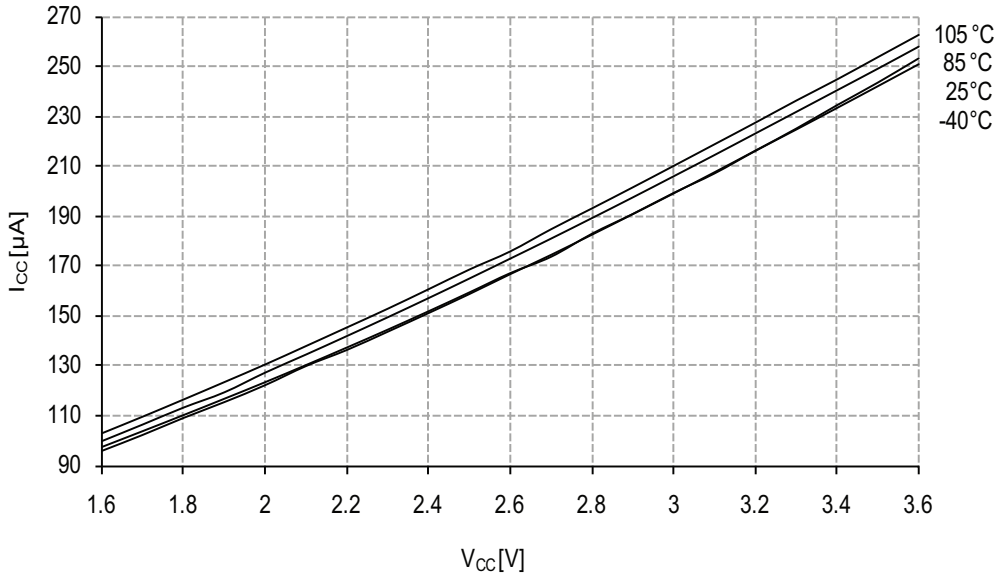


Figure 38-12.Idle mode supply current vs. V_{CC}.

f_{SYS} = 2MHz internal oscillator.

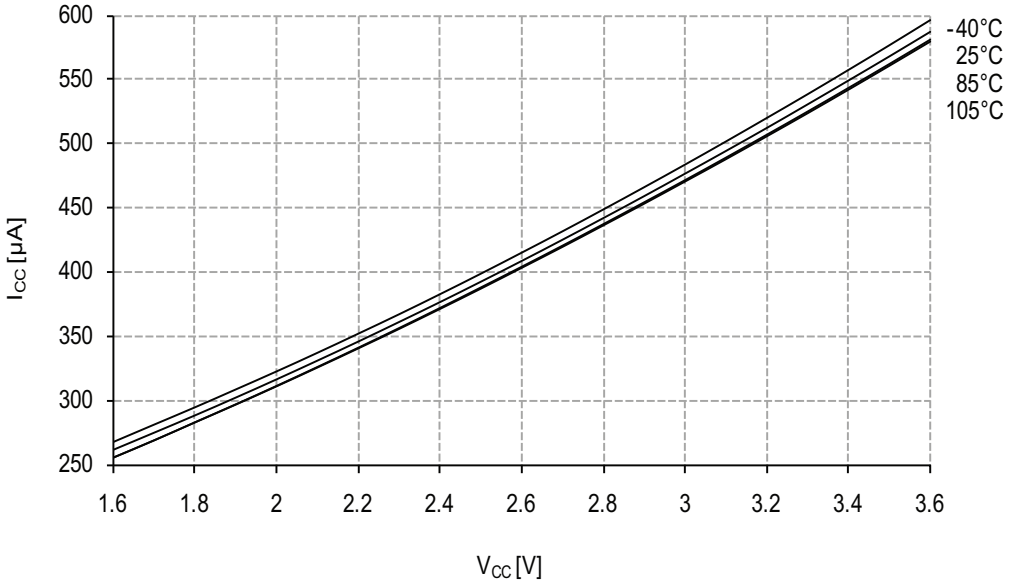


Figure 38-137.Analog comparator current source vs. calibration value.

Temperature = 25°C.

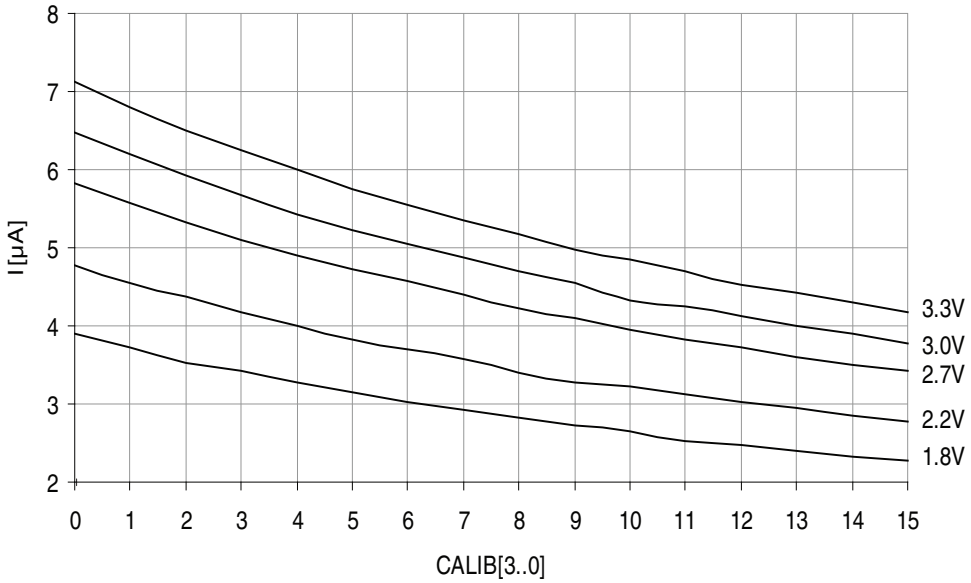
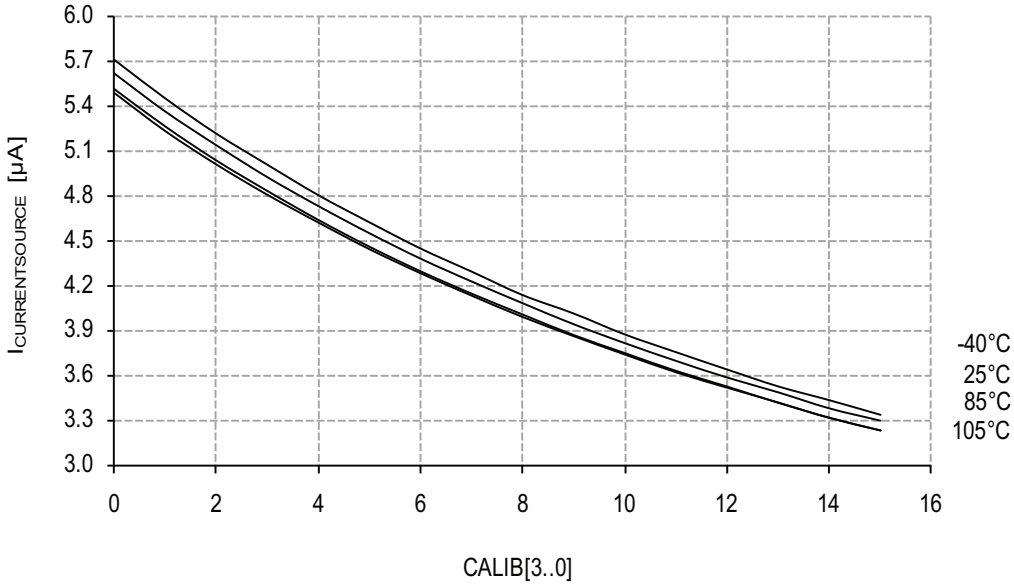


Figure 38-138.Analog comparator current source vs. calibration value.

V_{CC} = 3.0V.



38.2.8 External Reset Characteristics

Figure 38-143.Minimum Reset pin pulse width vs. V_{CC}.

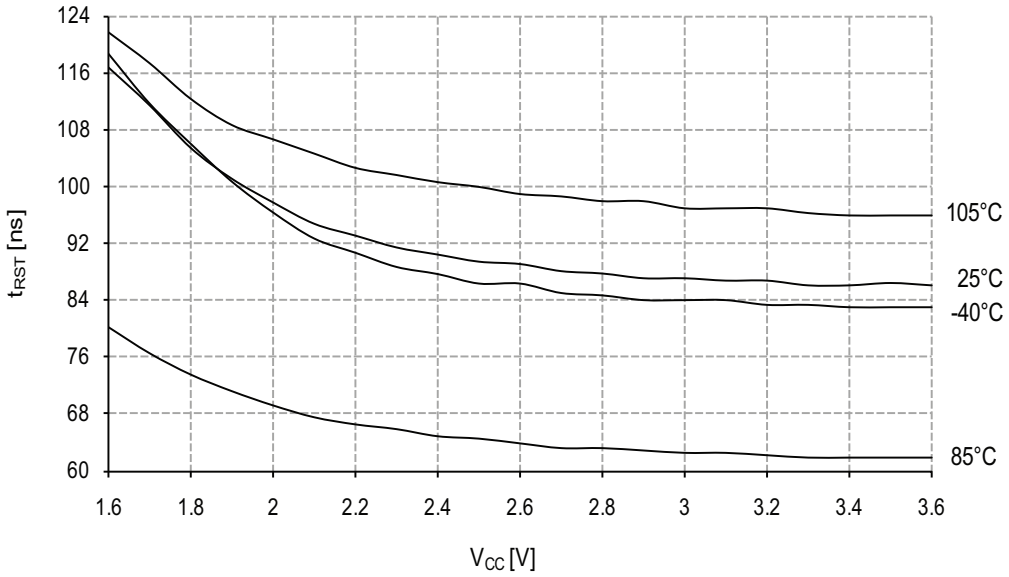


Figure 38-144.Reset pin pull-up resistor current vs. reset pin voltage.
V_{CC} = 1.8V.

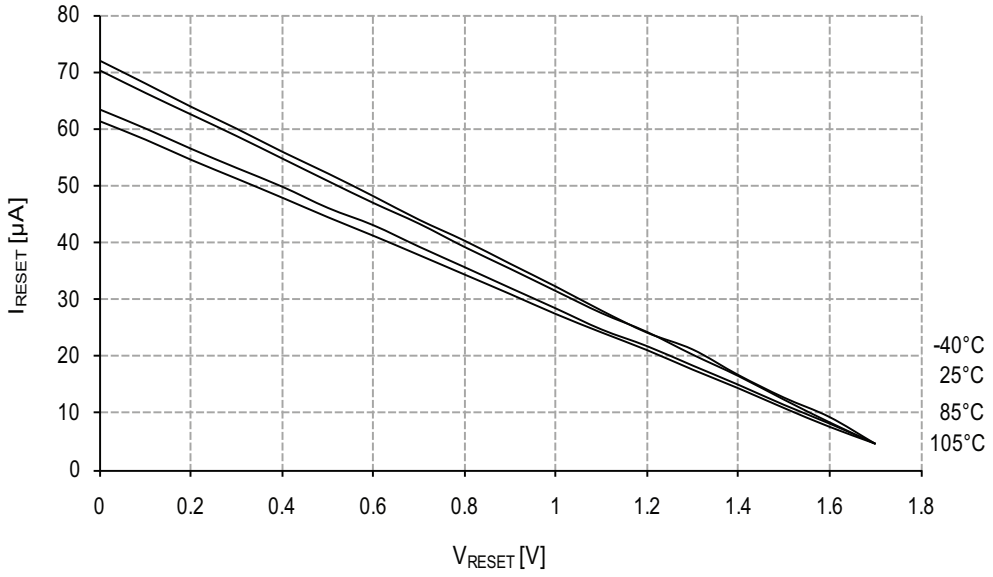


Figure 38-147.Reset pin input threshold voltage vs. V_{CC}.

V_{IH} - Reset pin read as "1".

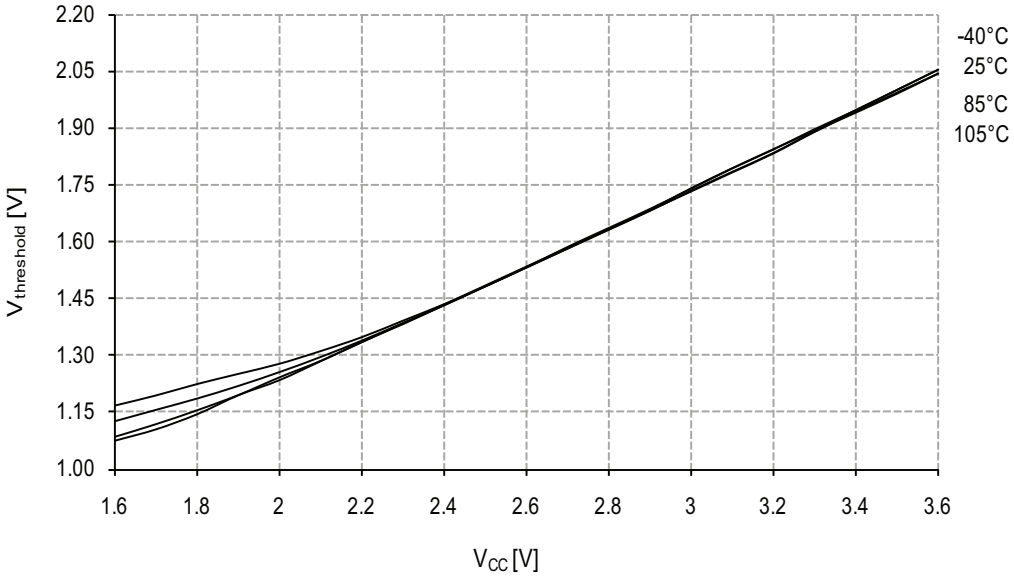
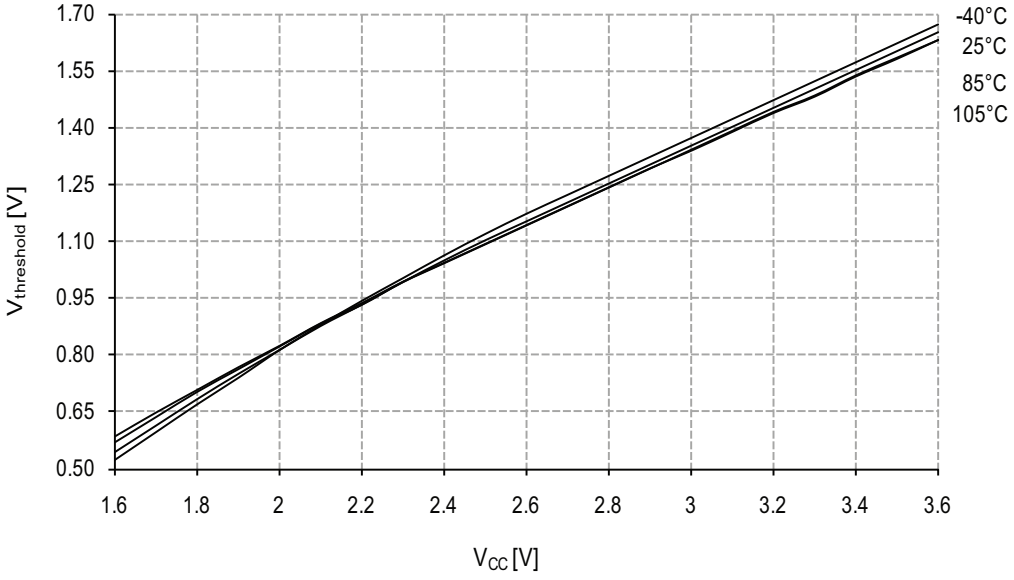


Figure 38-148.Reset pin input threshold voltage vs. V_{CC}.

V_{IL} - Reset pin read as "0".



39. Errata

39.1 ATxmega64A1U

39.1.1 Rev. L

- Register ANAINIT in MCUR will always read as zero
- Enabling DFLL with illegal reference oscillator will lock the DFLL
- XOSCPWR configuration is non-functional
- Configuration of PGM and CWCM is not as described in XMEGA AU Manual
- AWEX PWM output after fault restarted with wrong values
- RTC Counter value not correctly read after sleep
- RTC clock output option is non-functional
- USB, when receiving 1023 byte length isochronous frame, it will corrupt 1024th SRAM location
- USB endpoint table is 16-byte alignment
- USB Auto ZLP feature is non-functional
- Disabling the USART transmitter does not automatically set the TxD pin direction to input
- TWI, SDAHOLD configuration in the TWI CTRL register is one bit
- ADC has increased INL error in when used in SE unsigned mode at low temperatures
- ADC is non-functional in SE unsigned mode with VREF below 1.8V
- ADC has increased linearity error when using the gain stage above 500ksps
- DAC Offset calibration range too small when using AVCC as reference
- DAC clock noise
- Internal 1V reference has noise at low temperature

1 Register ANAINIT in MCUR will always read as zero

The ANAINIT register in the MCUR module will always be read as zero even if written to a value. The actual content of the register is correct.

Problem fix/Workaround

Do not use software that reads these registers to get the Analog Initialization configuration.

2. Enabling DFLL with illegal reference oscillator will lock the clock system

If external crystal is selected as reference for DFLL, but no crystal is connected and DFLL is enabled, the DFLL will be locked until reset is issued.

Problem fix/Workaround

Do not enable DFLL before reference clock is present, enabled and ready.

3. XOSCPWR configuration is non-functional

The Crystal oscillator drive (XOSCPWR) option in the XOSC Control register is non-functional.

Problem fix/Workaround

None.

4. **Configuration of PGM and CWCM is not as described in XMEGA AU Manual**

Configuration of common waveform channel mode (CWCM) and pattern generation mode (PGM), is not as described in the XMEGA AU manual.

Problem fix/Workaround

Configure PWM and CWCM according to the Table 39-1 on page 203.

Table 39-1. PWM and CWCM configuration.

PGM	CWCM	Description
0	0	PGM and CWCM disabled
0	1	PGM enabled
1	0	PGM and CWCM enabled
1	1	PGM enabled

5. **AWEX PWM output after fault restarted with wrong values**

When recovering from fault state, the PWM output will drive wrong values to the port for up to two CLK_{PER} + one CLK_{PER4} cycles.

Problem fix/Workaround

The following seqence can be used in Latched Mode:

a. Disable DTI outputs (Write DTICCxEN to 0)
b. Clear fault flag
c. Wait for Overflow
d. Re-enable DTI (Write DTICCxEN to 1)
e. Set pin direction to Output

This will remove the glitch, but the following period will be shorter. In Cycle-by-cycle mode the same procedure can be followed as long as the Pattern Generation Mode is not enabled.

For Pattern generation mode, there is no workaround.

6. **RTC Counter value not correctly read after sleep**

If a real time counter (RTC) interrupt is used wake up the device from sleep, and bit 0 of RTC count register (CNT) has the same value as when the device entered sleep, CNT will not be read correctly during the first prescaled RTC clock cycle after wakeup. The value read will be the same as the value in the register was when entering sleep.

Problem fix/Workaround

Wait at least one prescaled RTC clock cycle before reading CNT.

7. **RTC clock output option is non-functional**

The real time counter (RTC) as clock output option is non-functional, and setting the RTCOUT bit in the clock and event out register (CLKEVOUT) will have no effect.

Problem fix/Workaround

None

7.	Added electrical characterization for “ATxmega64A1U” on page 74.
8.	Updated Table 37-29 on page 89 and Table 37-63 on page 112. Added ESR and start-up time parameters.
9.	Added typical characteristics for “ATxmega64A1U” on page 120.

40.6 8385D – 07/2012

1.	Updated Table 7-2 on page 15. Devices are respectively ATxmega64A1U and ATxmega128A1U.

40.7 8385C – 07/2012

1.	Updated Table 7-1 on page 13. Device ID for ATxmega128A1U is 4C97. Device ID for ATxmega64A1U is 4E96.
2.	Updated the package “100C2” on page 73. The ball rows are A-K (without I).
3.	Updated the whole datasheet using the Atmel new updated datasheet template that includes Atmel new logo and new registered TM.

40.8 8385B – 03/2012

1.	Added “Electrical Characteristics” on page 74.
2.	Added “Typical Characteristics” on page 120.
3.	Updated “Errata” on page 202.
4.	Used Atmel new datasheet template that includes Atmel new addresses on the last page.

40.9 8385A – 11/2011

1.	Initial revision.