**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

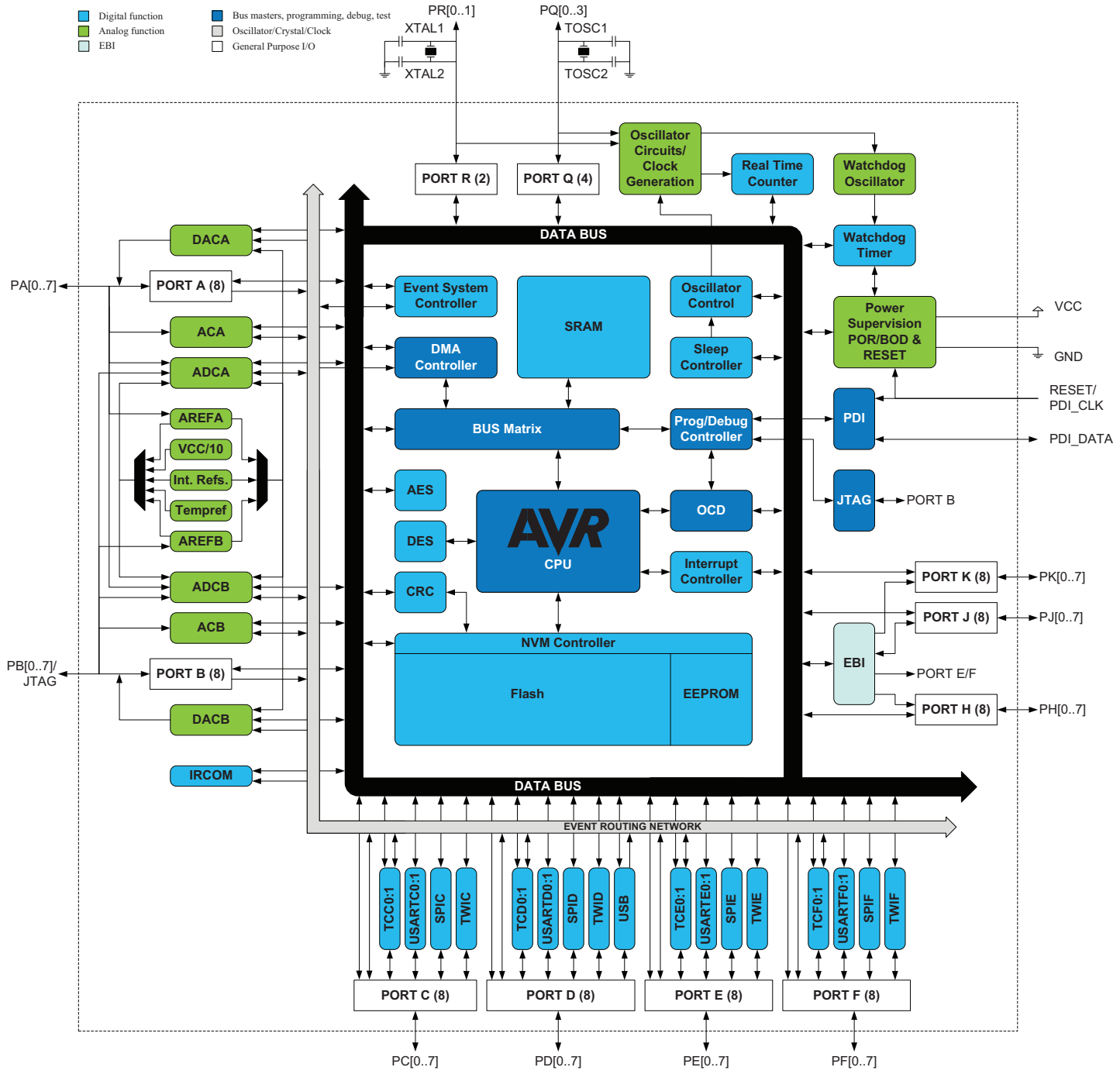
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | AVR |
| Core Size | 8/16-Bit |
| Speed | 32MHz |
| Connectivity | EBI/EMI, I²C, IrDA, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 78 |
| Program Memory Size | 64KB (32K x 16) |
| Program Memory Type | FLASH |
| EEPROM Size | 2K x 8 |
| RAM Size | 4K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.6V ~ 3.6V |
| Data Converters | A/D 16x12b; D/A 4x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-VFBGA |
| Supplier Device Package | 100-VFBGA (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/atxmega64a1u-c7ur |

## 3.1 Block Diagram

**Figure 3-1. XMEGA A1U Block Diagram.**



The available memory size configurations are shown in “Ordering Information” on page 2. In addition each device has a flash memory signature rows for calibration data, device identification, serial number etc.

## 7.3 Flash Program Memory

The Atmel AVR XMEGA devices contain on-chip, in-system reprogrammable flash memory for program storage. The flash memory can be accessed for read and write from an external programmer through the PDI or from application software running in the device.

All AVR CPU instructions are 16 or 32 bits wide, and each flash location is 16 bits wide. The flash memory is organized in two main sections, the application section and the boot loader section. The sizes of the different sections are fixed, but device-dependent. These two sections have separate lock bits, and can have different levels of protection. The store program memory (SPM) instruction, which is used to write to the flash from the application software, will only operate when executed from the boot loader section.

The application section contains an application table section with separate lock settings. This enables safe storage of nonvolatile data in the program memory.

**Figure 7-1. Flash program memory (Hexadecimal address).**

| Word Address | | | |
|---|---|---|---|
| **ATxmega128A1U** | | **ATxmega64A1U** | |
| 0 | | 0 | Application Section (bytes) (128K/64K) |
| | | | |
| | | | ... |
| EFFF | / | 77FF | |
| F000 | / | 7800 | Application Table Section (bytes) (8K/4K) |
| FFFF | / | 7FFF | |
| 10000 | / | 8000 | Boot Section (bytes) (8K/4K) |
| 10FFF | / | 87FF | |

### 7.3.1 Application Section

The Application section is the section of the flash that is used for storing the executable application code. The protection level for the application section can be selected by the boot lock bits for this section. The application section can not store any boot loader code since the SPM instruction cannot be executed from the application section.

### 7.3.2 Application Table Section

The application table section is a part of the application section of the flash memory that can be used for storing data. The size is identical to the boot loader section. The protection level for the application table section can be selected by the boot lock bits for this section. The possibilities for different protection levels on the application section and the application table section enable safe parameter storage in the program memory. If this section is not used for data, application code can reside here.

### 7.3.3 Boot Loader Section

While the application section is used for storing the application code, the boot loader software must be located in the boot loader section because the SPM instruction can only initiate programming when executing from this section. The SPM instruction can access the entire flash, including the boot loader section itself. The protection level for the boot loader section can be selected by the boot loader lock bits. If this section is not used for boot loader software, application code can be stored here.

# 13. WDT – Watchdog Timer

## 13.1 Features

- Issues a device reset if the timer is not reset before its timeout period
- Asynchronous operation from dedicated oscillator
- 1kHz output of the 32kHz ultra low power oscillator
- 11 selectable timeout periods, from 8ms to 8s
- Two operation modes:
  - Normal mode
  - Window mode
- Configuration lock to prevent unwanted changes

## 13.2 Overview

The watchdog timer (WDT) is a system function for monitoring correct program operation. It makes it possible to recover from error situations such as runaway or deadlocked code. The WDT is a timer, configured to a predefined timeout period, and is constantly running when enabled. If the WDT is not reset within the timeout period, it will issue a microcontroller reset. The WDT is reset by executing the WDR (watchdog timer reset) instruction from the application code.

The window mode makes it possible to define a time slot or window inside the total timeout period during which WDT must be reset. If the WDT is reset outside this window, either too early or too late, a system reset will be issued. Compared to the normal mode, this can also catch situations where a code error causes constant WDR execution.

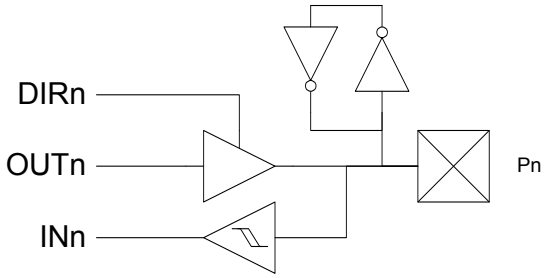
The WDT will run in active mode and all sleep modes, if enabled. It is asynchronous, runs from a CPU-independent clock source, and will continue to operate to issue a system reset even if the main clocks fail.

The configuration change protection mechanism ensures that the WDT settings cannot be changed by accident. For increased safety, a fuse for locking the WDT settings is also available.

### 15.3.4 Bus-keeper

The bus-keeper's weak output produces the same logical level as the last output level. It acts as a pull-up if the last level was '1', and pull-down if the last level was '0'.

**Figure 15-4. I/O configuration - Totem-pole with bus-keeper.**




### 15.3.5 Others

**Figure 15-5. Output configuration - Wired-OR with optional pull-down.**

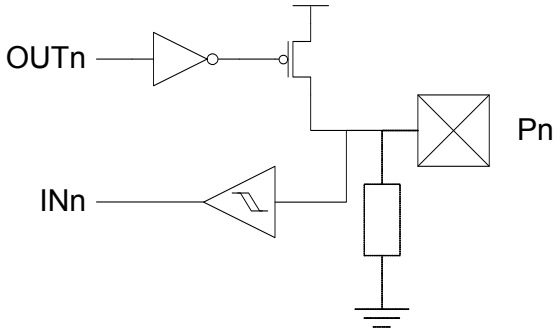
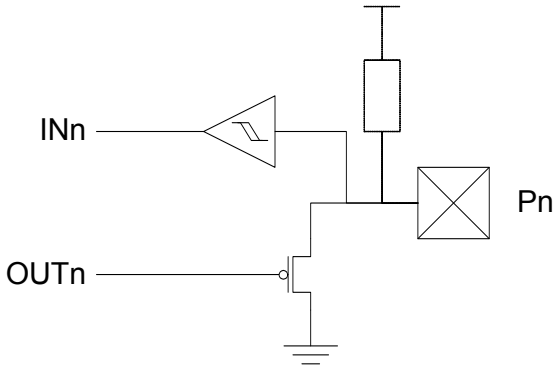



**Figure 15-6. I/O configuration - Wired-AND with optional pull-up.**



# 18. AWeX – Advanced Waveform Extension

## 18.1 Features

- Waveform output with complementary output from each compare channel
- Four dead-time insertion (DTI) units
  - 8-bit resolution
  - Separate high and low side dead-time setting
  - Double buffered dead time
  - Optionally halts timer during dead-time insertion
- Pattern generation unit creating synchronised bit pattern across the port pins
  - Double buffered pattern generation
  - Optional distribution of one compare channel output across the port pins
- Event controlled fault protection for instant and predictable fault triggering

## 18.2 Overview

The advanced waveform extension (AWeX) provides extra functions to the timer/counter in waveform generation (WG) modes. It is primarily intended for use with different types of motor control and other power control applications. It enables low- and high side output with dead-time insertion and fault protection for disabling and shutting down external drivers. It can also generate a synchronized bit pattern across the port pins.

Each of the waveform generator outputs from the Timer/Counter 0 are split into a complimentary pair of outputs when any AWeX features are enabled. These output pairs go through a dead-time insertion (DTI) unit that generates the non-inverted low side (LS) and inverted high side (HS) of the WG output with dead-time insertion between LS and HS switching. The DTI output will override the normal port value according to the port override setting.

The pattern generation unit can be used to generate a synchronized bit pattern on the port it is connected to. In addition, the WG output from compare channel A can be distributed to and override all the port pins. When the pattern generator unit is enabled, the DTI unit is bypassed.

The fault protection unit is connected to the event system, enabling any event to trigger a fault condition that will disable the AWeX output. The event system ensures predictable and instant fault reaction, and gives great flexibility in the selection of fault triggers.

The AWeX is available for TCC0 and TCE0. The notation of these are AWEXC and AWEXE.

# 21. USB – Universal Serial Bus Interface

## 21.1 Features

- One USB 2.0 full speed (12Mbps) and low speed (1.5Mbps) device compliant interface
- Integrated on-chip USB transceiver, no external components needed
- 16 endpoint addresses with full endpoint flexibility for up to 31 endpoints
  - One input endpoint per endpoint address
  - One output endpoint per endpoint address
- Endpoint address transfer type selectable to
  - Control transfers
  - Interrupt transfers
  - Bulk transfers
  - Isochronous transfers
- Configurable data payload size per endpoint, up to 1023 bytes
- Endpoint configuration and data buffers located in internal SRAM
  - Configurable location for endpoint configuration data
  - Configurable location for each endpoint's data buffer
- Built-in direct memory access (DMA) to internal SRAM for:
  - Endpoint configurations
  - Reading and writing endpoint data
- Ping-pong operation for higher throughput and double buffered operation
  - Input and output endpoint data buffers used in a single direction
  - CPU/DMA controller can update data buffer during transfer
- Multi packet transfer for reduced interrupt load and software intervention
  - Data payload exceeding maximum packet size is transferred in one continuous transfer
  - No interrupts or software interaction on packet transaction level
- Transaction complete FIFO for workflow management when using multiple endpoints
  - Tracks all completed transactions in a first-come, first-served work queue
- Clock selection independent of system clock source and selection
- Minimum 1.5MHz CPU clock required for low speed USB operation
- Minimum 12MHz CPU clock required for full speed operation
- Connection to event system
- On chip debug possibilities during USB transactions

## 21.2 Overview

The USB module is a USB 2.0 full speed (12Mbps) and low speed (1.5Mbps) device compliant interface.

The USB supports 16 endpoint addresses. All endpoint addresses have one input and one output endpoint, for a total of 31 configurable endpoints and one control endpoint. Each endpoint address is fully configurable and can be configured for any of the four transfer types; control, interrupt, bulk, or isochronous. The data payload size is also selectable, and it supports data payloads up to 1023 bytes.

No dedicated memory is allocated for or included in the USB module. Internal SRAM is used to keep the configuration for each endpoint address and the data buffer for each endpoint. The memory locations used for endpoint configurations and data buffers are fully configurable. The amount of memory allocated is fully dynamic, according to the number of endpoints in use and the configuration of these. The USB module has built-in direct memory access (DMA), and will read/write data from/to the SRAM when a USB transaction takes place.

To maximize throughput, an endpoint address can be configured for ping-pong operation. When done, the input and output endpoints are both used in the same direction. The CPU or DMA controller can then read/write one data buffer while the USB module writes/reads the others, and vice versa. This gives double buffered communication.

# 25. IRCOM – IR Communication Module

## 25.1 Features

- Pulse modulation/demodulation for infrared communication
- IrDA compatible for baud rates up to 115.2Kbps
- Selectable pulse modulation scheme
  - 3/16 of the baud rate period
  - Fixed pulse period, 8-bit programmable
  - Pulse modulation disabled
- Built-in filtering
- Can be connected to and used by any USART

## 25.2 Overview

Atmel AVR XMEGA devices contain an infrared communication module (IRCOM) that is IrDA compatible for baud rates up to 115.2Kbps. It can be connected to any USART to enable infrared pulse encoding/decoding for that USART.

# 29. ADC – 12-bit Analog to Digital Converter

## 29.1 Features

- Two Analog to Digital Converters
- 12-bit resolution
- Up to two million samples per second
  - Two inputs can be sampled simultaneously using ADC and 1x gain stage
  - Four inputs can be sampled within 1.5µs
  - Down to 2.5µs conversion time with 8-bit resolution
  - Down to 3.5µs conversion time with 12-bit resolution
- Differential and single-ended input
  - Up to 16 single-ended inputs
  - 16x4 differential inputs without gain
  - 8x4 differential input with gain
- Built-in differential gain stage
  - 1/2x, 1x, 2x, 4x, 8x, 16x, 32x, and 64x gain options
- Single, continuous and scan conversion options
- Four internal inputs
  - Internal temperature sensor
  - DAC output
  - $AV_{CC}$ voltage divided by 10
  - 1.1V bandgap voltage
- Four conversion channels with individual input control and result registers
  - Enable four parallel configurations and results
- Internal and external reference options
- Compare function for accurate monitoring of user defined thresholds
- Optional event triggered conversion for accurate timing
- Optional DMA transfer of conversion results
- Optional interrupt/event on compare result

## 29.2 Overview

The ADC converts analog signals to digital values. There are two Analog to Digital Converters (ADCs) modules that can be operated simultaneously, individually or synchronized.

The ADC has 12-bit resolution and is capable of converting up to two million samples per second (msps). The input selection is flexible, and both single-ended and differential measurements can be done. For differential measurements, an optional gain stage is available to increase the dynamic range. In addition, several internal signal inputs are available. The ADC can provide both signed and unsigned results.

This is a pipelined ADC that consists of several consecutive stages. The pipelined design allows a high sample rate at a low system clock frequency. It also means that a new input can be sampled and a new ADC conversion started while other ADC conversions are still ongoing. This removes dependencies between sample rate and propagation delay.

The ADC has four conversion channels (0-3) with individual input selection, result registers, and conversion start control. The ADC can then keep and use four parallel configurations and results, and this will ease use for applications with high data throughput or for multiple modules using the ADC independently. It is possible to use DMA to move ADC results directly to memory or peripherals when conversions are done.

Both internal and external reference voltages can be used. An integrated temperature sensor is available for use with the ADC. The output from the DAC, $AV_{CC}/10$ and the bandgap voltage can also be measured by the ADC.

The ADC has a compare function for accurate monitoring of user defined thresholds with minimum software intervention required.

# 30. DAC – 12-bit Digital to Analog Converter

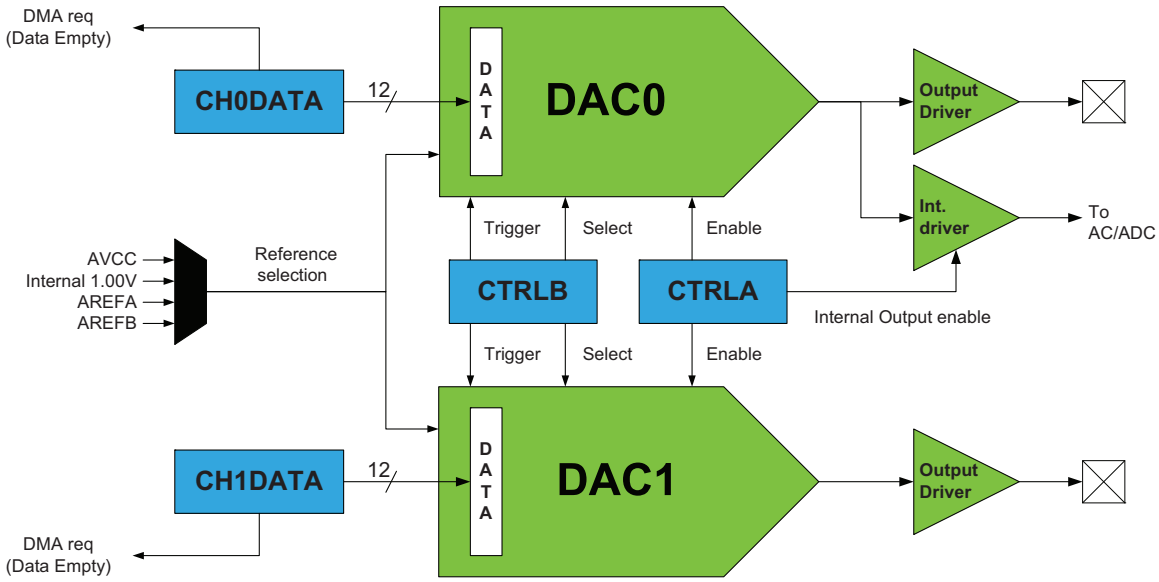
## 30.1 Features

- Two digital to analog converters (DACs)
- 12-bit resolution
- Two independent, continuous-drive output channels
- Up to one million samples per second conversion rate per DAC channel
- Built-in calibration that removes:
  - Offset error
  - Gain error
- Multiple conversion trigger sources
  - On new available data
  - Events from the event system
- High drive capabilities and support for
  - Resistive loads
  - Capacitive loads
  - Combined resistive and capacitive loads
- Internal and external reference options
- DAC output available as input to analog comparator and ADC
- Low-power mode, with reduced drive strength
- Optional DMA transfer of data

## 30.2 Overview

The digital-to-analog converter (DAC) converts digital values to voltages. The DAC has two channels, each with12-bit resolution, and is capable of converting up to one million samples per second (msps) on each channel. The built-in calibration system can remove offset and gain error when loaded with calibration values from software.

**Figure 30-1. DAC overview.**



### 33.1.5 Timer/Counter and AWEX functions

| | |
|---|---|
| OCnxLS | Output Compare Channel x Low Side for Timer/Counter n |
| OCnxHS | Output Compare Channel x High Side for Timer/Counter n |

### 33.1.6 Communication functions

| | |
|---|---|
| SCL | Serial Clock for TWI |
| SDA | Serial Data for TWI |
| SCLIN | Serial Clock In for TWI when external driver interface is enabled |
| SCLOUT | Serial Clock Out for TWI when external driver interface is enabled |
| SDAIN | Serial Data In for TWI when external driver interface is enabled |
| SDAOUT | Serial Data Out for TWI when external driver interface is enabled |
| XCKn | Transfer Clock for USART n |
| RXDn | Receiver Data for USART n |
| TXDn | Transmitter Data for USART n |
| $\overline{SS}$ | Slave Select for SPI |
| MOSI | Master Out Slave In for SPI |
| MISO | Master In Slave Out for SPI |
| SCK | Serial Clock for SPI |
| D- | Data- for USB |
| D+ | Data+ for USB |

### 33.1.7 Oscillators, Clock and Event

| | |
|---|---|
| TOSCn | Timer Oscillator pin n |
| XTALn | Input/Output for Oscillator pin n |
| CLKOUT | Peripheral Clock Output |
| EVOUT | Event Channel 0 Output |

### 33.1.8 Debug/System functions

| | |
|---|---|
| $\overline{RESET}$ | Reset pin |
| PDI_CLK | Program and Debug Interface Clock pin |
| PDI_DATA | Program and Debug Interface Data pin |
| TCK | JTAG Test Clock |
| TDI | JTAG Test Data In |
| TDO | JTAG Test Data Out |
| TMS | JTAG Test Mode Select |

| PORT E | PIN # | INTERRUPT | TCE0 | AWEXE | TCE1 | USARTE0 | USARTE1 | SPIE | TWIE | CLOCKOUT | EVENTOUT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **PE2** | 37 | SYNC/ASYNC | OC0C | $\overline{\text{OC0BLS}}$ | | RXD0 | | | | | |
| **PE3** | 38 | SYNC | OC0D | OC0BHS | | TXD0 | | | | | |
| **PE4** | 39 | SYNC | | $\overline{\text{OC0CLS}}$ | OC1A | | | $\overline{\text{SS}}$ | | | |
| **PE5** | 40 | SYNC | | OC0CHS | OC1B | | XCK1 | MOSI | | | |
| **PE6** | 41 | SYNC | | $\overline{\text{OC0DLS}}$ | | | RXD1 | MISO | | | |
| **PE7** | 42 | SYNC | | OC0DHS | | | TXD1 | SCK | | $clk_{PER}$ | EVOUT |

Notes: 1. All pins on the port can optionally be used for EBI chip select or address lines. Refer to the EBIOUT register description in the XMEGA AU Manual.

**Table 33-6. Port F - alternate functions.**

| PORT F | PIN # | INTERRUPT | TCF0 | TCF1 | USARTF0 | USARTF1 | SPIF | TWIF |
|---|---|---|---|---|---|---|---|---|
| **GND** | 43 | | | | | | | |
| **VCC** | 44 | | | | | | | |
| **PF0** | 45 | SYNC | OC0A | | | | | SDA |
| **PF1** | 46 | SYNC | OC0B | | XCK0 | | | SCL |
| **PF2** | 47 | SYNC/ASYNC | OC0C | | RXD0 | | | |
| **PF3** | 48 | SYNC | OC0D | | TXD0 | | | |
| **PF4** | 49 | SYNC | | OC1A | | | $\overline{\text{SS}}$ | |
| **PF5** | 50 | SYNC | | OC1B | | XCK1 | MOSI | |
| **PF6** | 51 | SYNC | | | | RXD1 | MISO | |
| **PF7** | 52 | SYNC | | | | TXD1 | SCK | |

Note: 1. All pins on the port can optionally be used for EBI chip select or address lines. Refer to the EBIOUT register description in the XMEGA AU Manual.

**Table 33-7. Port H - alternate functions.**

| PORT H | PIN # | INTERRUPT | SDRAM 3P | SRAM ALE1 | SRAM ALE12 | LPC3 ALE1 | LPC2 ALE1 | LPC2 ALE12 |
|---|---|---|---|---|---|---|---|---|
| **GND** | 53 | | | | | | | |
| **VCC** | 54 | | | | | | | |
| **PH0** | 55 | SYNC | $\overline{\text{WE}}$ | $\overline{\text{WE}}$ | $\overline{\text{WE}}$ | $\overline{\text{WE}}$ | $\overline{\text{WE}}$ | $\overline{\text{WE}}$ |
| **PH1** | 56 | SYNC | $\overline{\text{CAS}}$ | $\overline{\text{RE}}$ | $\overline{\text{RE}}$ | $\overline{\text{RE}}$ | $\overline{\text{RE}}$ | $\overline{\text{RE}}$ |
| **PH2** | 57 | SYNC/ASYNC | $\overline{\text{RAS}}$ | $\overline{\text{ALE1}}$ | $\overline{\text{ALE1}}$ | $\overline{\text{ALE1}}$ | $\overline{\text{ALE1}}$ | $\overline{\text{ALE1}}$ |
| **PH3** | 58 | SYNC | $\overline{\text{DQM}}$ | | $\overline{\text{ALE2}}$ | | | $\overline{\text{ALE2}}$ |
| **PH4** | 59 | SYNC | BA0 | $\overline{\text{CS0}}$/A16 | $\overline{\text{CS0}}$ | $\overline{\text{CS0}}$/A16 | $\overline{\text{CS0}}$ | $\overline{\text{CS0}}$/A16 |
| **PH5** | 60 | SYNC | BA1 | $\overline{\text{CS1}}$/A17 | $\overline{\text{CS1}}$ | $\overline{\text{CS1}}$/A17 | $\overline{\text{CS1}}$ | $\overline{\text{CS1}}$/A17 |
| **PH6** | 61 | SYNC | CKE | $\overline{\text{CS2}}$/A18 | $\overline{\text{CS2}}$ | $\overline{\text{CS2}}$/A18 | $\overline{\text{CS2}}$ | $\overline{\text{CS2}}$/A18 |
| **PH7** | 62 | SYNC | CLK | $\overline{\text{CS3}}$/A19 | $\overline{\text{CS3}}$ | $\overline{\text{CS3}}$/A19 | $\overline{\text{CS3}}$ | $\overline{\text{CS3}}$/A19 |

Notes: 1. CS0 - CS3 can optionally be moved to Port E or F
2. A16-A23 can optionally be moved to Port E or F when EBI configured in 4PORT mode. Refer to the EBIOUT register description in the XMEGA AU Manual.

# 35. Instruction Set Summary

| Mnemonics | Operands | Description | Operation | Flags | #Clocks |
|---|---|---|---|---|---|
| **Arithmetic and Logic Instructions** | | | | | |
| ADD | Rd, Rr | Add without Carry | Rd ← Rd + Rr | Z,C,N,V,S,H | 1 |
| ADC | Rd, Rr | Add with Carry | Rd ← Rd + Rr + C | Z,C,N,V,S,H | 1 |
| ADIW | Rd, K | Add Immediate to Word | Rd ← Rd + 1:Rd + K | Z,C,N,V,S | 2 |
| SUB | Rd, Rr | Subtract without Carry | Rd ← Rd - Rr | Z,C,N,V,S,H | 1 |
| SUBI | Rd, K | Subtract Immediate | Rd ← Rd - K | Z,C,N,V,S,H | 1 |
| SBC | Rd, Rr | Subtract with Carry | Rd ← Rd - Rr - C | Z,C,N,V,S,H | 1 |
| SBCI | Rd, K | Subtract Immediate with Carry | Rd ← Rd - K - C | Z,C,N,V,S,H | 1 |
| SBIW | Rd, K | Subtract Immediate from Word | Rd + 1:Rd ← Rd + 1:Rd - K | Z,C,N,V,S | 2 |
| AND | Rd, Rr | Logical AND | Rd ← Rd • Rr | Z,N,V,S | 1 |
| ANDI | Rd, K | Logical AND with Immediate | Rd ← Rd • K | Z,N,V,S | 1 |
| OR | Rd, Rr | Logical OR | Rd ← Rd v Rr | Z,N,V,S | 1 |
| ORI | Rd, K | Logical OR with Immediate | Rd ← Rd v K | Z,N,V,S | 1 |
| EOR | Rd, Rr | Exclusive OR | Rd ← Rd ⊕ Rr | Z,N,V,S | 1 |
| COM | Rd | One's Complement | Rd ← $FF - Rd | Z,C,N,V,S | 1 |
| NEG | Rd | Two's Complement | Rd ← $00 - Rd | Z,C,N,V,S,H | 1 |
| SBR | Rd,K | Set Bit(s) in Register | Rd ← Rd v K | Z,N,V,S | 1 |
| CBR | Rd,K | Clear Bit(s) in Register | Rd ← Rd • ($FFh - K) | Z,N,V,S | 1 |
| INC | Rd | Increment | Rd ← Rd + 1 | Z,N,V,S | 1 |
| DEC | Rd | Decrement | Rd ← Rd - 1 | Z,N,V,S | 1 |
| TST | Rd | Test for Zero or Minus | Rd ← Rd • Rd | Z,N,V,S | 1 |
| CLR | Rd | Clear Register | Rd ← Rd ⊕ Rd | Z,N,V,S | 1 |
| SER | Rd | Set Register | Rd ← $FF | None | 1 |
| MUL | Rd,Rr | Multiply Unsigned | R1:R0 ← Rd x Rr (UU) | Z,C | 2 |
| MULS | Rd,Rr | Multiply Signed | R1:R0 ← Rd x Rr (SS) | Z,C | 2 |
| MULSU | Rd,Rr | Multiply Signed with Unsigned | R1:R0 ← Rd x Rr (SU) | Z,C | 2 |
| FMUL | Rd,Rr | Fractional Multiply Unsigned | R1:R0 ← Rd x Rr<<1 (UU) | Z,C | 2 |
| FMULS | Rd,Rr | Fractional Multiply Signed | R1:R0 ← Rd x Rr<<1 (SS) | Z,C | 2 |
| FMULSU | Rd,Rr | Fractional Multiply Signed with Unsigned | R1:R0 ← Rd x Rr<<1 (SU) | Z,C | 2 |
| DES | K | Data Encryption | if (H = 0) then R15:R0 ← Encrypt(R15:R0, K)<br>else if (H = 1) then R15:R0 ← Decrypt(R15:R0, K) | | 1/2 |
| **Branch instructions** | | | | | |
| RJMP | k | Relative Jump | PC ← PC + k + 1 | None | 2 |
| IJMP | | Indirect Jump to (Z) | PC(15:0) ← Z,<br>PC(21:16) ← 0 | None | 2 |
| EIJMP | | Extended Indirect Jump to (Z) | PC(15:0) ← Z,<br>PC(21:16) ← EIND | None | 2 |
| JMP | k | Jump | PC ← k | None | 3 |
| RCALL | k | Relative Call Subroutine | PC ← PC + k + 1 | None | 2 / 3 (1) |

### 37.1.3 Current consumption

**Table 37-4. Current consumption for Active mode and sleep modes.**

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Active power consumption[1] | 32kHz, Ext. Clk | $V_{CC}$ = 1.8V | | 50 | | µA |
| | | | $V_{CC}$ = 3.0V | | 95 | | |
| | | 1MHz, Ext. Clk | $V_{CC}$ = 1.8V | | 350 | | |
| | | | $V_{CC}$ = 3.0V | | 700 | | |
| | | 2MHz, Ext. Clk | $V_{CC}$ = 1.8V | | 650 | 700 | |
| | | | $V_{CC}$ = 3.0V | | 1.2 | 1.4 | mA |
| | | 32MHz, Ext. Clk | | | 15 | 20 | |
| | Idle power consumption[1] | 32kHz, Ext. Clk | $V_{CC}$ = 1.8V | | 3.5 | | µA |
| | | | $V_{CC}$ = 3.0V | | 6.4 | | |
| | | 1MHz, Ext. Clk | $V_{CC}$ = 1.8V | | 109 | | |
| | | | $V_{CC}$ = 3.0V | | 200 | | |
| | | 2MHz, Ext. Clk | $V_{CC}$ = 1.8V | | 290 | 380 | |
| | | | $V_{CC}$ = 3.0V | | 476 | 650 | |
| | | 32MHz, Ext. Clk | | | 6.6 | 9.2 | mA |
| | Power-down power consumption | T = 25°C | $V_{CC}$ = 1.8V | | 0.1 | 1.0 | µA |
| | | T = 25°C | $V_{CC}$ = 3.0V | | 0.1 | 1.0 | |
| | | T = 85°C | | | 1.7 | 5.0 | |
| | | T = 105°C | | | 6.0 | 10 | |
| | | WDT and sampled BOD enabled, T = 25°C | | | 1.3 | 3.0 | |
| | | WDT and sampled BOD enabled, T = 85°C | | | 3.1 | 10 | |
| | | WDT and sampled BOD enabled, T = 105°C | | | 7.0 | 12 | |
| | Power-save power consumption[2] | RTC on ULP clock, WDT and sampled BOD enabled, T = 25°C | $V_{CC}$ = 1.8V | | 1.2 | | |
| | | | $V_{CC}$ = 3.0V | | 1.3 | | |
| | | RTC on 1.024kHz low power 32.768kHz TOSC, T = 25°C | $V_{CC}$ = 1.8V | | 0.7 | 2.0 | |
| | | | $V_{CC}$ = 3.0V | | 0.8 | 2.0 | |
| | | RTC from low power 32.768kHz TOSC, T = 25°C | $V_{CC}$ = 1.8V | | 0.9 | 3.0 | |
| | | | $V_{CC}$ = 3.0V | | 1.0 | 3.0 | |
| | Reset power consumption | Current through $\overline{\text{RESET}}$ pin subtracted | $V_{CC}$ = 3.0V | | 914 | | |

Notes:
1. All Power Reduction Registers set.
2. Maximum limits are based on characterization, and not tested in production.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{CL}$ | Clock Low Time | $V_{CC}$ = 1.6 - 1.8V | 4.5 | | | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | 2.4 | | | |
| $t_{CR}$ | Rise Time (for maximum frequency) | $V_{CC}$ = 1.6 - 1.8V | | | 1.5 | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | | | 1.0 | |
| $t_{CF}$ | Fall Time (for maximum frequency) | $V_{CC}$ = 1.6 - 1.8V | | | 1.5 | ns |
| | | $V_{CC}$ = 2.7 - 3.6V | | | 1.0 | |
| $\Delta t_{CK}$ | Change in period from one clock cycle to the next | | | | 10 | % |

Notes: 1. System Clock Prescalers must be set so that maximum CPU clock frequency for device is not exceeded.
2. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

### 37.1.14.7 External 16MHz crystal oscillator and XOSC characteristics

**Table 37-29. External 16MHz crystal oscillator and XOSC characteristics.**

| Symbol | Parameter | Condition | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| | Cycle to cycle jitter | FRQRANGE=0 | | | <10 | | ns |
| | | FRQRANGE=1, 2, 3 | | | <1 | | |
| | Frequency error | FRQRANGE=0 | | | <0.5 | | % |
| | | FRQRANGE=1 | | | <0.05 | | |
| | | FRQRANGE=2 | | | <0.005 | | |
| | | FRQRANGE=3 | | | <0.005 | | |
| | Duty cycle | FRQRANGE=0 | | | 50 | | |
| | | FRQRANGE=1 | | | 50 | | |
| | | FRQRANGE=2 | | | 50 | | |
| | | FRQRANGE=3 | | | 50 | | |

**Table 37-55. Programming time.**

| Symbol | Parameter | Condition | Min. | Typ. [1] | Max. | Units |
|---|---|---|---|---|---|---|
| | Chip Erase | 128KB Flash, EEPROM[2] and SRAM Erase | | 75 | | ms |
| | Flash | Page Erase | | 4 | | |
| | | Page Write | | 4 | | |
| | | Atomic Page Erase and Write | | 8 | | |
| | EEPROM | Page Erase | | 4 | | |
| | | Page Write | | 4 | | |
| | | Atomic Page Erase and Write | | 8 | | |

Notes: 1. Programming is timed from the 2MHz internal oscillator.
2. EEPROM is not erased if the EESAVE fuse is programmed.

## 37.2.14 Clock and Oscillator Characteristics

### 37.2.14.1 Calibrated 32.768kHz Internal Oscillator characteristics

**Table 37-56. 32.768kHz internal oscillator characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| | Frequency | | | 32.768 | | kHz |
| | Factory calibration accuracy | T = 85°C, $V_{CC}$ = 3.0V | -0.5 | | 0.5 | % |
| | User calibration accuracy | | -0.5 | | 0.5 | |

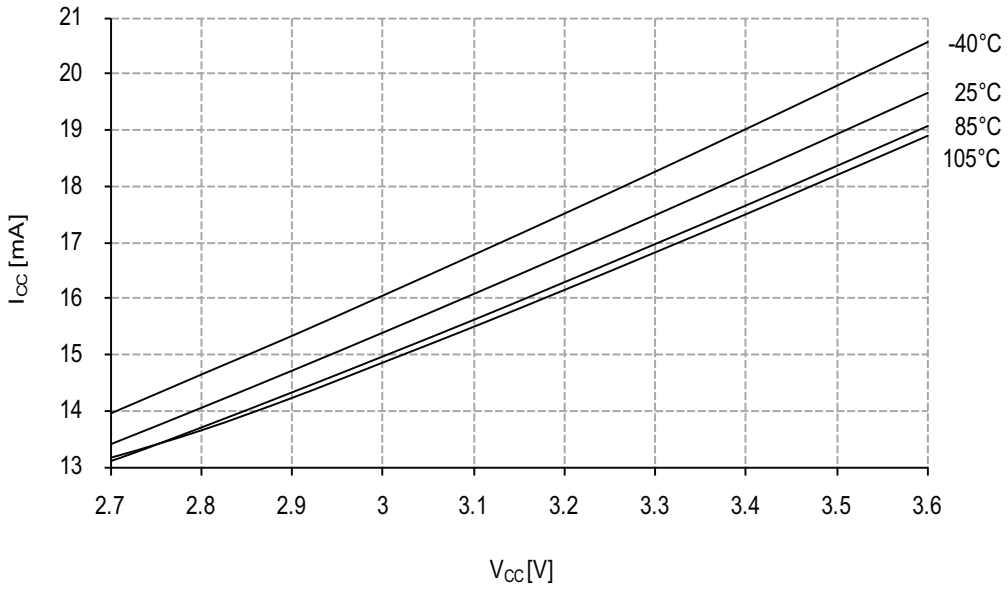
### 37.2.14.2 Calibrated 2MHz RC Internal Oscillator characteristics

**Table 37-57. 2MHz internal oscillator characteristics.**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| | Tunable frequency range | DFLL can tune to this frequency over voltage and temperature | 1.8 | | 2.2 | MHz |
| | Factory calibrated frequency | | | 2.0 | | |
| | Factory calibration accuracy | T = 85°C, $V_{CC}$= 3.0V | -1.5 | | 1.5 | % |
| | DFLL calibration stepsize | T = 25°C, $V_{CC}$= 3.0V | | 0.23 | | |

**Figure 38-7. Active mode supply current vs. $V_{CC}$.**

***$f_{SYS}$ = 32MHz internal oscillator.***




### 38.1.1.2 Idle mode supply current

**Figure 38-8. Idle mode supply current vs. frequency.**

***$f_{SYS}$ = 0 - 1MHz external clock, T = 25°C.***

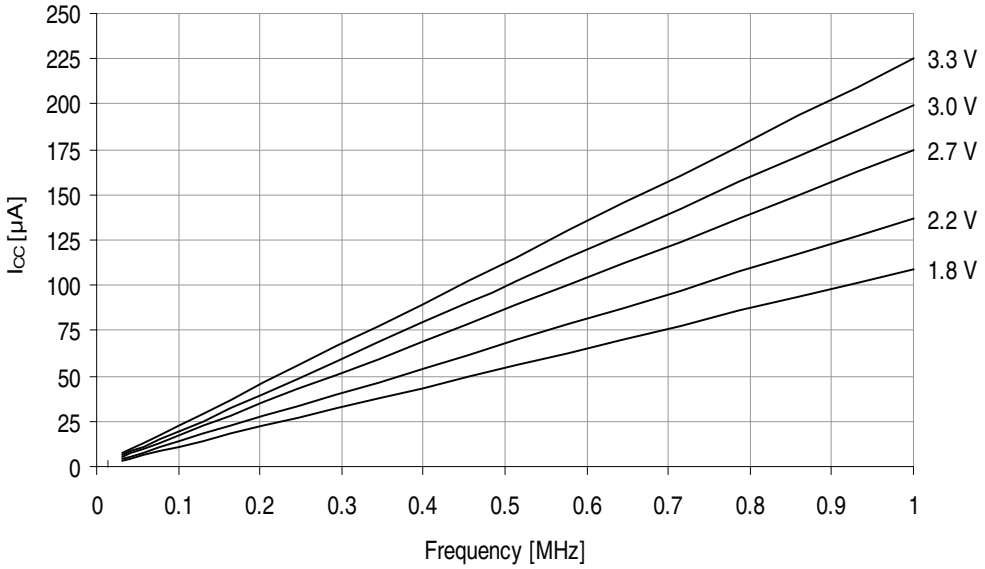


**Figure 38-37.INL error vs. input code**

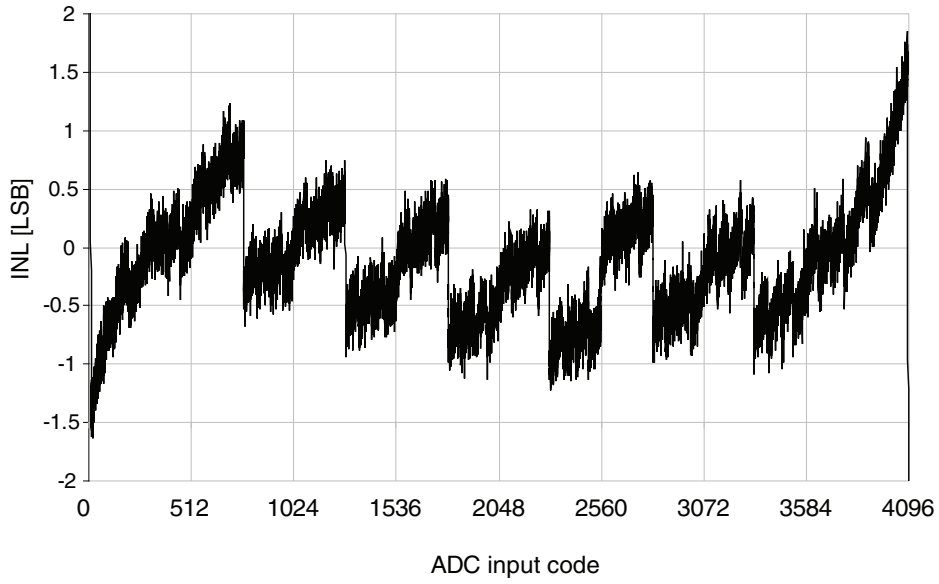
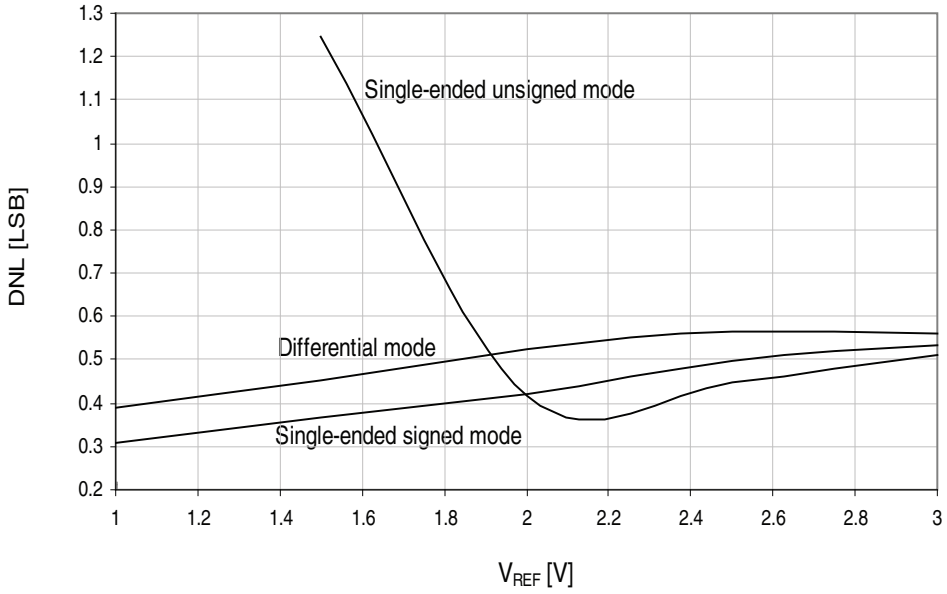



**Figure 38-38.DNL error vs. external $V_{REF}$.**

***T = 25°C, $V_{CC}$ = 3.6V, external reference.***



### 38.1.9 Power-on Reset Characteristics

**Figure 38-67.Power-on reset current consumption vs. $V_{CC}$.**

***BOD level = 3.0V, enabled in continuous mode.***

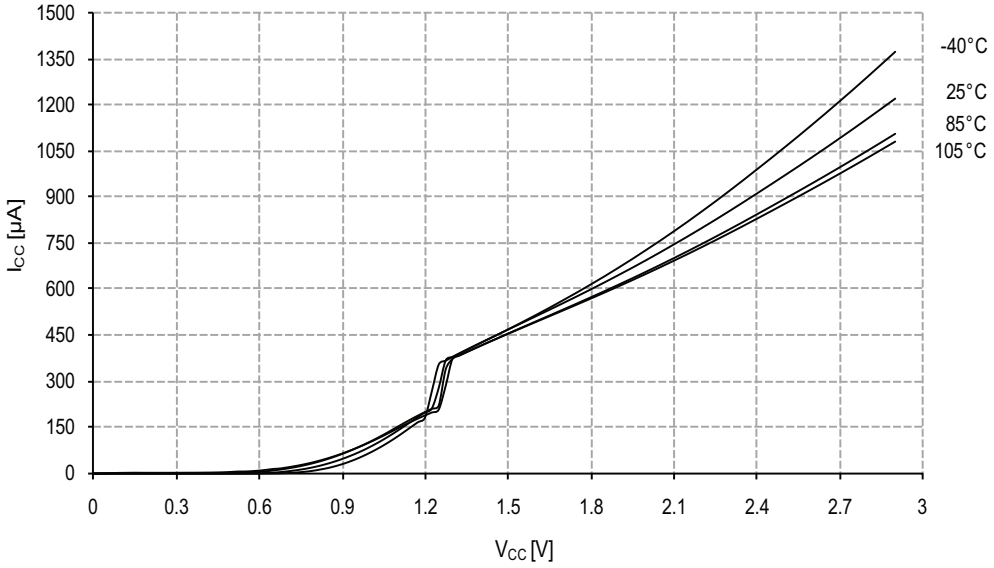



**Figure 38-68.Power-on reset current consumption vs. $V_{CC}$.**

***BOD level = 3.0V, enabled in sampled mode.***

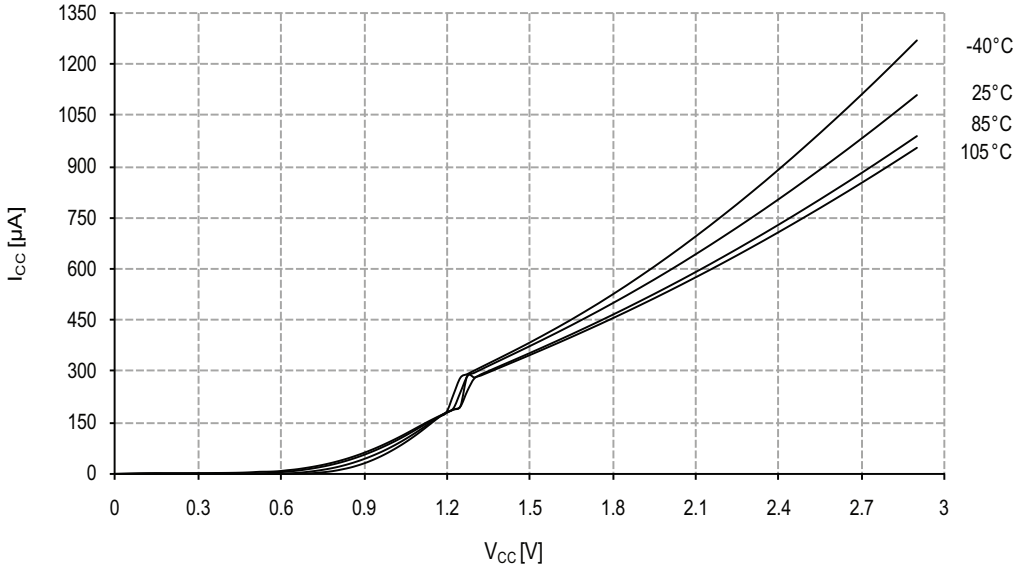


**Figure 38-93.Idle mode supply current vs. $V_{CC}$.**

***$f_{SYS}$ = 1MHz external clock.***

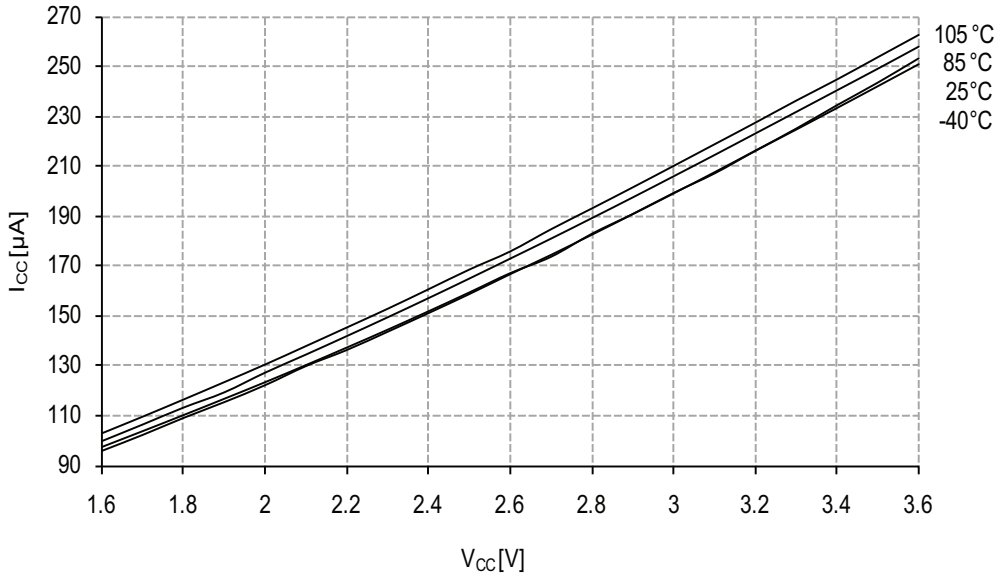
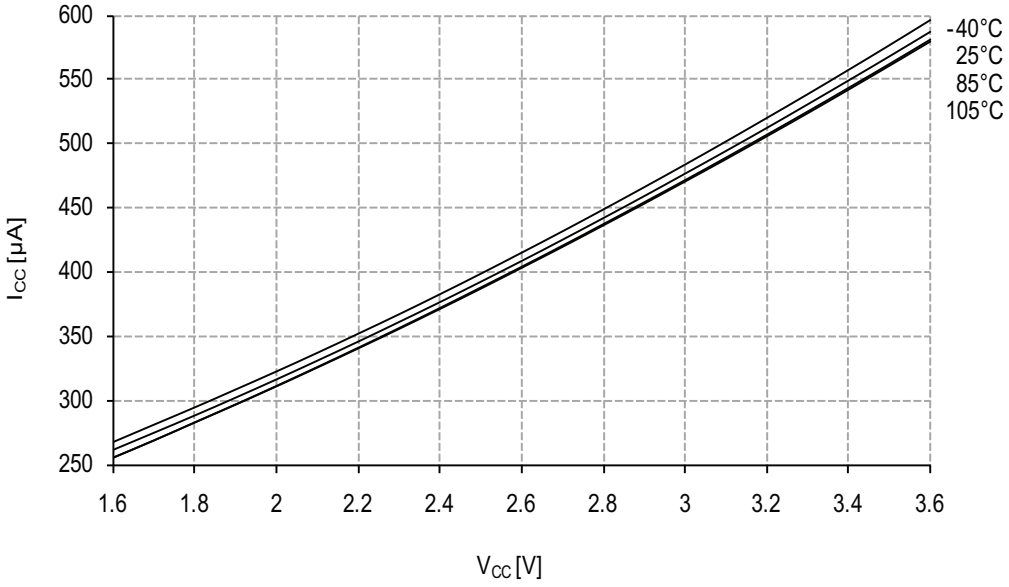



**Figure 38-94.Idle mode supply current vs. $V_{CC}$.**

***$f_{SYS}$ = 2MHz internal oscillator.***



### 38.2.3 ADC Characteristics

**Figure 38-117.INL error vs. external $V_{REF}$.**

***T = 25°C, $V_{CC}$ = 3.6V, external reference.***

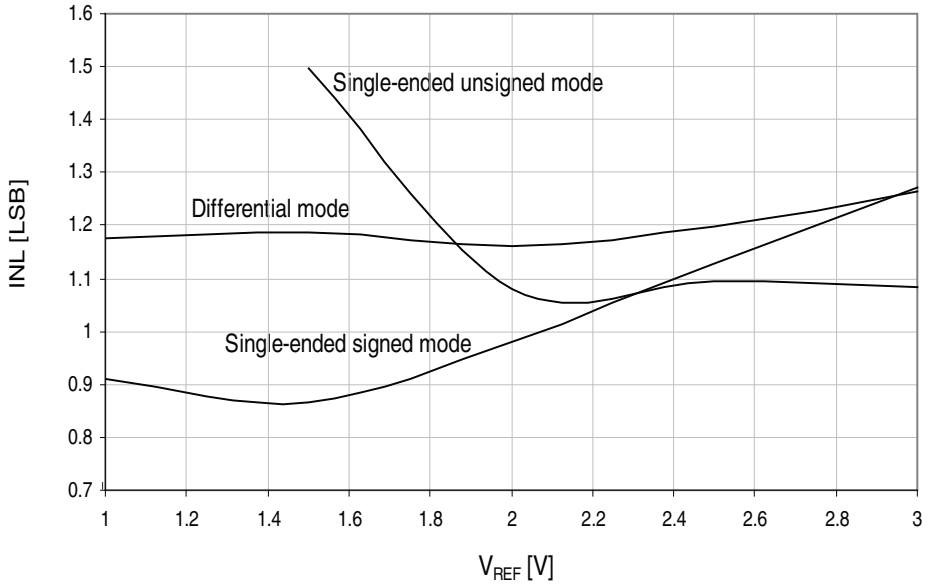



**Figure 38-118.INL error vs. sample rate.**

***T = 25°C, $V_{CC}$ = 3.6V, $V_{REF}$ = 2.0V external.***