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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	EBI/EMI, I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	78
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 16x12b; D/A 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-CBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega64a1u-cur

7.10 Memory Timing

Read and write access to the I/O memory takes one CPU clock cycle. A write to SRAM takes one cycle, and a read from SRAM takes two cycles. For burst read (DMA), new data are available every cycle. EEPROM page load (write) takes one cycle, and three cycles are required for read. For burst read, new data are available every second cycle. External memory has multi-cycle read and write. The number of cycles depends on the type of memory and configuration of the external bus interface. Refer to the instruction summary for more details on instructions and instruction timing.

7.11 Device ID and Revision

Each device has a three-byte device ID. This ID identifies Atmel as the manufacturer of the device and the device type. A separate register contains the revision number of the device.

7.12 I/O Memory Protection

Some features in the device are regarded as critical for safety in some applications. Due to this, it is possible to lock the I/O register related to the clock system, the event system, and the advanced waveform extensions. As long as the lock is enabled, all related I/O registers are locked and they can not be written from the application software. The lock registers themselves are protected by the configuration change protection mechanism.

7.13 JTAG Disable

It is possible to disable the JTAG interface from the application software. This will prevent all external JTAG access to the device until the next device reset or until JTAG is enabled again from the application software. As long as JTAG is disabled, the I/O pins required for JTAG can be used as normal I/O pins.

7.14 Flash and EEPROM Page Size

The flash program memory and EEPROM data memory are organized in pages. The pages are word accessible for the flash and byte accessible for the EEPROM.

Table 7-2 on page 15 shows the Flash Program Memory organization. Flash write and erase operations are performed on one page at a time, while reading the Flash is done one byte at a time. For Flash access the Z-pointer (Z[m:n]) is used for addressing. The most significant bits in the address (FPAGE) gives the page number and the least significant address bits (FWORD) gives the word in the page.

Table 7-2. Number of words and Pages in the Flash.

Devices	PC size	Flash	Page Size	FWORD	FPAGE	Application		Boot	
	bits	bytes	words			Size	No of pages	Size	No of pages
ATxmega64A1U	16	64K + 4K	128	Z[7:1]	Z[16:8]	64K	256	4K	16
ATxmega128A1U	17	128K + 8K	256	Z[8:1]	Z[17:9]	128K	256	8K	16

Table 7-3 on page 16 shows EEPROM memory organization for the Atmel AVR XMEGA A1U devices. EEPROM write and erase operations can be performed one page or one byte at a time, while reading the EEPROM is done one byte at a time. For EEPROM access the NVM Address Register (ADDR[m:n]) is used for addressing. The most significant bits in the address (E2PAGE) give the page number and the least significant address bits (E2BYTE) give the byte in the page.

11.3.3 Power-save Mode

Power-save mode is identical to power down, with one exception. If the real-time counter (RTC) is enabled, it will keep running during sleep, and the device can also wake up from either an RTC overflow or compare match interrupt.

11.3.4 Standby Mode

Standby mode is identical to power down, with the exception that the enabled system clock sources are kept running while the CPU, peripheral, and RTC clocks are stopped. This reduces the wake-up time.

11.3.5 Extended Standby Mode

Extended standby mode is identical to power-save mode, with the exception that the enabled system clock sources are kept running while the CPU and peripheral clocks are stopped. This reduces the wake-up time.

24. USART

24.1 Features

- Eight identical USART peripherals
- Full-duplex operation
- Asynchronous or synchronous operation
  - Synchronous02 clock rates up to 1/2 of the device clock frequency
  - Asynchronous clock rates up to 1/8 of the device clock frequency
- Supports serial frames with 5, 6, 7, 8, or 9 data bits and 1 or 2 stop bits
- Fractional baud rate generator
  - Can generate desired baud rate from any system clock frequency
  - No need for external oscillator with certain frequencies
- Built-in error detection and correction schemes
  - Odd or even parity generation and parity check
  - Data overrun and framing error detection
  - Noise filtering includes false start bit detection and digital low-pass filter
- Separate interrupts for
  - Transmit complete
  - Transmit data register empty
  - Receive complete
- Multiprocessor communication mode
  - Addressing scheme to address a specific devices on a multi device bus
  - Enable unaddressed devices to automatically ignore all frames
- Master SPI mode
  - Double buffered operation
  - Operation up to 1/2 of the peripheral clock frequency
- IRCOM module for IrDA compliant pulse modulation/demodulation

24.2 Overview

The universal synchronous and asynchronous serial receiver and transmitter (USART) is a fast and flexible serial communication module. The USART supports full-duplex communication and asynchronous and synchronous operation. The USART can be configured to operate in SPI master mode and used for SPI communication.

Communication is frame based, and the frame format can be customized to support a wide range of standards. The USART is buffered in both directions, enabling continued data transmission without any delay between frames. Separate interrupts for receive and transmit complete enable fully interrupt driven communication. Frame error and buffer overflow are detected in hardware and indicated with separate status flags. Even or odd parity generation and parity check can also be enabled.

The clock generator includes a fractional baud rate generator that is able to generate a wide range of USART baud rates from any system clock frequencies. This removes the need to use an external crystal oscillator with a specific frequency to achieve a required baud rate. It also supports external clock input in synchronous slave operation.

When the USART is set in master SPI mode, all USART-specific logic is disabled, leaving the transmit and receive buffers, shift registers, and baud rate generator enabled. Pin control and interrupt generation are identical in both modes. The registers are used in both modes, but their functionality differs for some control settings.

An IRCOM module can be enabled for one USART to support IrDA 1.4 physical compliant pulse modulation and demodulation for baud rates up to 115.2Kbps.

PORTC, PORTD, PORTE, and PORTF each has two USARTs. Notation of these peripherals are USARTC0, USARTC1, USARTD0, USARTD1, USARTE0, USARTE1, USARTF0 and USARTF1.

31. AC – Analog Comparator

31.1 Features

- Four Analog Comparators
- Selectable propagation delay versus current consumption
- Selectable hysteresis
  - No
  - Small
  - Large
- Analog comparator output available on pin
- Flexible input selection
  - All pins on the port
  - Output from the DAC
  - Bandgap reference voltage
  - A 64-level programmable voltage scaler of the internal AV_{CC} voltage
- Interrupt and event generation on:
  - Rising edge
  - Falling edge
  - Toggle
- Window function interrupt and event generation on:
  - Signal above window
  - Signal inside window
  - Signal below window
- Constant current source with configurable output pin selection

31.2 Overview

The analog comparator (AC) compares the voltage levels on two inputs and gives a digital output based on this comparison. The analog comparator may be configured to generate interrupt requests and/or events upon several different combinations of input change.

Two important properties of the analog comparator's dynamic behavior are: hysteresis and propagation delay. Both of these parameters may be adjusted in order to achieve the optimal operation for each application.

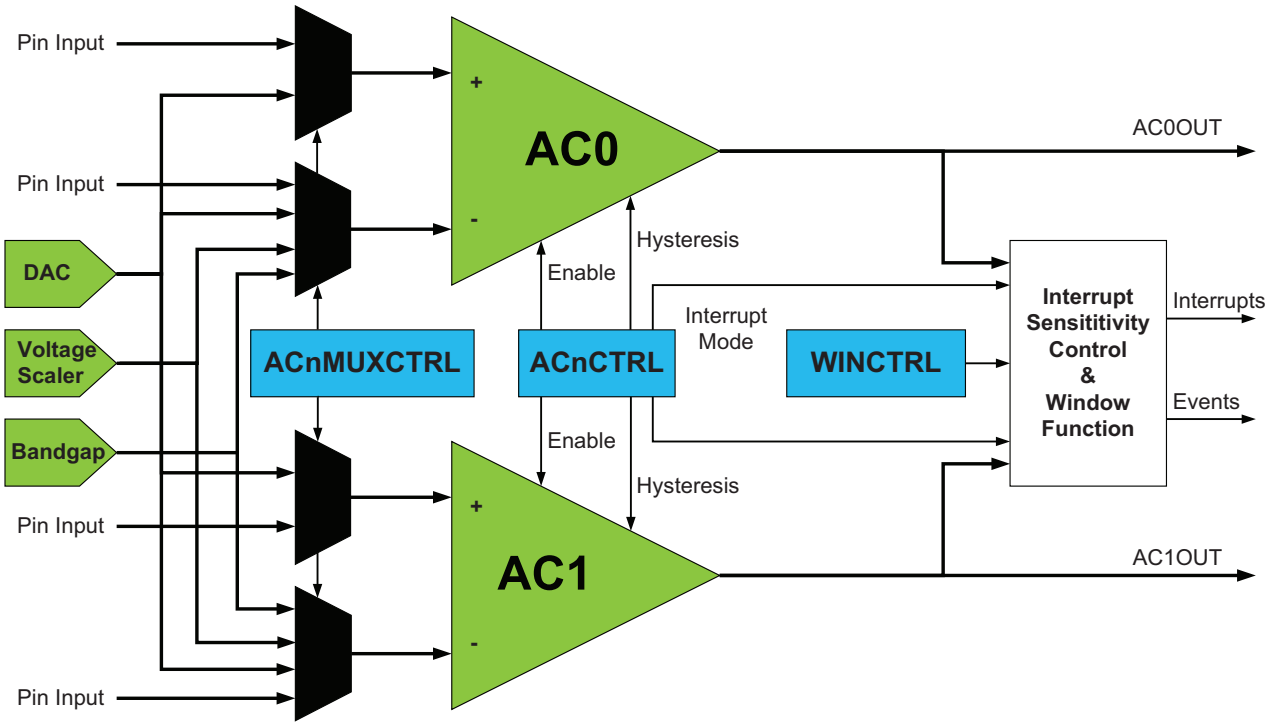
The input selection includes analog port pins, several internal signals, and a 64-level programmable voltage scaler. The analog comparator output state can also be output on a pin for use by external devices.

A constant current source can be enabled and output on a selectable pin. This can be used to replace, for example, external resistors used to charge capacitors in capacitive touch sensing applications.

The analog comparators are always grouped in pairs on each port. These are called analog comparator 0 (AC0) and analog comparator 1 (AC1). They have identical behavior, but separate control registers. Used as pair, they can be set in window mode to compare a signal to a voltage range instead of a voltage level.

PORTA and PORTB each has one AC pair. Notations are ACA and ACB, respectively.

Figure 31-1. Analog comparator overview.



The window function is realized by connecting the external inputs of the two analog comparators in a pair as shown in Figure 31-2.

Figure 31-2. Analog comparator window function.

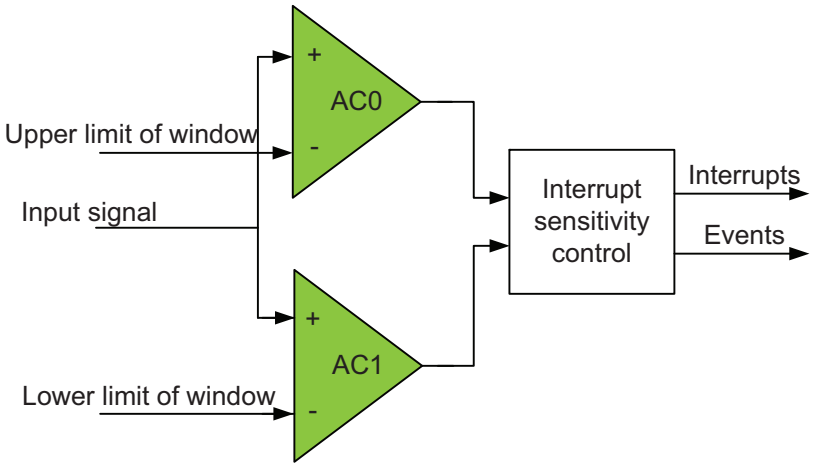


Table 37-5. Current consumption for modules and peripherals.

Symbol	Parameter	Condition[1]		Min.	Typ.	Max.	Units
I_{CC}	ULP oscillator				1.0		µA
	32.768kHz int. oscillator				27		
	2MHz int. oscillator				85		
		DFLL enabled with 32.768kHz int. osc. as reference			120		
	32MHz int. oscillator				310		
		DFLL enabled with 32.768kHz int. osc. as reference			560		
	Watchdog timer				1.0		
	BOD	Continuous mode			126		
		Sampled mode, includes ULP oscillator			1.2		
	Internal 1.0V reference				89		
	Temperature sensor				83		
	ADC	250ksps V_{REF} = Ext ref			3.0		mA
			CURRLIMIT = LOW		2.6		
			CURRLIMIT = MEDIUM		2.1		
			CURRLIMIT = HIGH		1.6		
	DAC	250ksps V_{REF} = Ext ref No load	Normal mode		1.9		
			Low Power mode		1.1		
	AC	High speed mode			324		µA
		Low power mode			122		
	DMA	615KBps between I/O registers and SRAM			140		
	Timer/counter				20		
	USART	Rx and Tx enabled, 9600 BAUD			4.0		
	Flash memory and EEPROM programming				4.0	8.0	mA

Note: 1. All parameters measured as the difference in current consumption between module enabled and disabled. All data at V_{CC} = 3.0V, Clk_{SYS} = 1MHz external clock without prescaling, T = 25°C unless other conditions are given.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
t_{delay}	Propagation delay	V_{CC} = 3.0V, T= 85°C	mode = HS		60	90	ns
		mode = HS			60		
		V_{CC} = 3.0V, T= 85°C	mode = LP		130		
	Current source calibration range	Single mode		2		8	µs
		Double mode		4		16	
	64-Level Voltage Scaler	Integral non-linearity (INL)			0.3	0.5	lsb

37.1.9 Bandgap and Internal 1.0V Reference Characteristics

Table 37-16. Bandgap and Internal 1.0V reference characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Startup time	As reference for ADC or DAC	1 Clk_{PER} + 2.5µs			µs
		As input voltage to ADC and AC		1.5		
	Bandgap voltage			1.1		V
INT1V	Internal 1.00V reference for ADC and DAC	T= 85°C, after calibration	0.99	1	1.01	
	Variation over voltage and temperature	Relative to T= 85°C, V_{CC} = 3.0V		±1.0		%

37.1.10 Brownout Detection Characteristics

Table 37-17. Brownout detection characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{BOT}	BOD level 0 falling V_{CC}		1.60	1.62	1.72	V
	BOD level 1 falling V_{CC}			1.8		
	BOD level 2 falling V_{CC}			2.0		
	BOD level 3 falling V_{CC}			2.2		
	BOD level 4 falling V_{CC}			2.4		
	BOD level 5 falling V_{CC}			2.6		
	BOD level 6 falling V_{CC}			2.8		
	BOD level 7 falling V_{CC}			3.0		
t_{BOD}	Detection time	Continuous mode		0.4		µs
		Sampled mode		1000		
V_{HYST}	Hysteresis			1.4		%

Table 37-21. Programming time.

Symbol	Parameter	Condition	Min.	Typ. [1]	Max.	Units
	Chip Erase	64KB Flash, EEPROM[2] and SRAM Erase		55		ms
	Flash	Page Erase		4		
		Page Write		4		
		Atomic Page Erase and Write		8		
	EEPROM	Page Erase		4		
		Page Write		4		
		Atomic Page Erase and Write		8		

Notes: 1. Programming is timed from the 2MHz internal oscillator.
2. EEPROM is not erased if the EESAVE fuse is programmed.

37.1.14 Clock and Oscillator Characteristics

37.1.14.1 Calibrated 32.768kHz Internal Oscillator characteristics

Table 37-22. 32.768kHz internal oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency			32.768		kHz
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-0.5		0.5	%
	User calibration accuracy		-0.5		0.5	

37.1.14.2 Calibrated 2MHz RC Internal Oscillator characteristics

Table 37-23. 2MHz internal oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Tunable frequency range	DFLL can tune to this frequency over voltage and temperature	1.8		2.2	MHz
	Factory calibrated frequency			2.0		
	Factory calibration accuracy	T = 85°C, V_{CC}= 3.0V	-1.5		1.5	%
	DFLL calibration stepsize	T = 25°C, V_{CC}= 3.0V		0.23		

37.1.14.6 External clock characteristics

Figure 37-3. External clock drive waveform.

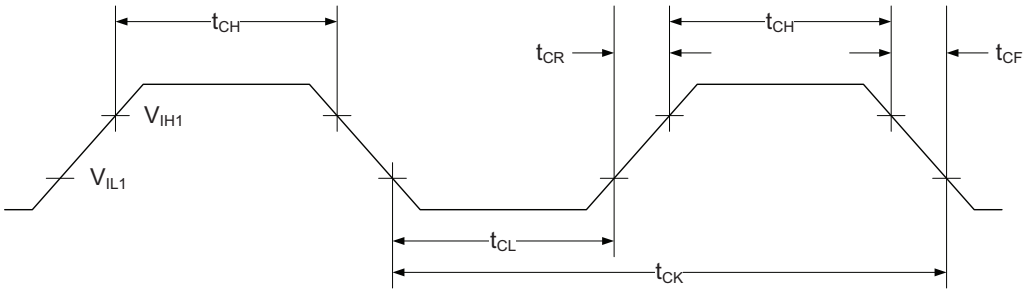


Table 37-27. External clock used as system clock without prescaling.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock Frequency (1)	V_{CC} = 1.6 - 1.8V	0		12	MHz
		V_{CC} = 2.7 - 3.6V	0		32	
t_{CK}	Clock Period	V_{CC} = 1.6 - 1.8V	83.3			ns
		V_{CC} = 2.7 - 3.6V	31.5			
t_{CH}	Clock High Time	V_{CC} = 1.6 - 1.8V	30.0			ns
		V_{CC} = 2.7 - 3.6V	12.5			
t_{CL}	Clock Low Time	V_{CC} = 1.6 - 1.8V	30.0			ns
		V_{CC} = 2.7 - 3.6V	12.5			
t_{CR}	Rise Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			10	ns
		V_{CC} = 2.7 - 3.6V			3	
t_{CF}	Fall Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			10	ns
		V_{CC} = 2.7 - 3.6V			3	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Note: 1. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

Table 37-28. External clock with prescaler (1) for system clock.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock Frequency (2)	V_{CC} = 1.6 - 1.8V	0		90	MHz
		V_{CC} = 2.7 - 3.6V	0		142	
t_{CK}	Clock Period	V_{CC} = 1.6 - 1.8V	11			ns
		V_{CC} = 2.7 - 3.6V	7			
t_{CH}	Clock High Time	V_{CC} = 1.6 - 1.8V	4.5			ns
		V_{CC} = 2.7 - 3.6V	2.4			

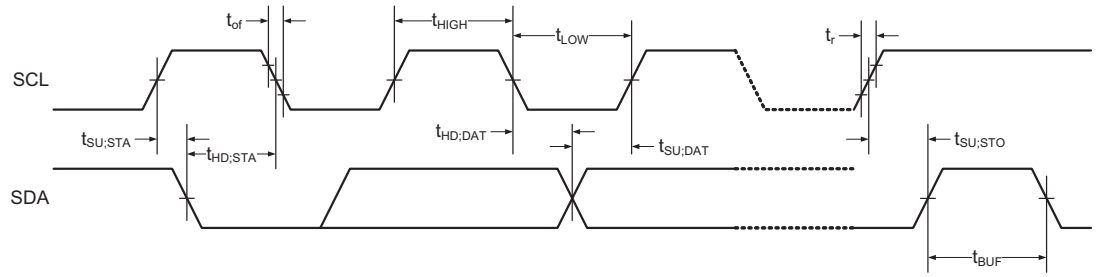
Table 37-33. EBI SDRAM characteristics and requirements.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$t_{ClkPER2}$	SDRAM clock period		$0.5*t_{ClkPER}$			ns
t_{AH}	SDRAM address hold time			$0.5*t_{ClkPER2}$		
t_{AS}	SDRAM address setup time			$0.5*t_{ClkPER2}$		
t_{CH}	SDRAM clock high-level width			$0.5*t_{ClkPER2}$		
t_{CL}	SDRAM clock low-level width			$0.5*t_{ClkPER2}$		
t_{CKH}	SDRAM CKE hold time			$0.5*t_{ClkPER2}$		
t_{CKS}	SDRAM CKE setup time			$0.5*t_{ClkPER2}$		
t_{CMH}	SDRAM CS, RAS, CAS, WE, DQM hold time			$0.5*t_{ClkPER2}$		
t_{CMS}	SDRAM CS, RAS, CAS, WE, DQM setup time			$0.5*t_{ClkPER2}$		
t_{DRH}	SDRAM data in hold after CLK high		0			
t_{AC}	SDRAM access time from CLK				t_{ClkPER}-5	
t_{DWH}	SDRAM data out hold after CLK high			$0.5*t_{ClkPER2}$		
t_{DWS}	SDRAM data out setup before CLK high			$0.5*t_{ClkPER2}$		

37.1.17 Two-Wire Interface Characteristics

Table 37-34 on page 96 describes the requirements for devices connected to the Two-Wire Interface Bus. The Atmel AVR XMEGA Two-Wire Interface meets or exceeds these requirements under the noted conditions. Timing symbols refer to Figure 37-7.

Figure 37-7. Two-Wire Interface bus timing.



Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Gain Error	1x gain, normal mode			-0.7		%
		8x gain, normal mode			-3.0		
		64x gain, normal mode			-4.8		
	Offset Error, input referred	1x gain, normal mode			0.4		mV
		8x gain, normal mode			0.4		
		64x gain, normal mode			0.4		
	Noise	1x gain, normal mode	V_{CC} = 3.6V Ext. V_{REF}		0.6		mV rms
		8x gain, normal mode			2.0		
		64x gain, normal mode			11		

Note: 1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% input voltage range.

37.2.7 DAC Characteristics

Table 37-46. Power supply, reference and output range.

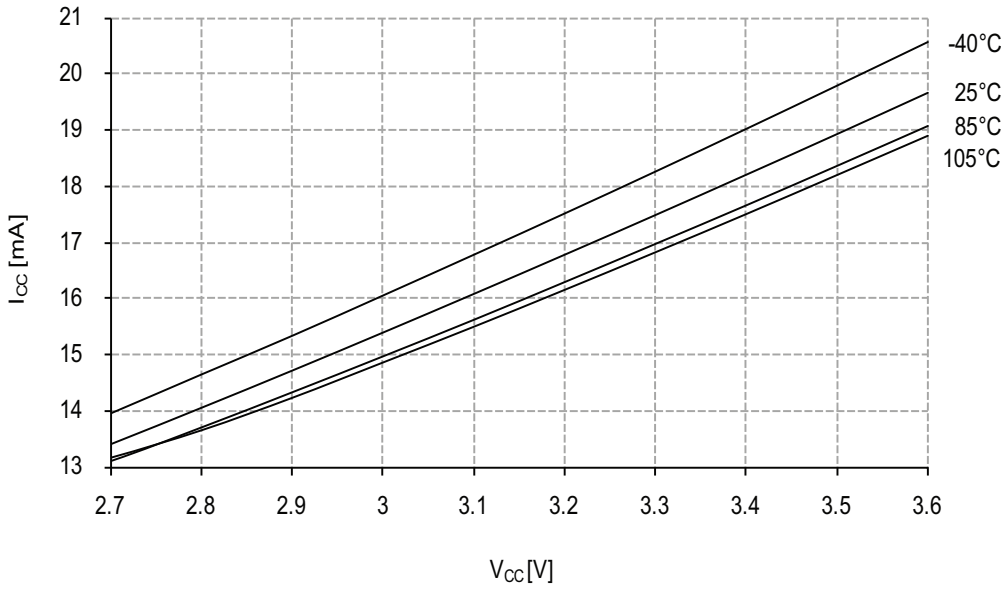
Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
AV_{CC}	Analog supply voltage		V_{CC}- 0.3		V_{CC}+ 0.3	
AV_{REF}	External reference voltage		1.0		V_{CC}- 0.6	V
$R_{channel}$	DC output impedance				50	Ω
	Linear output voltage range		0.15		AV_{CC}-0.15	V
R_{AREF}	Reference input resistance			>10		MΩ
CAREF	Reference input capacitance	Static load		7		pF
	Minimum resistance load		1			kΩ
	Maximum capacitance load				100	pF
		1000Ω serial resistance			1	nF
	Output sink/source	Operating within accuracy specification			AV_{CC}/1000	mA
		Safe operation			10	

Table 37-47. Clock and timing.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
f_{DAC}	Conversion rate	C_{load}=100pF, maximum step size	Normal mode	0		1000	ksps
			Low power mode			500	

Figure 38-7. Active mode supply current vs. V_{CC}.

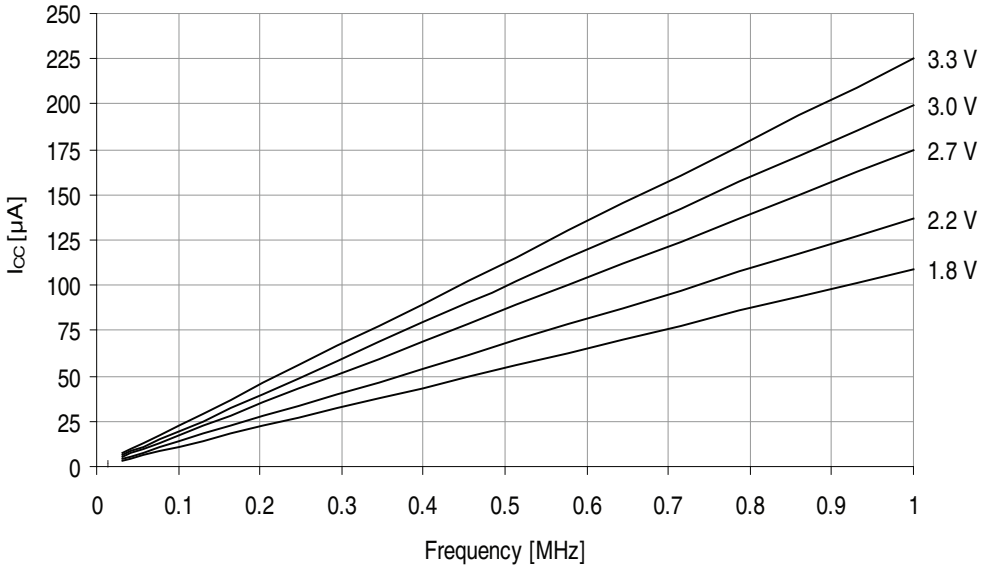
f_{SYS} = 32MHz internal oscillator.



38.1.1.2 Idle mode supply current

Figure 38-8. Idle mode supply current vs. frequency.

f_{SYS} = 0 - 1MHz external clock, T = 25°C.



38.1.8 External Reset Characteristics

Figure 38-61.Minimum Reset pin pulse width vs. V_{CC}.

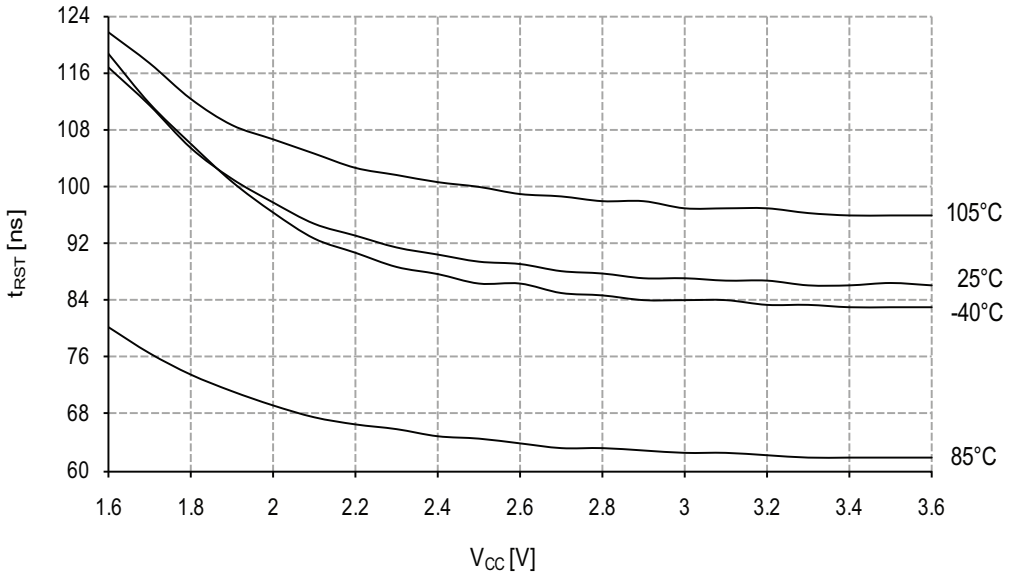


Figure 38-62.Reset pin pull-up resistor current vs. reset pin voltage.
V_{CC} = 1.8V.

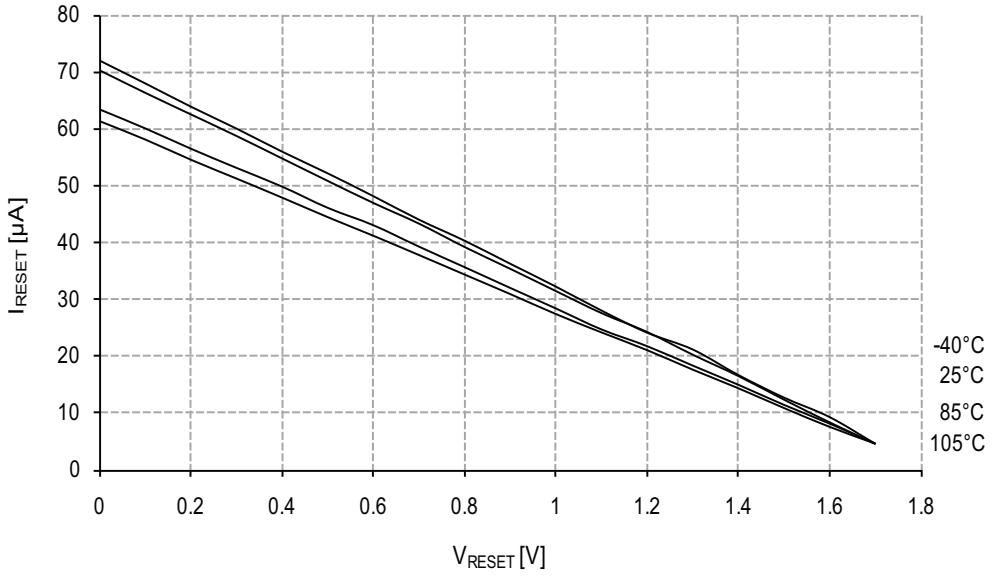


Figure 38-63.Reset pin pull-up resistor current vs. reset pin voltage.

V_{CC} = 3.0V.

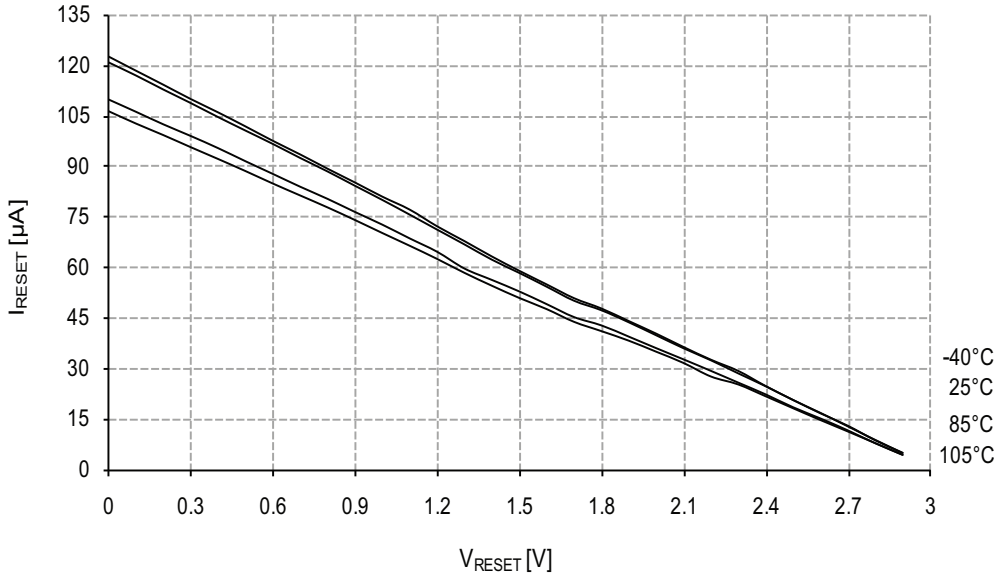


Figure 38-64.Reset pin pull-up resistor current vs. reset pin voltage.

V_{CC} = 3.3V.

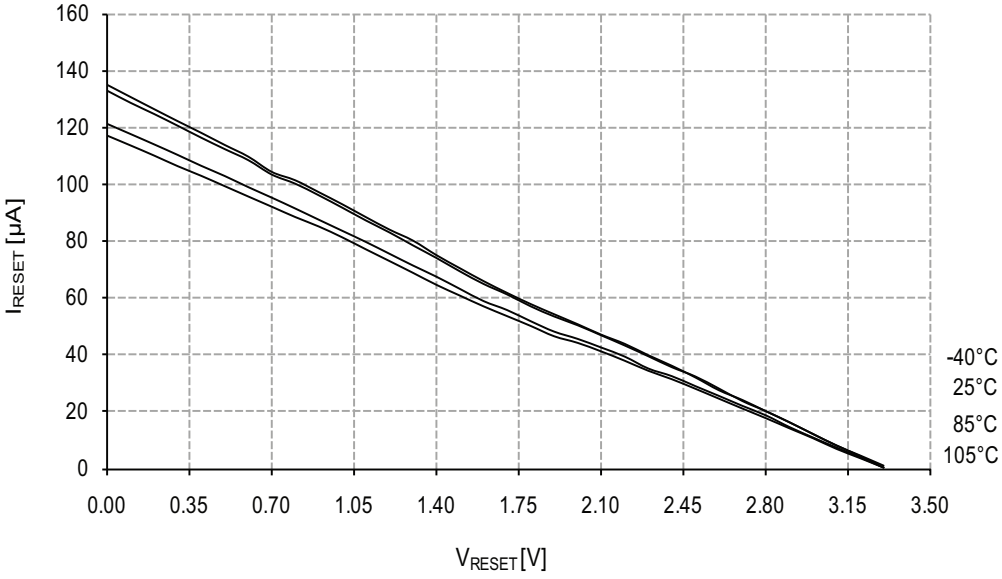
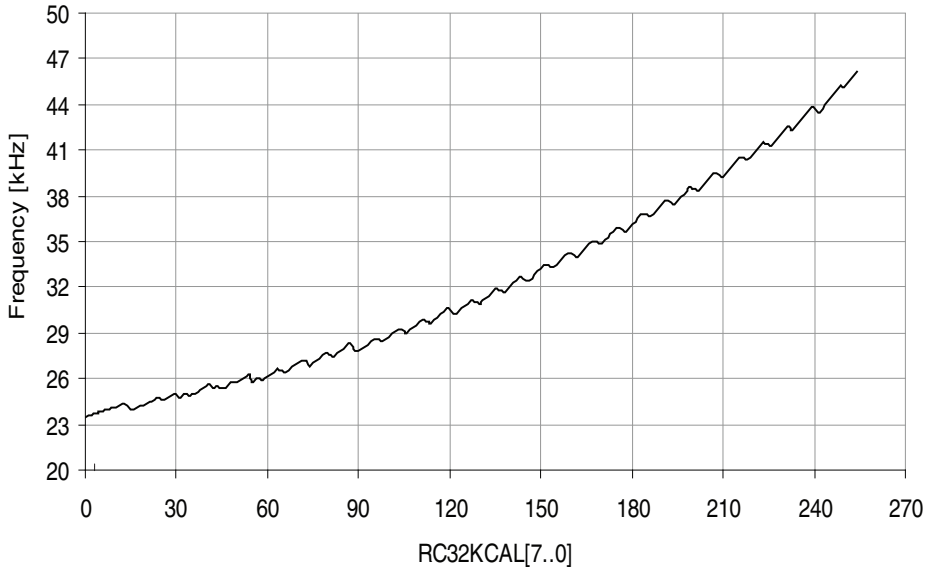


Figure 38-71. 32.768kHz internal oscillator frequency vs. calibration value.

V_{CC} = 3.0V, T = 25°C.



38.1.10.3 2MHz Internal Oscillator

Figure 38-72. 2MHz internal oscillator frequency vs. temperature.

DFLL disabled.

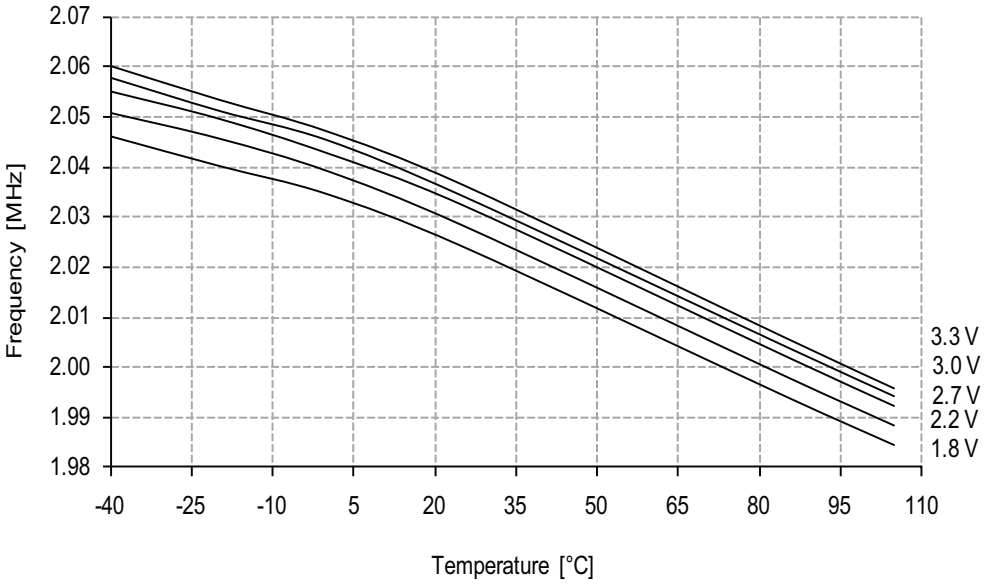


Figure 38-85. Active mode supply current vs. V_{CC}.

f_{SYS} = 32.768kHz internal oscillator.

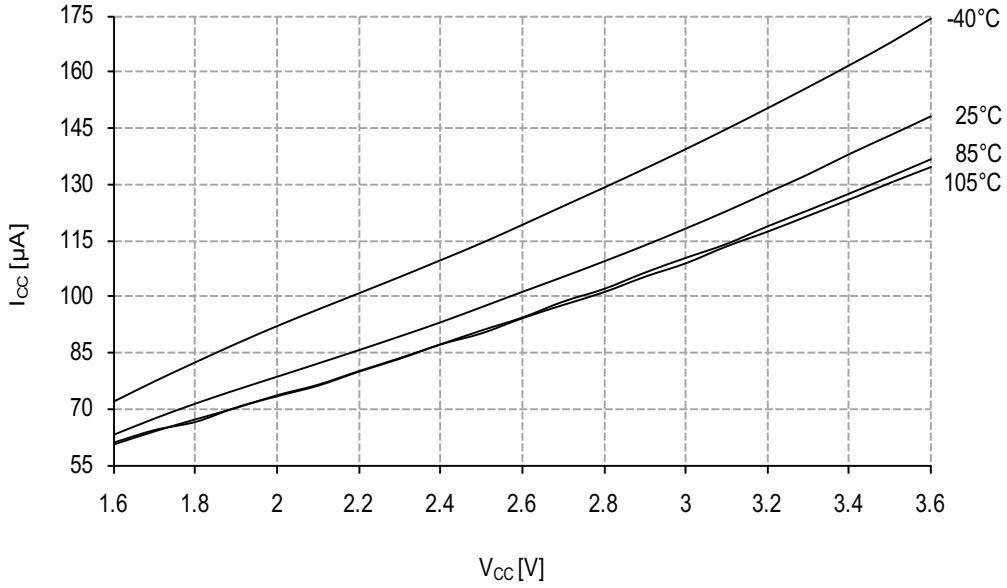


Figure 38-86. Active mode supply current vs. V_{CC}.

f_{SYS} = 1MHz external clock.

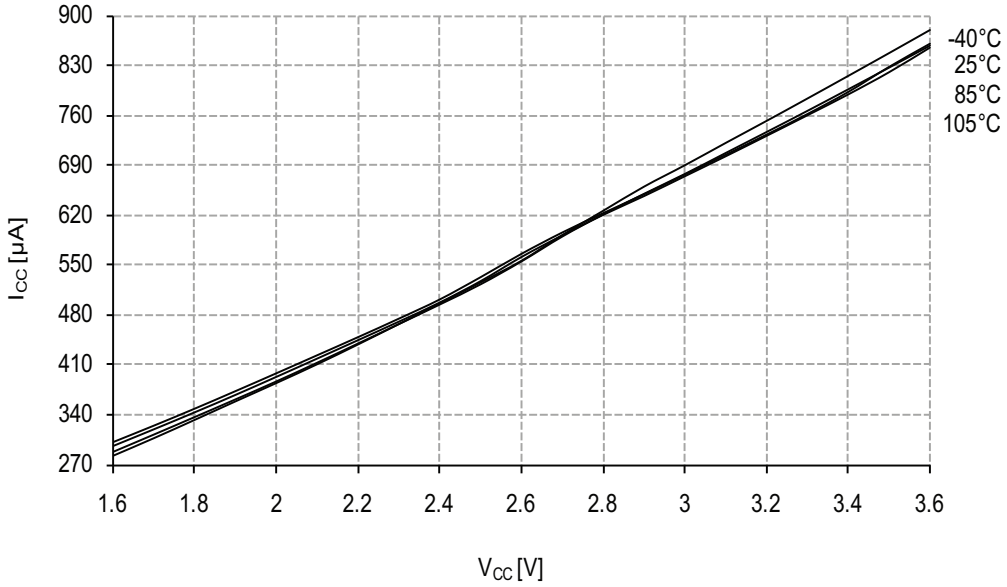
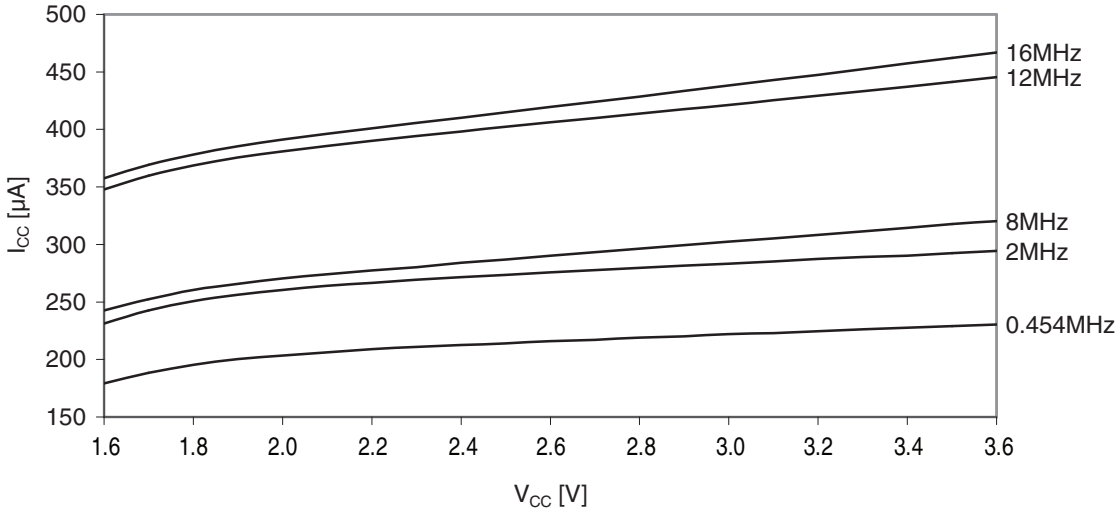


Figure 38-101. Standby supply current vs. V_{CC}.

25°C, running from different crystal oscillators.



38.2.2 I/O Pin Characteristics

38.2.2.1 Pull-up

Figure 38-102. I/O pin pull-up resistor current vs. pin voltage.

V_{CC} = 1.8V.

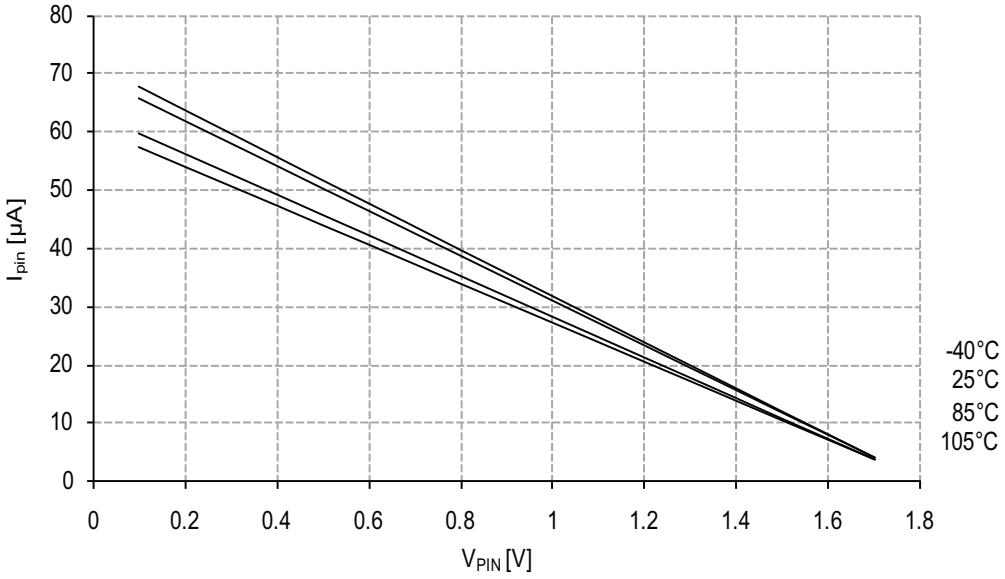


Figure 38-137.Analog comparator current source vs. calibration value.

Temperature = 25°C.

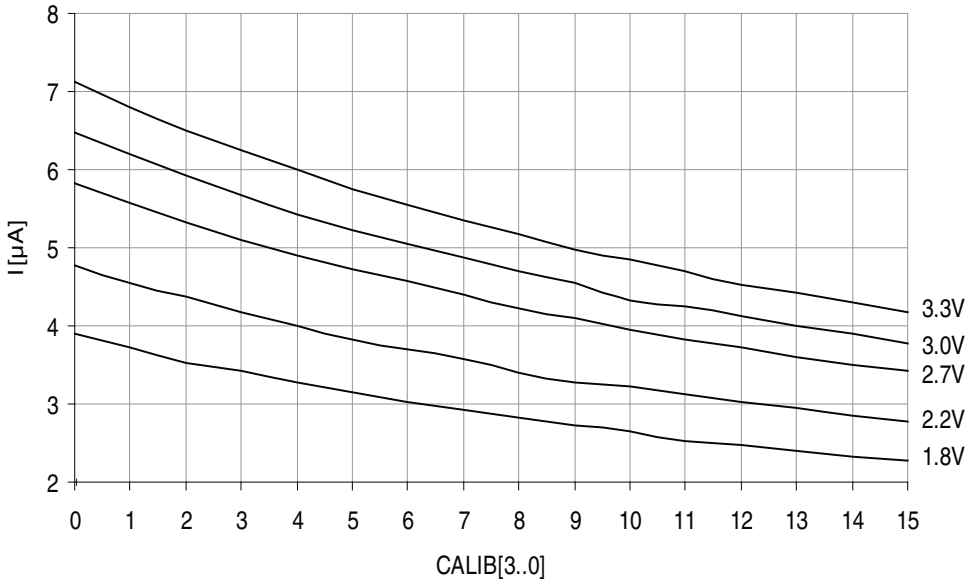


Figure 38-138.Analog comparator current source vs. calibration value.

V_{CC} = 3.0V.

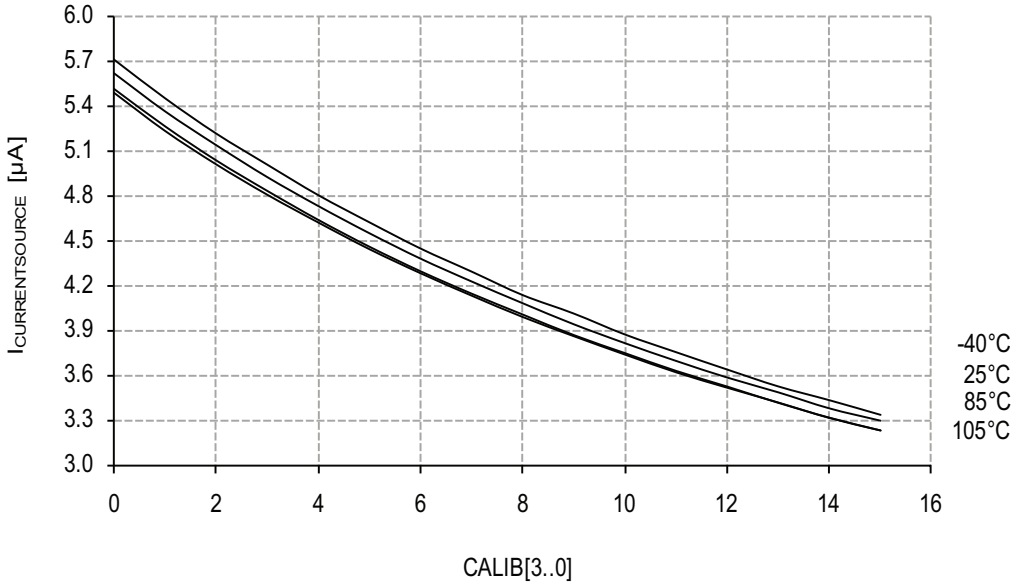
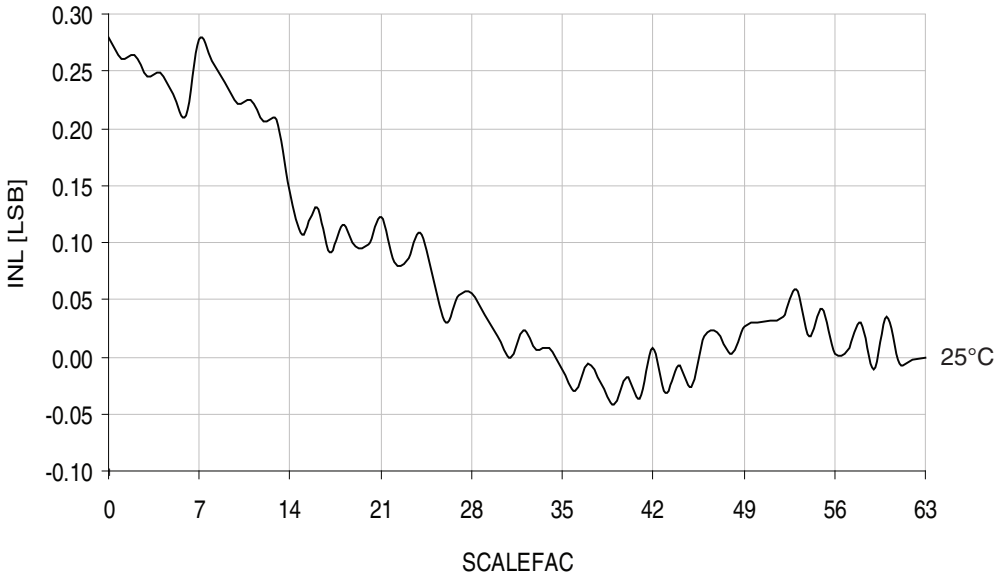


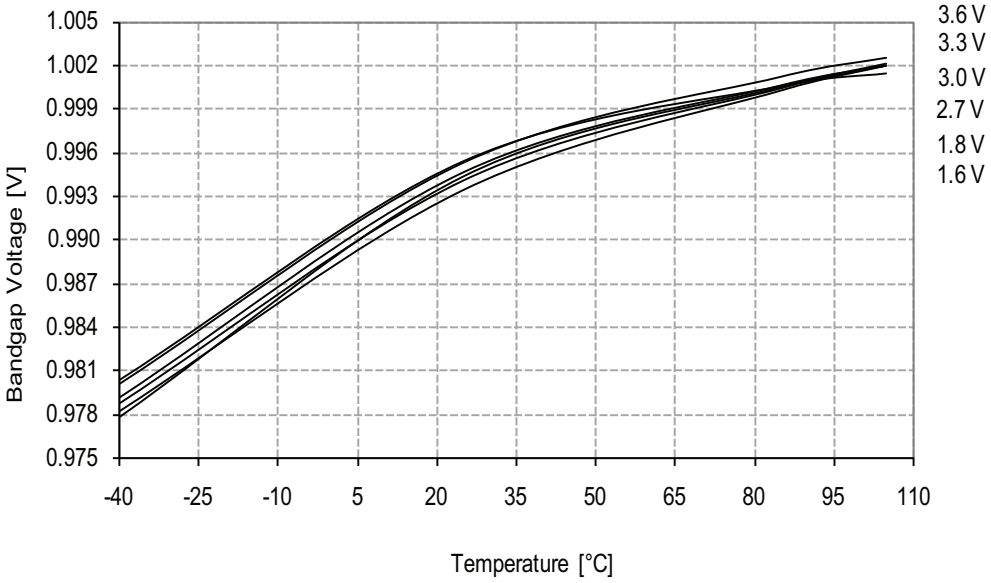
Figure 38-139.Voltage scaler INL vs. SCALEFAC.

T = 25°C, V_{CC} = 3.0V.



38.2.6 Internal 1.0V reference Characteristics

Figure 38-140. ADC/DAC Internal 1.0V reference vs. temperature.



Problem fix/Workaround

Allocate 1024bytes RAM buffer when using 1023 isochronous endpoint. This workaround is implemented in all USB software and source code delivered from Atmel in the AVR Software Framework.

9. **USB endpoint table is 16-byte alignment**

The USB endpoint table uses 16-byte alignment, instead of 16-bit alignment.

Problem fix/Workaround

Align the endpoint configuration table pointer in SRAM to a 16-byte. This workaround is implemented in all USB software and source code delivered from Atmel in the AVR Software Framework.

10. **USB Auto ZLP feature is non-functional**

The Auto ZLP feature is non-functional and can not be used.

Problem fix/Workaround

None.

11. **Disabling the USART transmitter does not automatically set the TxD pin direction to input**

If the USART transmitter is idle with no frames to transmit, setting TXEN to zero will not automatically set the TxD pin direction to input.

Problem fix/Workaround

The TxD pin direction can be set to input using the Port pin direction to input using the port direction (DIR) register. When the port pin direction is input, it will be immediate and ongoing transmissions will be truncated.

12. **TWI, SDAHOLD configuration in the TWI CTRL register is one bit**

The SDAHOLD configuration in the TWI Control register (CTRL) is one bit. Due to this the SDA hold time can be configured for maximum ~50ns when enabled. Configuring for longer hold time will have no effect.

Problem fix/Workaround

If longer SDA hold time than 50nS is required it must be handled in software.

13. **ADC has increased INL error in when used in SE unsigned mode at low temperatures**

When the ADC is used on single ended (SE) unsigned mode, -INL error is increased up to +/- 5 LSB in temperatures below -20C.

Problem fix/Workaround

Use the ADC in single ended signed mode.

14. **ADC is non-functional in SE unsigned mode with V_{REF} below 1.8V**

When the ADC is used on single ended unsigned mode and V_{REF} is below 1.8V, INL and DNL error is increased above +/- 10LSB, i.e. the ADC have missing codes under this condition.

Problem fix/Workaround

Use the ADC in single ended signed mode.