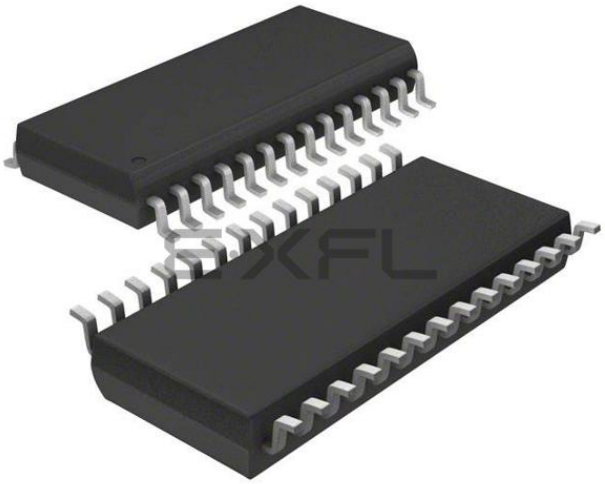

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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	USB Microcontroller
Core Processor	M8C
Program Memory Type	FLASH (16KB)
Controller Series	CY7C642xx
RAM Size	1K x 8
Interface	I²C, USB
Number of I/O	22
Voltage - Supply	3V ~ 5.25V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy7c64215-28pvxi

Applications

- PC human interface devices
  - Mouse (optomechanical, optical, trackball)
  - Keyboards
  - Joysticks
- Gaming
  - Game pads
  - Console keyboards
- General purpose
  - Barcode scanners
  - POS terminal
  - Consumer electronics
  - Toys
  - Remote controls
  - USB to serial

enCoRe III Functional Overview

The enCoRe III is based on the flexible PSoC architecture and is a full-featured, full-speed (12-Mbps) USB part. Configurable analog, digital, and interconnect circuitry enable a high level of integration in a host of consumer, and communication applications.

This architecture enables the user to create customized peripheral configurations that match the requirements of each individual application. Additionally, a fast CPU, flash program memory, SRAM data memory, and configurable I/O are included in both 28-pin SSOP and 56-pin QFN packages.

enCoRe III architecture, as illustrated in the "Block Diagram" on page 1, is comprised of four main areas: enCoRe III core, digital system, analog system, and system resources including a full-speed USB port. Configurable global busing enables all the device resources to combine into a complete custom system. The enCoRe III CY7C64215 can have up to seven I/O ports that connect to the global digital and analog interconnects, providing access to four digital blocks and six analog blocks.

enCoRe III Core

The enCoRe III Core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable GPIOs.

The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four-million instructions per second (MIPS) 8-bit Harvard-architecture microprocessor. The CPU uses an interrupt controller with up to 20 vectors, to simplify programming of real-time embedded events. Program execution is timed and protected using the included sleep and watchdog timers (WDT).

Memory encompasses 16 KB of flash for program storage, 1 KB of SRAM for data storage, and up to 2 KB of EEPROM emulated using the flash. Program flash uses four protection levels on blocks of 64 bytes, enabling customized software IP protection.

enCoRe III incorporates flexible internal clock generators, including a 24-MHz internal main oscillator (IMO) accurate to 8% over temperature and voltage as well as an option for an external clock oscillator (ECO). USB operation requires the OSC LOCK bit of the USB_CR0 register to be set to obtain IMO accuracy to.25%.

The 24-MHz IMO is doubled to 48 MHz for use by the digital system, if needed. The 48-MHz clock is required to clock the USB block and must be enabled for communication. A low-power 32-kHz internal low-speed oscillator (ILO) is provided for the sleep timer and WDT. The clocks, together with programmable clock dividers (system resource), provide flexibility to integrate almost any timing requirement into enCoRe III. In USB systems, the IMO self-tunes to ±0.25% accuracy for USB communication.

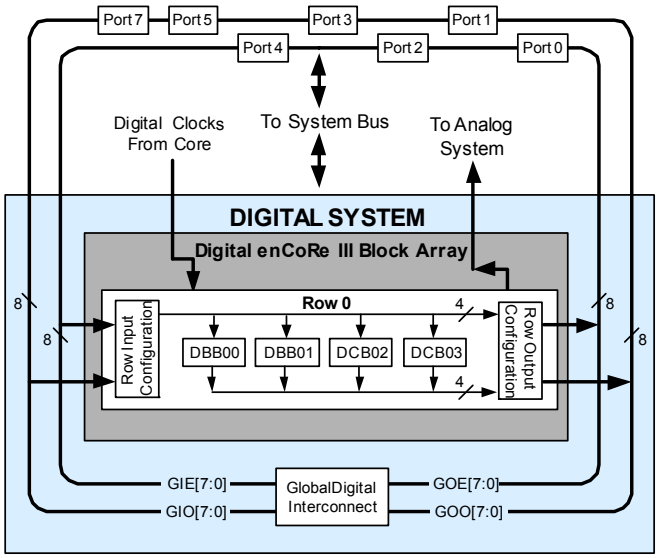
The extended temperature range for the industrial operating range (–40 °C to +85 °C) requires the use of an ECO, which is only available on the 56-pin QFN package.

enCoRe III GPIOs provide connection to the CPU, digital and analog resources of the device. Each pin's drive mode may be selected from eight options, enabling great flexibility in external interfacing. Every pin also has capability to generate a system interrupt on high-level, low-level, and change from last read.

The Digital System

The digital system is composed of four digital enCoRe III blocks. Each block is an 8-bit resource that is used alone or combined with other blocks to form 8-, 16-, 24-, and 32-bit peripherals, which are called user module references.

Figure 1. Digital System Block Diagram



The following digital configurations can be built from the blocks:

- PWMs, timers, and counters (8-bit and 16-bit)
- UART 8-bit with selectable parity
- SPI master and slave
- I^2C master
- RF interface: Interface to Cypress CYFI radio

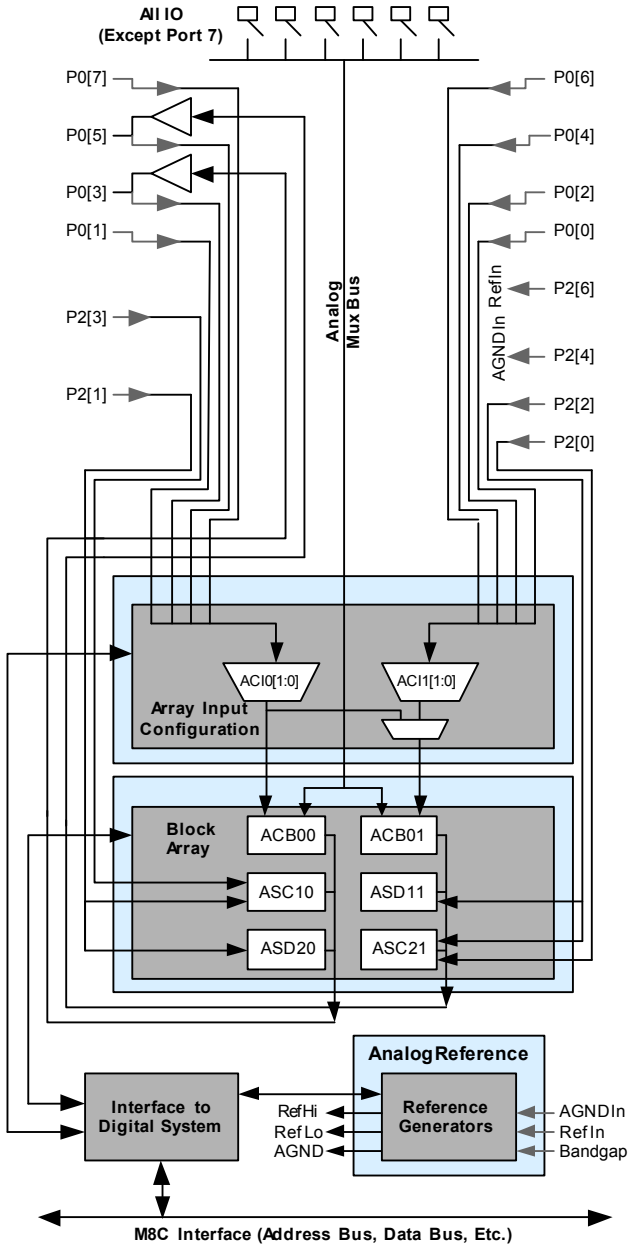
The digital blocks are connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also enable signal multiplexing and performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

The Analog System

The analog system is composed of six configurable blocks, comprised of an opamp circuit enabling the creation of complex analog signal flows. Analog peripherals are very flexible and are customized to support specific application requirements. enCoRe III analog function supports the Analog-to-digital converters (with 6- to 14-bit resolution, selectable as incremental, and delta-sigma) and programmable threshold comparator).

Analog blocks are arranged in two columns of three, with each column comprising one continuous time (CT) - AC B00 or AC B01 - and two switched capacitor (SC) - ASC10 and ASD20 or ASD11 and ASC21 - blocks, as shown in Figure 2.

Figure 2. Analog System Block Diagram



The Analog Multiplexer System

The analog mux bus can connect to every GPIO pin in ports 0 to 5. Pins are connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with comparators and analog-to-digital converters. It is split into two sections for simultaneous dual-channel processing. An additional 8:1 analog input multiplexer provides a second path to bring Port 0 pins to the analog array.

Additional System Resources

System resources provide additional capability useful to complete systems. Additional resources include a multiplier, decimator, low voltage detection, and power-on reset. Brief statements describing the merits of each resource follow.

- Full-speed USB (12 Mbps) with five configurable endpoints and 256 bytes of RAM. No external components required except two series resistors. Industrial temperature operating range for USB requires an external clock oscillator.
- Two multiply accumulates (MACs) provide fast 8-bit multipliers with 32-bit accumulate, to assist in both general math and digital filters.
- The decimator provides a custom hardware filter for digital signal processing applications including the creation of delta-sigma ADCs.
- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks are routed to both the digital and analog systems.
- The I^2C module provides 100- and 400-kHz communication over two wires. Slave, master, and multimaster modes are all supported.
- LVD interrupts can signal the application of falling voltage levels, while the advanced power-on reset (POR) circuit eliminates the need for a system supervisor.

enCoRe III Device Characteristics

enCoRe III devices have four digital blocks and six analog blocks. The following table lists the resources available for specific enCoRe III devices.

Table 1. enCoRe III Device Characteristics

Part Number	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY7C64215 28 Pin	up to 22	1	4	22	2	2	6	1K	16K
CY7C64215 56 Pin	up to 50	1	4	48	2	2	6	1K	16K

Pin Information

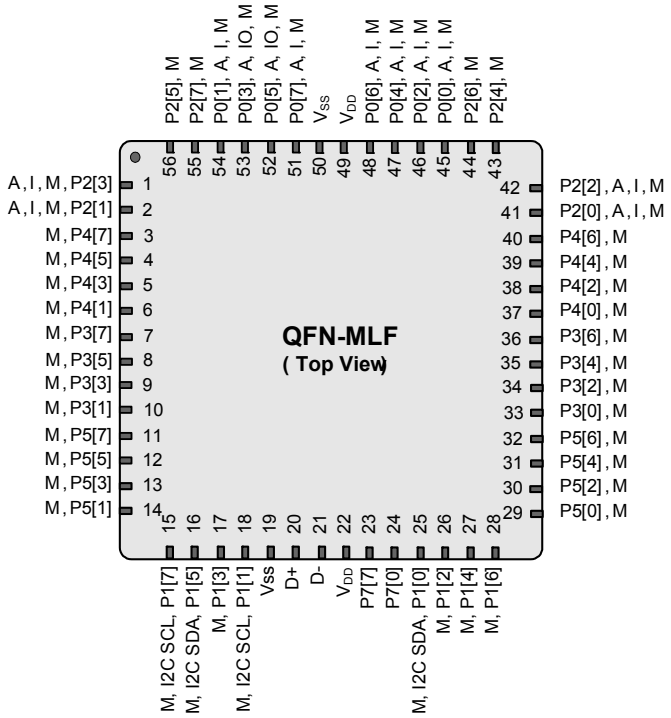
56-Pin Part Pinout

The CY7C64215 enCoRe III device is available in a 56-pin package which is listed and illustrated in the following table. Every port pin (labeled “P”) is capable of digital I/O. However, V_{SS} and V_{DD} are not capable of digital I/O.

Table 2. 56-Pin Part Pinout (QFN-MLF SAWN)[1]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I, M	P2[3]	Direct switched capacitor block input.
2	I/O	I, M	P2[1]	Direct switched capacitor block input.
3	I/O	M	P4[7]	
4	I/O	M	P4[5]	
5	I/O	M	P4[3]	
6	I/O	M	P4[1]	
7	I/O	M	P3[7]	
8	I/O	M	P3[5]	
9	I/O	M	P3[3]	
10	I/O	M	P3[1]	
11	I/O	M	P5[7]	
12	I/O	M	P5[5]	
13	I/O	M	P5[3]	
14	I/O	M	P5[1]	
15	I/O	M	P1[7]	I^2C serial clock (SCL).
16	I/O	M	P1[5]	I^2C serial data (SDA).
17	I/O	M	P1[3]	
18	I/O	M	P1[1]	I^2C SCL, ISSP-SCLK.
19	Power		V_{SS}	Ground connection.
20	USB		D+	
21	USB		D-	
22	Power		V_{DD}	Supply voltage.
23	I/O		P7[7]	
24	I/O		P7[0]	
25	I/O	M	P1[0]	I^2C SDA, ISSP-SDATA.
26	I/O	M	P1[2]	
27	I/O	M	P1[4]	Optional external clock input EXTCLK.
28	I/O	M	P1[6]	
29	I/O	M	P5[0]	
30	I/O	M	P5[2]	
31	I/O	M	P5[4]	
32	I/O	M	P5[6]	
33	I/O	M	P3[0]	
34	I/O	M	P3[2]	
35	I/O	M	P3[4]	
36	I/O	M	P3[6]	
37	I/O	M	P4[0]	
38	I/O	M	P4[2]	
39	I/O	M	P4[4]	
40	I/O	M	P4[6]	
41	I/O	I, M	P2[0]	Direct switched capacitor block input.
42	I/O	I, M	P2[2]	Direct switched capacitor block input.
43	I/O	M	P2[4]	External analog ground (AGND) input.
44	I/O	M	P2[6]	External voltage reference (VREF) input.
45	I/O	I, M	P0[0]	Analog column mux input.
46	I/O	I, M	P0[2]	Analog column mux input and column output.
47	I/O	I, M	P0[4]	Analog column mux input and column output.
48	I/O	I, M	P0[6]	Analog column mux input.
49	Power		V_{DD}	Supply voltage.
50	Power		V_{SS}	Ground connection.
51	I/O	I, M	P0[7]	Analog column mux input.
52	I/O	I/O, M	P0[5]	Analog column mux input and column output
53	I/O	I/O, M	P0[3]	Analog column mux input and column output.
54	I/O	I, M	P0[1]	Analog column mux input.
55	I/O	M	P2[7]	
56	I/O	M	P2[5]	

Figure 3. CY7C64215 56-Pin enCoRe III Device



LEGEND A = Analog, I = Input, O = Output, and M = Analog Mux Input.

Note
1. The center pad on the QFN-MLF package should be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal.

28-Pin Part Pinout

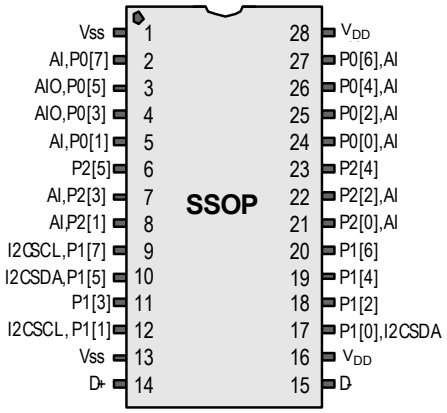
The CY7C64215 enCoRe III device is available in a 28-pin package which is listed and illustrated in the following table. Every port pin (labeled with a “P”) is capable of digital I/O. However, V_{SS} and V_{DD} are not capable of digital I/O.

Table 3. 28-Pin Part Pinout (SSOP)

Pin No.	Type		Name	Description
	Digital	Analog		
1	Power		GND	Ground connection.
2	I/O	I, M	P0[7]	Analog column mux input.
3	I/O	I/O,M	P0[5]	Analog column mux input and column output.
4	I/O	I/O,M	P0[3]	Analog column mux input and column output.
5	I/O	I,M	P0[1]	Analog column mux input.
6	I/O	M	P2[5]	
7	I/O	M	P2[3]	Direct switched capacitor block input.
8	I/O	M	P2[1]	Direct switched capacitor block input.
9	I/O	M	P1[7]	I^2C SCL
10	I/O	M	P1[5]	I^2C SDA
11	I/O	M	P1[3]	
12	I/O	M	P1[1]	I^2C SCL, ISSP-SCLK.
13	Power		GND	Ground connection.
14	USB		D+	
15	USB		D-	
16	Power		V_{DD}	Supply voltage.
17	I/O	M	P1[0]	I^2C SCL, ISSP-SDATA.
18	I/O	M	P1[2]	
19	I/O	M	P1[4]	
20	I/O	M	P1[6]	
21	I/O	M	P2[0]	Direct switched capacitor block input.
22	I/O	M	P2[2]	Direct switched capacitor block input.
23	I/O	M	P2[4]	External analog ground (AGND) input.
24	I/O	M	P0[0]	Analog column mux input.
25	I/O	M	P0[2]	Analog column mux input and column output.
26	I/O	M	P0[4]	Analog column mux input and column output.
27	I/O	M	P0[6]	Analog column mux input.
28	Power		V_{DD}	Supply voltage.

LEGEND A = Analog, I = Input, O = Output, and M = Analog Mux Input.

Figure 4. CY7C64215 28-Pin enCoRe III Device



Register Reference

The register conventions specific to this section are listed in the following table.

Table 4. Register Conventions

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

Register Mapping Tables

The enCoRe III device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks, bank 0 and bank 1. The XOI bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XOI bit is set to ‘1’, the user is in bank 1.

Note In the following register mapping tables, blank fields are reserved and should not be accessed.

Absolute Maximum Ratings

Table 5. Absolute Maximum Ratings

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{STG}	Storage temperature	–55	–	+100	°C	Higher storage temperatures reduces data retention time.
$T_{BAKETEMP}$	Bake temperature	–	125	See package label	°C	–
$T_{BAKETIME}$	Bake time	See package label	–	72	Hours	–
T_A	Ambient temperature with power applied	0	–	+70	°C	–
V_{DD}	Supply voltage on V_{DD} relative to V_{SS}	–0.5	–	+6.0	V	–
V_{IO}	DC input voltage	V_{SS} – 0.5	–	V_{DD} + 0.5	V	–
V_{IO2}	DC voltage applied to tristate	V_{SS} – 0.5	–	V_{DD} + 0.5	V	–
I_{MIO}	Maximum current into any port pin	–25	–	+50	mA	–
I_{MAIO}	Maximum current into any port pin configured as an analog driver	–50	–	+50	mA	–
ESD	Electrostatic discharge voltage	2000	–	–	V	Human body model ESD.
LU	Latch up current	–	–	200	mA	–

Operating Temperature

Table 6. Operating Temperature

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{AC}	Commercial ambient temperature	0	–	+70	°C	–
T_{AI}	Industrial ambient temperature	–40	–	+85	°C	USB operation requires the use of an external clock oscillator and the 56-pin QFN package.
T_J	Junction temperature	–40	–	+100	°C	The temperature rise from ambient to junction is package specific. See “Thermal Impedance” on page 32. The user must limit the power consumption to comply with this requirement.

DC Electrical Characteristics

DC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.15 V to 3.5 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 7. DC Chip-Level Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{DD}	Supply voltage	3.0	–	5.25	V	See DC POR and LVD specifications, Table 15 on page 22. USB hardware is not functional when V_{DD} is between 3.5 V to 4.35 V.
I_{DD5}	Supply current, IMO = 24 MHz (5 V)	–	14	27	mA	Conditions are V_{DD} = 5.0 V, T_A = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz, analog power = off.
I_{DD3}	Supply current, IMO = 24 MHz (3.3 V)	–	8	14	mA	Conditions are V_{DD} = 3.3 V, T_A = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 0.367 kHz, analog power = off.
I_{SB}	Sleep [3] (mode) current with POR, LVD, sleep timer, and WDT [4].	–	3	6.5	µA	Conditions are with internal slow speed oscillator, V_{DD} = 3.3 V, 0 °C ≤ T_A ≤ 55 °C, analog power = off.
I_{SBH}	Sleep (mode) current with POR, LVD, sleep timer, and WDT at high temperature [4] .	–	4	25	µA	Conditions are with internal slow speed oscillator, V_{DD} = 3.3 V, 55 °C < T_A ≤ 70 °C, analog power = off.

Notes

3. Errata: When the device operates at4.75 V to 5.25 V and the 3.3-V regulator is enabled, a short low pulse may be created on the DP signal line during device wakeup. The 15- to 20-µs low pulse of the DP line may be interpreted by the host computer as a deattach or the beginning of a wakeup. For more details refer to Errata on page 40.
4. Standby current includes all functions (POR, LVD, WDT, sleep time) needed for reliable system operation. This should be compared with devices that have similar functions enabled.

DC Analog Reference Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.15 V to 3.5 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

The guaranteed specifications are measured through the analog continuous time PSoC blocks. The power levels for AGND refer to the power of the Analog Continuous Time PSoC block. The power levels for RefHi and RefLo refer to the Analog Reference Control register. The limits stated for AGND include the offset error of the AGND buffer local to the Analog Continuous Time PSoC block. Reference control power is high.

Table 12. 5-V DC Analog Reference Specifications

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b000	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.229	$V_{DD}/2$ + 1.290	$V_{DD}/2$ + 1.346	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.038	$V_{DD}/2$	$V_{DD}/2$ + 0.040	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.356	$V_{DD}/2$ – 1.295	$V_{DD}/2$ – 1.218	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.220	$V_{DD}/2$ + 1.292	$V_{DD}/2$ + 1.348	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.036	$V_{DD}/2$	$V_{DD}/2$ + 0.036	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.357	$V_{DD}/2$ – 1.297	$V_{DD}/2$ – 1.225	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.221	$V_{DD}/2$ + 1.293	$V_{DD}/2$ + 1.351	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.036	$V_{DD}/2$	$V_{DD}/2$ + 0.036	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.357	$V_{DD}/2$ – 1.298	$V_{DD}/2$ – 1.228	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.219	$V_{DD}/2$ + 1.293	$V_{DD}/2$ + 1.353	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.037	$V_{DD}/2$ – 0.001	$V_{DD}/2$ + 0.036	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.359	$V_{DD}/2$ – 1.299	$V_{DD}/2$ – 1.229	V
0b001	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.092	P2[4] + P2[6] – 0.011	P2[4] + P2[6] + 0.064	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.031	P2[4] – P2[6] + 0.007	P2[4] – P2[6] + 0.056	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.078	P2[4] + P2[6] – 0.008	P2[4] + P2[6] + 0.063	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.031	P2[4] – P2[6] + 0.004	P2[4] – P2[6] + 0.043	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.073	P2[4] + P2[6] – 0.006	P2[4] + P2[6] + 0.062	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.032	P2[4] – P2[6] + 0.003	P2[4] – P2[6] + 0.038	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.073	P2[4] + P2[6] – 0.006	P2[4] + P2[6] + 0.062	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.034	P2[4] – P2[6] + 0.002	P2[4] – P2[6] + 0.037	V

Table 13. 3.3-V DC Analog Reference Specifications

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b000	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.200	$V_{DD}/2$ + 1.290	$V_{DD}/2$ + 1.365	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.030	$V_{DD}/2$	$V_{DD}/2$ + 0.034	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.346	$V_{DD}/2$ – 1.292	$V_{DD}/2$ – 1.208	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.196	$V_{DD}/2$ + 1.292	$V_{DD}/2$ + 1.374	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.029	$V_{DD}/2$	$V_{DD}/2$ + 0.031	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.349	$V_{DD}/2$ – 1.295	$V_{DD}/2$ – 1.227	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.204	$V_{DD}/2$ + 1.293	$V_{DD}/2$ + 1.369	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.030	$V_{DD}/2$	$V_{DD}/2$ + 0.030	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.351	$V_{DD}/2$ – 1.297	$V_{DD}/2$ – 1.229	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.189	$V_{DD}/2$ + 1.294	$V_{DD}/2$ + 1.384	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.032	$V_{DD}/2$	$V_{DD}/2$ + 0.029	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.353	$V_{DD}/2$ – 1.297	$V_{DD}/2$ – 1.230	V
0b001	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.105	P2[4] + P2[6] – 0.008	P2[4] + P2[6] + 0.095	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.035	P2[4] – P2[6] + 0.006	P2[4] – P2[6] + 0.053	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.094	P2[4] + P2[6] – 0.005	P2[4] + P2[6] + 0.073	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.033	P2[4] – P2[6] + 0.002	P2[4] – P2[6] + 0.042	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.094	P2[4] + P2[6] – 0.003	P2[4] + P2[6] + 0.075	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.035	P2[4] – P2[6]	P2[4] – P2[6] + 0.038	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] + P2[6] – 0.095	P2[4] + P2[6] – 0.003	P2[4] + P2[6] + 0.080	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 0.5 V)	P2[4] – P2[6] – 0.038	P2[4] – P2[6]	P2[4] – P2[6] + 0.038	V
0b010	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.119	V_{DD} – 0.005	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.028	$V_{DD}/2$	$V_{DD}/2$ + 0.029	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.022	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.131	V_{DD} – 0.004	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.028	$V_{DD}/2$	$V_{DD}/2$ + 0.028	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.021	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.111	V_{DD} – 0.003	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.029	$V_{DD}/2$	$V_{DD}/2$ + 0.028	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.002	V_{SS} + 0.017	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	V_{DD}	V_{DD} – 0.128	V_{DD} – 0.003	V_{DD}	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.029	$V_{DD}/2$	$V_{DD}/2$ + 0.029	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.002	V_{SS} + 0.019	V
0b011	All power settings. Not allowed for 3.3 V.	–	–	–	–	–	–	–

DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.15 V to 3.5 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 16. DC Programming Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{DDP}	V_{DD} for programming and erase	4.5	5.0	5.5	V	This specification applies to the functional requirements of external programmer tools
V_{DDLV}	Low V_{DD} for verify	3.0	3.1	3.2	V	This specification applies to the functional requirements of external programmer tools
V_{DDHV}	High V_{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools
$V_{DDIWRITE}$	Supply voltage for flash write operation	3.15	–	5.25	V	This specification applies to this device when it is executing internal flash writes
I_{DDP}	Supply current during programming or verify	–	15	30	mA	–
V_{ILP}	Input low voltage during programming or verify	–	–	0.8	V	–
V_{IHP}	Input high voltage during programming or Verify	2.1	–	–	V	–
I_{ILP}	Input current when applying Vilp to P1[0] or P1[1] during programming or verify	–	–	0.2	mA	Driving internal pull-down resistor.
I_{IHP}	Input current when applying Vihp to P1[0] or P1[1] during programming or verify	–	–	1.5	mA	Driving internal pull-down resistor.
V_{OLV}	Output low voltage during programming or verify	–	–	V_{SS} + 0.75	V	–
V_{OHV}	Output high voltage during programming or verify	V_{DD} – 1.0	–	V_{DD}	V	–
$Flash_{ENPB}$	Flash endurance (per block)	50,000[8]	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash endurance (total)[9]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash data retention	10	–	–	Years	–

DC I^2C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.15 V to 3.5 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 17. DC I^2C Specifications [10]

Symbol	Description	Min	Typ	Max	Units	Notes
V_{ILI2C}	Input low level	–	–	0.3 × V_{DD}	V	3.15 V ≤ V_{DD} ≤ 3.6 V
		–	–	0.25 × V_{DD}	V	4.75 V ≤ V_{DD} ≤ 5.25 V
V_{IHI2C}	Input high level	0.7 × V_{DD}	–	–	V	3.15 V ≤ V_{DD} ≤ 5.25 V

Notes

8. The 50,000 cycle Flash endurance per block will only be guaranteed if the Flash is operating within one voltage range. Voltage ranges are 3.0V to 3.6V and 4.75V to 5.25V.
9. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).
   For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs application note AN2015 for more information.
10. All GPIOs meet the DC GPIO V_{IL} and V_{IH} specifications found in the DC GPIO Specifications sections. The I^2C GPIO pins also meet the mentioned specifications.

AC Electrical Characteristics

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.15 V to 3.5 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 18. AC Chip-Level Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
$F_{IMO245V}$	IMO frequency for 24 MHz (5 V)	23.04	24	24.96[11, 12]	MHz	Trimmed for 5 V operation using factory trim values.
$F_{IMO243V}$	IMO frequency for 24 MHz (3.3 V)	22.08	24	25.92[11,13]	MHz	Trimmed for 3.3 V operation using factory trim values.
F_{IMOUSB}	IMO frequency with USB frequency locking enabled and USB traffic present	23.94	24	24.06[12]	MHz	USB operation for system clock source from the IMO is limited to 0°C ≤ T_A ≤ 70°C.
F_{CPU1}	CPU frequency (5 V nominal)	0.090	24	24.96[11,12]	MHz	SLIMO mode = 0.
F_{CPU2}	CPU frequency (3.3 V nominal)	0.086	12	12.96[12,13]	MHz	SLIMO mode = 0.
F_{BLK5}	Digital PSoC block frequency (5 V nominal)	0	48	49.92[11,12,14]	MHz	Refer to the AC Digital Block Specifications on page 26.
F_{BLK3}	Digital PSoC block frequency (3.3 V nominal)	0	24	25.92[12,14]	MHz	–
F_{32K1}	ILO frequency	15	32	64	kHz	–
F_{32K_U}	ILO untrimmed frequency	5	–	100	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference Manual for details on this timing.
DC_{ILO}	ILO duty cycle	20	50	80	%	–
DC_{24M}	24-MHz duty cycle	40	50	60	%	–
Step24M	24-MH trim step size	–	50	–	kHz	–
Fout48M	48-MHz output frequency	46.08	48.0	49.92[11,13]	MHz	Trimmed. Utilizing factory trim values.
F_{MAX}	Maximum frequency of signal on row input or row output	–	–	12.96	MHz	–
SR_{POWER_UP}	Power supply slew rate	–	–	250	V/ms	–
$T_{POWERUP}$	Time from end of POR to CPU executing code	–	16	100	ms	–
T_{jit_IMO}[15]	24 MHz IMO cycle-to-cycle jitter (RMS)	–	200	1200	ps	
	24 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	900	6000	ps	N = 32.
	24 MHz IMO period jitter (RMS)	–	200	900	ps	

Notes

11. 4.75 V < V_{DD} < 5.25 V.
12. Accuracy derived from Internal Main Oscillator with appropriate trim for V_{DD} range.
13. 3.0 V < V_{DD} < 3.6 V. See application note AN2012 “Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation” for information on trimming for operation at 3.3 V.
14. See the individual user module data sheets for information on maximum frequencies for user modules.
15. Refer to Cypress Jitter Specifications application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 for more information.

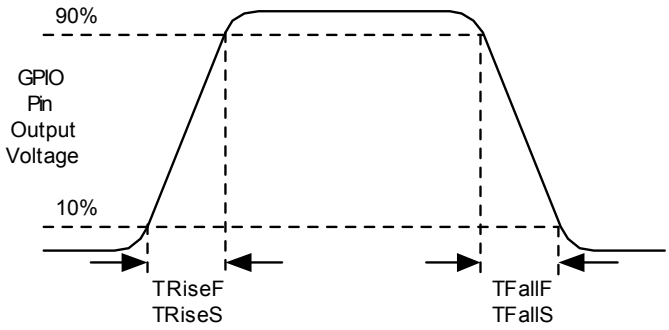
AC GPIO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.15 V to 3.5 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 19. AC GPIO Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
F_{GPIO}	GPIO operating frequency	0	–	12	MHz	Normal Strong Mode
TRiseF	Rise time, normal strong mode, Cload = 50 pF	3	–	18	ns	V_{DD} = 4.5 to 5.25 V, 10%–90%
TFallF	Fall time, normal strong mode, Cload = 50 pF	2	–	18	ns	V_{DD} = 4.5 to 5.25 V, 10%–90%
TRiseS	Rise time, slow strong mode, Cload = 50 pF	10	27	–	ns	V_{DD} = 3 to 5.25 V, 10%–90%
TFallS	Fall time, slow strong mode, Cload = 50 pF	10	22	–	ns	V_{DD} = 3 to 5.25 V, 10%–90%

Figure 6. GPIO Timing Diagram



AC Full Speed USB Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.15 V to 3.5 V and –40 °C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 20. AC Full-Speed (12 Mbps) USB Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{RFS}	Transition rise time	4	–	20	ns	For 50-pF load.
T_{FSS}	Transition fall time	4	–	20	ns	For 50-pF load.
T_{RFMFS}	Rise/fall time matching: (T_R/T_F)	90	–	111	%	For 50-pF load.
$T_{DRATEFS}$	Full-speed data rate	12 – 0.25%	12	12 + 0.25%	Mbps	–

AC External Clock Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.15 V to 3.5 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 22. AC External Clock Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
F_{OSCEXT}	Frequency for USB applications	23.94	24	24.06	MHz	USB operation in the extended Industrial temperature range (–40 °C ≤ T_A ≤ 85 °C) requires that the system clock is sourced from an external clock oscillator.
–	Duty cycle	47	50	53	%	–
–	Power-up to IMO switch	150	–	–	µs	–

AC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.15 V to 3.5 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 23. 5 V AC Analog Output Buffer Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{ROB}	Rising settling time to 0.1%, 1 V Step, 100-pF load Power = low Power = high	 – –	 – –	 2.5 2.5	 µs µs	–
T_{SOB}	Falling settling time to 0.1%, 1 V Step, 100-pF load Power = low Power = high	 – –	 – –	 2.2 2.2	 µs µs	–
SR_{ROB}	Rising slew rate (20% to 80%), 1 V Step, 100-pF load Power = low Power = high	 0.65 0.65	 – –	 – –	 V/µs V/µs	–
SR_{FOB}	Falling slew rate (80% to 20%), 1 V Step, 100-pF load Power = low Power = high	 0.65 0.65	 – –	 – –	 V/µs V/µs	–
BW_{OBSS}	Small signal bandwidth, 20 mV_{pp}, 3-dB BW, 100-pF load Power = low Power = high	 0.8 0.8	 – –	 – –	 MHz MHz	–
BW_{OBLS}	Large signal bandwidth, 1 V_{pp}, 3-dB BW, 100-pF load Power = low Power = high	 300 300	 – –	 – –	 kHz kHz	–

Table 24. 3.3 V AC Analog Output Buffer Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{ROB}	Rising settling time to 0.1%, 1 V Step, 100-pF load Power = low Power = high	 – –	 – –	 3.8 3.8	 µs µs	–
T_{SOB}	Falling settling time to 0.1%, 1 V Step, 100-pF load Power = low Power = high	 – –	 – –	 2.6 2.6	 µs µs	–
SR_{ROB}	Rising slew rate (20% to 80%), 1 V Step, 100-pF load Power = low Power = high	 0.5 0.5	 – –	 – –	 V/µs V/µs	–
SR_{FOB}	Falling slew rate (80% to 20%), 1 V Step, 100-pF load Power = low Power = high	 0.5 0.5	 – –	 – –	 V/µs V/µs	–
BW_{OBSS}	Small signal bandwidth, 20 mV_{pp}, 3dB BW, 100-pF load Power = low Power = high	 0.7 0.7	 – –	 – –	 MHz MHz	–
BW_{OBLS}	Large signal bandwidth, 1 V_{pp}, 3dB BW, 100-pF load Power = low Power = high	 200 200	 – –	 – –	 kHz kHz	–

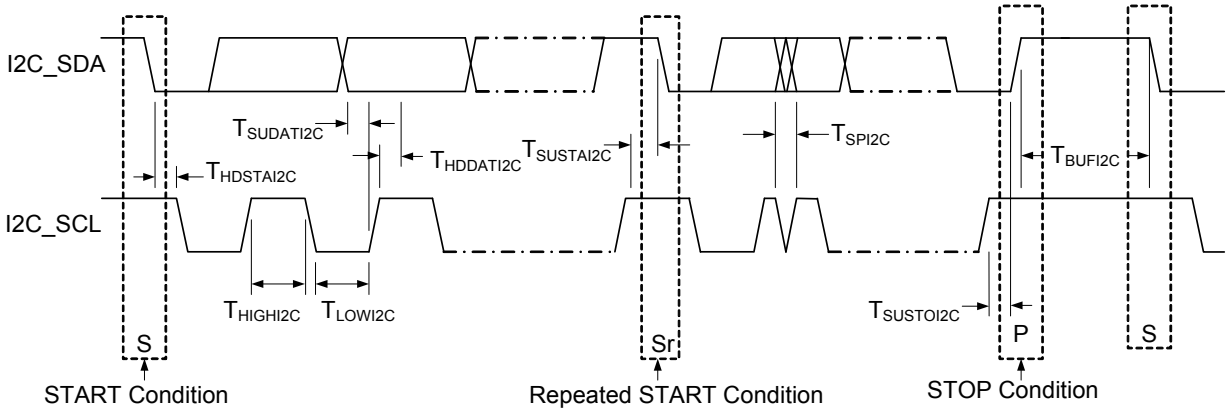
AC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.15 V to 3.5 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 26. AC Characteristics of the I²C SDA and SCL Pins for V_{DD}

Parameter	Description	Standard-Mode		Fast-Mode		Unit	Notes
		Min	Max	Min	Max		
F_{SCLI2C}	SCL clock frequency	0	100	0	400	kHz	–
$T_{HDSTAI2C}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs	–
T_{LOWI2C}	LOW period of the SCL clock	4.7	–	1.3	–	µs	–
$T_{HIGHI2C}$	HIGH period of the SCL clock	4.0	–	0.6	–	µs	–
$T_{SUSTAI2C}$	Setup time for a repeated START condition	4.7	–	0.6	–	µs	–
$T_{HDDATI2C}$	Data hold time	0	–	0	–	µs	–
$T_{SUDATI2C}$	Data setup time	250	–	100[17]	–	ns	–
$T_{SUSTOI2C}$	Setup time for STOP condition	4.0	–	0.6	–	µs	–
T_{BUFI2C}	Bus free time between a STOP and START condition	4.7	–	1.3	–	µs	–
T_{SPI2C}	Pulse width of spikes are suppressed by the input filter.	–	–	0	50	ns	–

Figure 7. Definition for Timing for Fast-/Standard-Mode on the I²C Bus



Note

17. A Fast-Mode I²C-bus device can be used in a Standard-Mode I²C-bus system, but the requirement $T_{SUDATI2C} \geq 250$ ns must then be met. This automatically is the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + T_{SUDATI2C} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I²C-bus specification) before the SCL line is released.

Thermal Impedance

Table 27. Thermal Impedance for the Package

Package	Typical θ_{JA} [18]
56-pin QFN[19]	20 °C/W
28-pin SSOP	96 °C/W

Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Table 28. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Time at Maximum Peak Temperature
56-pin QFN	260 °C	20 s
28-pin SSOP	260 °C	20 s

Notes
18. $T_J = T_A + POWER \times \theta_{JA}$
19. To achieve the thermal impedance specified for the QFN package, the center thermal pad should be soldered to the PCB ground plane.

buffer	1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for IO operations, into which data is read, or from which data is written. 2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device. 3. An amplifier used to lower the output impedance of a system.
bus	1. A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns. 2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0]. 3. One or more conductors that serve as a common connection for a group of related devices.
clock	The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks.
comparator	An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements.
compiler	A program that translates a high level language, such as C, into machine language.
configuration space	In PSoC devices, the register space accessed when the XIO bit, in the CPU_F register, is set to ‘1’.
crystal oscillator	An oscillator in which the frequency is controlled by a piezoelectric crystal. Typically a piezoelectric crystal is less sensitive to ambient temperature than other circuit components.
cyclic redundancy check (CRC)	A calculation used to detect errors in data communications, typically performed using a linear feedback shift register. Similar calculations may be used for a variety of other purposes such as data compression.
data bus	A bi-directional set of signals used by a computer to convey information from a memory location to the central processing unit and vice versa. More generally, a set of signals used to convey data between digital functions.
debugger	A hardware and software system that allows the user to analyze the operation of the system under development. A debugger usually allows the developer to step through the firmware one step at a time, set break points, and analyze memory.
dead band	A period of time when neither of two or more signals are in their active state or in transition.
digital blocks	The 8-bit logic blocks that can act as a counter, timer, serial receiver, serial transmitter, CRC generator, pseudo-random number generator, or SPI.
digital-to-analog (DAC)	A device that changes a digital signal to an analog signal of corresponding magnitude. The analog-to-digital (ADC) converter performs the reverse operation.
duty cycle	The relationship of a clock period high time to its low time, expressed as a percent.
emulator	Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system.
external reset (XRES)	An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state.

flash	An electrically programmable and erasable, non-volatile technology that provides users with the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is off.
Flash block	The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes.
frequency	The number of cycles or events per unit of time, for a periodic function.
gain	The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB.
I^2C	A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I2C uses only two bi-directional pins, clock and data, both running at +5V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode.
ICE	The in-circuit emulator that allows users to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer).
input/output (I/O)	A device that introduces data into or extracts data from a system.
interrupt	A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed.
interrupt service routine (ISR)	A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution.
jitter	1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams. 2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles.
low-voltage detect (LVD)	A circuit that senses V_{DD} and provides an interrupt to the system when V_{DD} falls lower than a selected threshold.
M8C	An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space.
master device	A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the ***slave device.***
microcontroller	An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and IO circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor.
mixed-signal	The reference to a circuit containing both analog and digital techniques and components.
modulator	A device that imposes a signal on a carrier.

noise	1. A disturbance that affects a signal and that may distort the information carried by the signal. 2. The random variations of one or more characteristics of any entity such as voltage, current, or data.
oscillator	A circuit that may be crystal controlled and is used to generate a clock frequency.
parity	A technique for testing transmitting data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity).
phase-locked loop (PLL)	An electronic circuit that controls an ***oscillator*** so that it maintains a constant phase angle relative to a reference signal.
pinouts	The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names.
port	A group of pins, usually eight.
power on reset (POR)	A circuit that forces the PSoC device to reset when the voltage is lower than a pre-set level. This is one type of hardware reset.
PSoC®	Cypress Semiconductor's PSoC® is a registered trademark and Programmable System-on-Chip™ is a trademark of Cypress.
PSoC Designer™	The software for Cypress' Programmable System-on-Chip technology.
pulse width modulator (PWM)	An output in the form of duty cycle which varies as a function of the applied measurand
RAM	An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in.
register	A storage device with a specific capacity, such as a bit or byte.
reset	A means of bringing a system back to a know state. See hardware reset and software reset.
ROM	An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in.
serial	1. Pertaining to a process in which all events occur one after the other. 2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel.
settling time	The time it takes for an output signal or value to stabilize after the input has changed from one value to another.
shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.
SRAM	An acronym for static random access memory. A memory device allowing users to store and retrieve data at a high rate of speed. The term static is used because, after a value has been loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.

Document History Page (continued)

Description Title: CY7C64215, enCoRe™ III Full-Speed USB Controller
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Rev.	ECN No.	Submission Date	Orig. of Change	Description of Change
*J	3995635	05/09/2013	CSAI	Updated Packaging Information: spec 001-12921 – Changed revision from *A to *B. spec 001-53450 – Changed revision from *B to *C. spec 51-85079 – Changed revision from *D to *E. Added Errata.
*K	4080167	07/29/2013	CSAI	Added Errata footnotes (Note 3, 5). Updated Electrical Specifications: Updated DC Electrical Characteristics: Updated DC Chip-Level Specifications: Added Note 3 and referred the same note in “Sleep Mode” in description of I_{SB} parameter in Table 7. Updated DC POR and LVD Specifications: Added Note 5 and referred the same note in V_{PPOR0}, V_{PPOR1}, V_{PPOR2} parameters in Table 15. Updated Reference Documents: Removed references of spec 001-17397 and spec 001-14503 as these specs are obsolete. Updated in new template.
*L	4247931	01/16/2014	CSAI	Updated Packaging Information: spec 001-53450 – Changed revision from *C to *D. Completing Sunset Review.
*M	4481449	08/28/2014	MVTA	Updated Packaging Information: spec 001-12921 – Changed revision from *B to *C. Updated Ordering Information (Updated part numbers). Updated in new template.

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