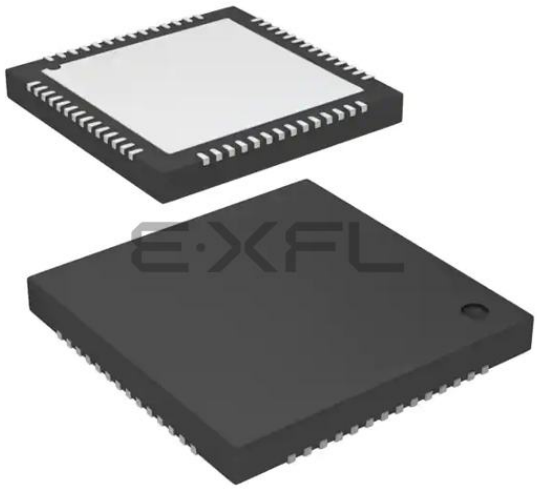

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Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	USB Microcontroller
Core Processor	M8C
Program Memory Type	FLASH (16kB)
Controller Series	CY7C642xx
RAM Size	1K x 8
Interface	I²C, USB
Number of I/O	50
Voltage - Supply	3V ~ 5.25V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	56-VFQFN Exposed Pad
Supplier Device Package	56-QFN-EP (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy7c64215-56ltxc

Applications

- PC human interface devices
  - Mouse (optomechanical, optical, trackball)
  - Keyboards
  - Joysticks
- Gaming
  - Game pads
  - Console keyboards
- General purpose
  - Barcode scanners
  - POS terminal
  - Consumer electronics
  - Toys
  - Remote controls
  - USB to serial

enCoRe III Functional Overview

The enCoRe III is based on the flexible PSoC architecture and is a full-featured, full-speed (12-Mbps) USB part. Configurable analog, digital, and interconnect circuitry enable a high level of integration in a host of consumer, and communication applications.

This architecture enables the user to create customized peripheral configurations that match the requirements of each individual application. Additionally, a fast CPU, flash program memory, SRAM data memory, and configurable I/O are included in both 28-pin SSOP and 56-pin QFN packages.

enCoRe III architecture, as illustrated in the "Block Diagram" on page 1, is comprised of four main areas: enCoRe III core, digital system, analog system, and system resources including a full-speed USB port. Configurable global busing enables all the device resources to combine into a complete custom system. The enCoRe III CY7C64215 can have up to seven I/O ports that connect to the global digital and analog interconnects, providing access to four digital blocks and six analog blocks.

enCoRe III Core

The enCoRe III Core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable GPIOs.

The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four-million instructions per second (MIPS) 8-bit Harvard-architecture microprocessor. The CPU uses an interrupt controller with up to 20 vectors, to simplify programming of real-time embedded events. Program execution is timed and protected using the included sleep and watchdog timers (WDT).

Memory encompasses 16 KB of flash for program storage, 1 KB of SRAM for data storage, and up to 2 KB of EEPROM emulated using the flash. Program flash uses four protection levels on blocks of 64 bytes, enabling customized software IP protection.

enCoRe III incorporates flexible internal clock generators, including a 24-MHz internal main oscillator (IMO) accurate to 8% over temperature and voltage as well as an option for an external clock oscillator (ECO). USB operation requires the OSC LOCK bit of the USB_CR0 register to be set to obtain IMO accuracy to.25%.

The 24-MHz IMO is doubled to 48 MHz for use by the digital system, if needed. The 48-MHz clock is required to clock the USB block and must be enabled for communication. A low-power 32-kHz internal low-speed oscillator (ILO) is provided for the sleep timer and WDT. The clocks, together with programmable clock dividers (system resource), provide flexibility to integrate almost any timing requirement into enCoRe III. In USB systems, the IMO self-tunes to ±0.25% accuracy for USB communication.

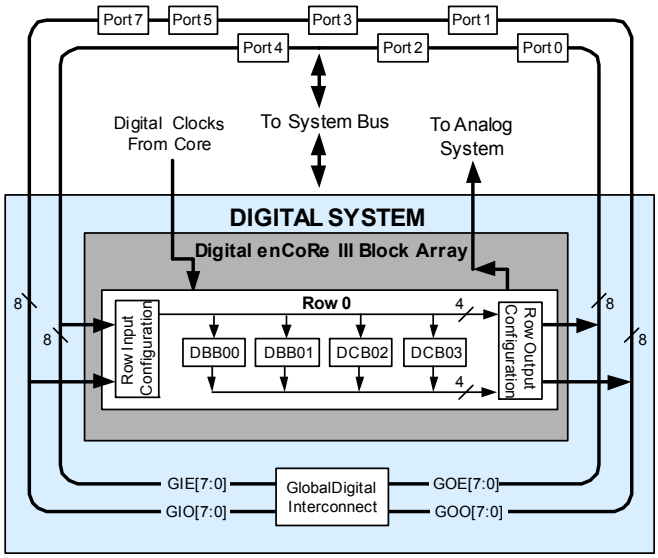
The extended temperature range for the industrial operating range (–40 °C to +85 °C) requires the use of an ECO, which is only available on the 56-pin QFN package.

enCoRe III GPIOs provide connection to the CPU, digital and analog resources of the device. Each pin's drive mode may be selected from eight options, enabling great flexibility in external interfacing. Every pin also has capability to generate a system interrupt on high-level, low-level, and change from last read.

The Digital System

The digital system is composed of four digital enCoRe III blocks. Each block is an 8-bit resource that is used alone or combined with other blocks to form 8-, 16-, 24-, and 32-bit peripherals, which are called user module references.

Figure 1. Digital System Block Diagram



The following digital configurations can be built from the blocks:

- PWMs, timers, and counters (8-bit and 16-bit)
- UART 8-bit with selectable parity
- SPI master and slave
- I^2C master
- RF interface: Interface to Cypress CYFI radio

The digital blocks are connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also enable signal multiplexing and performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

and provide program run, halt, and step control. The debugger also allows you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an online support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality in-circuit emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions.

The PSoC development process can be summarized in the following four steps:

1. Select User Modules
2. Configure User Modules
3. Organize and Connect
4. Generate, Verify, and Debug

Select Components

PSoC Designer provides a library of pre-built, pre-tested hardware peripheral components called “user modules”. User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure Components

Each of the User Modules you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more

digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the User Module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the "Generate Configuration Files" step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's Debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition

to traditional single-step, run-to-breakpoint and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

Register Reference

The register conventions specific to this section are listed in the following table.

Table 4. Register Conventions

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

Register Mapping Tables

The enCoRe III device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks, bank 0 and bank 1. The XOI bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XOI bit is set to ‘1’, the user is in bank 1.

Note In the following register mapping tables, blank fields are reserved and should not be accessed.

Absolute Maximum Ratings

Table 5. Absolute Maximum Ratings

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{STG}	Storage temperature	–55	–	+100	°C	Higher storage temperatures reduces data retention time.
$T_{BAKETEMP}$	Bake temperature	–	125	See package label	°C	–
$T_{BAKETIME}$	Bake time	See package label	–	72	Hours	–
T_A	Ambient temperature with power applied	0	–	+70	°C	–
V_{DD}	Supply voltage on V_{DD} relative to V_{SS}	–0.5	–	+6.0	V	–
V_{IO}	DC input voltage	V_{SS} – 0.5	–	V_{DD} + 0.5	V	–
V_{IO2}	DC voltage applied to tristate	V_{SS} – 0.5	–	V_{DD} + 0.5	V	–
I_{MIO}	Maximum current into any port pin	–25	–	+50	mA	–
I_{MAIO}	Maximum current into any port pin configured as an analog driver	–50	–	+50	mA	–
ESD	Electrostatic discharge voltage	2000	–	–	V	Human body model ESD.
LU	Latch up current	–	–	200	mA	–

Operating Temperature

Table 6. Operating Temperature

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{AC}	Commercial ambient temperature	0	–	+70	°C	–
T_{AI}	Industrial ambient temperature	–40	–	+85	°C	USB operation requires the use of an external clock oscillator and the 56-pin QFN package.
T_J	Junction temperature	–40	–	+100	°C	The temperature rise from ambient to junction is package specific. See “Thermal Impedance” on page 32. The user must limit the power consumption to comply with this requirement.

DC GPIO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.15 V to 3.5 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 8. DC GPIO Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	–
R_{PD}	Pull-down resistor	4	5.6	8	kΩ	–
V_{OH}	High output level	V_{DD} – 1.0	–	–	V	I_{OH} = 10 mA, V_{DD} = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 80 mA maximum combined I_{OH} budget.
V_{OL}	Low output level	–	–	0.75	V	I_{OL} = 25 mA, V_{DD} = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 150 mA maximum combined I_{OL} budget.
I_{OH}	High-level source current	10	–	–	mA	–
I_{OL}	Low-level sink current	25	–	–	mA	–
V_{IL}	Input low level	–	–	0.8	V	V_{DD} = 3.15 to 5.25.
V_{IH}	Input high level	2.1	–		V	V_{DD} = 3.15 to 5.25.
V_H	Input hysteresis	–	60	–	mV	–
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 µA.
C_{IN}	Capacitive load on pins as input	–	3.5	10	pF	Package and pin dependent. Temp = 25 °C.
C_{OUT}	Capacitive load on pins as output	–	3.5	10	pF	Package and pin dependent. Temp = 25 °C.

DC Full-Speed USB Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges when the IMO is selected as system clock: 4.75 V to 5.25 V and 0 °C ≤ T_A ≤ 70 °C, or 3.15 V to 3.5 V and 0 °C ≤ T_A ≤ 70 °C, respectively.

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges when an external clock is selected as the system clock: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.15 V to 3.5 V and –40 °C ≤ T_A ≤ 85 °C.

Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 9. DC Full Speed (12 Mbps) USB Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
USB Interface						
V_{DI}	Differential input sensitivity	0.2	–	–	V	| (D+) – (D–) |
V_{CM}	Differential input common mode range	0.8	–	2.5	V	–
V_{SE}	Single-ended receiver threshold	0.8	–	2.0	V	–
C_{IN}	Transceiver capacitance	–	–	20	pF	–
I_{IO}	High Z state data line leakage	–10	–	10	µA	0 V < V_{IN} < 3.3 V.
R_{EXT}	External USB series resistor	23	–	25	Ω	In series with each USB pin.
V_{UOH}	Static output high, driven	2.8	–	3.6	V	15 kΩ ± 5% to ground. Internal pull-up enabled.
V_{UOHI}	Static output high, idle	2.7	–	3.6	V	15 kΩ ± 5% to ground. Internal pull-up enabled.
V_{UOL}	Static output low	–	–	0.3	V	15 kΩ ± 5% to ground. Internal pull-up enabled.
Z_O	USB driver output impedance	28	–	44	Ω	Including R_{EXT} resistor.
V_{CRS}	D+/D– crossover voltage	1.3	–	2.0	V	–

DC Analog Reference Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.15 V to 3.5 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

The guaranteed specifications are measured through the analog continuous time PSoC blocks. The power levels for AGND refer to the power of the Analog Continuous Time PSoC block. The power levels for RefHi and RefLo refer to the Analog Reference Control register. The limits stated for AGND include the offset error of the AGND buffer local to the Analog Continuous Time PSoC block. Reference control power is high.

Table 12. 5-V DC Analog Reference Specifications

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b000	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.229	$V_{DD}/2$ + 1.290	$V_{DD}/2$ + 1.346	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.038	$V_{DD}/2$	$V_{DD}/2$ + 0.040	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.356	$V_{DD}/2$ – 1.295	$V_{DD}/2$ – 1.218	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.220	$V_{DD}/2$ + 1.292	$V_{DD}/2$ + 1.348	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.036	$V_{DD}/2$	$V_{DD}/2$ + 0.036	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.357	$V_{DD}/2$ – 1.297	$V_{DD}/2$ – 1.225	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.221	$V_{DD}/2$ + 1.293	$V_{DD}/2$ + 1.351	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.036	$V_{DD}/2$	$V_{DD}/2$ + 0.036	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.357	$V_{DD}/2$ – 1.298	$V_{DD}/2$ – 1.228	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	$V_{DD}/2$ + Bandgap	$V_{DD}/2$ + 1.219	$V_{DD}/2$ + 1.293	$V_{DD}/2$ + 1.353	V
		V_{AGND}	AGND	$V_{DD}/2$	$V_{DD}/2$ – 0.037	$V_{DD}/2$ – 0.001	$V_{DD}/2$ + 0.036	V
		V_{REFLO}	Ref Low	$V_{DD}/2$ – Bandgap	$V_{DD}/2$ – 1.359	$V_{DD}/2$ – 1.299	$V_{DD}/2$ – 1.229	V
0b001	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.092	P2[4] + P2[6] – 0.011	P2[4] + P2[6] + 0.064	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.031	P2[4] – P2[6] + 0.007	P2[4] – P2[6] + 0.056	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.078	P2[4] + P2[6] – 0.008	P2[4] + P2[6] + 0.063	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.031	P2[4] – P2[6] + 0.004	P2[4] – P2[6] + 0.043	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.073	P2[4] + P2[6] – 0.006	P2[4] + P2[6] + 0.062	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.032	P2[4] – P2[6] + 0.003	P2[4] – P2[6] + 0.038	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	P2[4]+P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] + P2[6] – 0.073	P2[4] + P2[6] – 0.006	P2[4] + P2[6] + 0.062	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4]–P2[6] (P2[4] = $V_{DD}/2$, P2[6] = 1.3 V)	P2[4] – P2[6] – 0.034	P2[4] – P2[6] + 0.002	P2[4] – P2[6] + 0.037	V

DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.15 V to 3.5 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Note The bits PORLEV and VM in the following table refer to bits in the VLT_CR register. See the *PSoC® Technical Reference Manual* for more information on the VLT_CR register.

Table 15. DC POR and LVD Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{PPOR0R} [5] V_{PPOR1R} [5] V_{PPOR2R} [5]	V_{DD} value for PPOR trip (positive ramp) PORLEV[1:0] = 00b PORLEV[1:0] = 01b PORLEV[1:0] = 10b	 – –	 2.91 4.39 4.55	 – –	 V V V	–
V_{PPOR0} V_{PPOR1} V_{PPOR2}	V_{DD} value for PPOR trip (negative ramp) PORLEV[1:0] = 00b PORLEV[1:0] = 01b PORLEV[1:0] = 10b	 – –	 2.82 4.39 4.55	 – –	 V V V	–
V_{PH0} V_{PH1} V_{PH2}	PPOR hysteresis PORLEV[1:0] = 00b PORLEV[1:0] = 01b PORLEV[1:0] = 10b	 – – –	 92 0 0	 – – –	 mV mV mV	–
V_{LVD0} V_{LVD1} V_{LVD2} V_{LVD3} V_{LVD4} V_{LVD5} V_{LVD6} V_{LVD7}	V_{DD} value for LVD trip VM[2:0] = 000b VM[2:0] = 001b VM[2:0] = 010b VM[2:0] = 011b VM[2:0] = 100b VM[2:0] = 101b VM[2:0] = 110b VM[2:0] = 111b	 2.86 2.96 3.07 3.92 4.39 4.55 4.63 4.72	 2.92 3.02 3.13 4.00 4.48 4.64 4.73 4.81	 2.98[6] 3.08 3.20 4.08 4.57 4.74[7] 4.82 4.91	 V V V V V V V V	–

Notes
5. Errata: When VDD of the device is pulled below ground just before power on, the first read from each 8K Flash page may be corrupted. This issue does not affect Flash page 0 because it is the selected page upon reset. For more details in Errata on page 40.
6. Always greater than 50 mV above PPOR (PORLEV = 00) for falling supply.
7. Always greater than 50 mV above PPOR (PORLEV = 10) for falling supply.

DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.15 V to 3.5 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 16. DC Programming Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{DDP}	V_{DD} for programming and erase	4.5	5.0	5.5	V	This specification applies to the functional requirements of external programmer tools
V_{DDLV}	Low V_{DD} for verify	3.0	3.1	3.2	V	This specification applies to the functional requirements of external programmer tools
V_{DDHV}	High V_{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools
$V_{DDIWRITE}$	Supply voltage for flash write operation	3.15	–	5.25	V	This specification applies to this device when it is executing internal flash writes
I_{DDP}	Supply current during programming or verify	–	15	30	mA	–
V_{ILP}	Input low voltage during programming or verify	–	–	0.8	V	–
V_{IHP}	Input high voltage during programming or Verify	2.1	–	–	V	–
I_{ILP}	Input current when applying Vilp to P1[0] or P1[1] during programming or verify	–	–	0.2	mA	Driving internal pull-down resistor.
I_{IHP}	Input current when applying Vihp to P1[0] or P1[1] during programming or verify	–	–	1.5	mA	Driving internal pull-down resistor.
V_{OLV}	Output low voltage during programming or verify	–	–	V_{SS} + 0.75	V	–
V_{OHV}	Output high voltage during programming or verify	V_{DD} – 1.0	–	V_{DD}	V	–
$Flash_{ENPB}$	Flash endurance (per block)	50,000[8]	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash endurance (total)[9]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash data retention	10	–	–	Years	–

DC I^2C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.15 V to 3.5 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 17. DC I^2C Specifications [10]

Symbol	Description	Min	Typ	Max	Units	Notes
V_{ILI2C}	Input low level	–	–	0.3 × V_{DD}	V	3.15 V ≤ V_{DD} ≤ 3.6 V
		–	–	0.25 × V_{DD}	V	4.75 V ≤ V_{DD} ≤ 5.25 V
V_{IHI2C}	Input high level	0.7 × V_{DD}	–	–	V	3.15 V ≤ V_{DD} ≤ 5.25 V

Notes

8. The 50,000 cycle Flash endurance per block will only be guaranteed if the Flash is operating within one voltage range. Voltage ranges are 3.0V to 3.6V and 4.75V to 5.25V.
9. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).
   For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs application note AN2015 for more information.
10. All GPIOs meet the DC GPIO V_{IL} and V_{IH} specifications found in the DC GPIO Specifications sections. The I^2C GPIO pins also meet the mentioned specifications.

AC Electrical Characteristics

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.15 V to 3.5 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 18. AC Chip-Level Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
$F_{IMO245V}$	IMO frequency for 24 MHz (5 V)	23.04	24	24.96[11, 12]	MHz	Trimmed for 5 V operation using factory trim values.
$F_{IMO243V}$	IMO frequency for 24 MHz (3.3 V)	22.08	24	25.92[11,13]	MHz	Trimmed for 3.3 V operation using factory trim values.
F_{IMOUSB}	IMO frequency with USB frequency locking enabled and USB traffic present	23.94	24	24.06[12]	MHz	USB operation for system clock source from the IMO is limited to 0°C ≤ T_A ≤ 70°C.
F_{CPU1}	CPU frequency (5 V nominal)	0.090	24	24.96[11,12]	MHz	SLIMO mode = 0.
F_{CPU2}	CPU frequency (3.3 V nominal)	0.086	12	12.96[12,13]	MHz	SLIMO mode = 0.
F_{BLK5}	Digital PSoC block frequency (5 V nominal)	0	48	49.92[11,12,14]	MHz	Refer to the AC Digital Block Specifications on page 26.
F_{BLK3}	Digital PSoC block frequency (3.3 V nominal)	0	24	25.92[12,14]	MHz	–
F_{32K1}	ILO frequency	15	32	64	kHz	–
F_{32K_U}	ILO untrimmed frequency	5	–	100	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference Manual for details on this timing.
DC_{ILO}	ILO duty cycle	20	50	80	%	–
DC_{24M}	24-MHz duty cycle	40	50	60	%	–
Step24M	24-MH trim step size	–	50	–	kHz	–
Fout48M	48-MHz output frequency	46.08	48.0	49.92[11,13]	MHz	Trimmed. Utilizing factory trim values.
F_{MAX}	Maximum frequency of signal on row input or row output	–	–	12.96	MHz	–
SR_{POWER_UP}	Power supply slew rate	–	–	250	V/ms	–
$T_{POWERUP}$	Time from end of POR to CPU executing code	–	16	100	ms	–
T_{jit_IMO}[15]	24 MHz IMO cycle-to-cycle jitter (RMS)	–	200	1200	ps	
	24 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	900	6000	ps	N = 32.
	24 MHz IMO period jitter (RMS)	–	200	900	ps	

Notes

11. 4.75 V < V_{DD} < 5.25 V.
12. Accuracy derived from Internal Main Oscillator with appropriate trim for V_{DD} range.
13. 3.0 V < V_{DD} < 3.6 V. See application note AN2012 “Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation” for information on trimming for operation at 3.3 V.
14. See the individual user module data sheets for information on maximum frequencies for user modules.
15. Refer to Cypress Jitter Specifications application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 for more information.

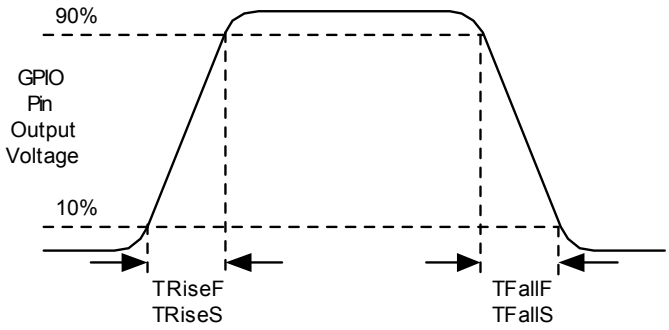
AC GPIO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.15 V to 3.5 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 19. AC GPIO Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
F_{GPIO}	GPIO operating frequency	0	–	12	MHz	Normal Strong Mode
TRiseF	Rise time, normal strong mode, Cload = 50 pF	3	–	18	ns	V_{DD} = 4.5 to 5.25 V, 10%–90%
TFallF	Fall time, normal strong mode, Cload = 50 pF	2	–	18	ns	V_{DD} = 4.5 to 5.25 V, 10%–90%
TRiseS	Rise time, slow strong mode, Cload = 50 pF	10	27	–	ns	V_{DD} = 3 to 5.25 V, 10%–90%
TFallS	Fall time, slow strong mode, Cload = 50 pF	10	22	–	ns	V_{DD} = 3 to 5.25 V, 10%–90%

Figure 6. GPIO Timing Diagram



AC Full Speed USB Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.15 V to 3.5 V and –40 °C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 20. AC Full-Speed (12 Mbps) USB Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{RFS}	Transition rise time	4	–	20	ns	For 50-pF load.
T_{FSS}	Transition fall time	4	–	20	ns	For 50-pF load.
T_{RFMFS}	Rise/fall time matching: (T_R/T_F)	90	–	111	%	For 50-pF load.
$T_{DRATEFS}$	Full-speed data rate	12 – 0.25%	12	12 + 0.25%	Mbps	–

AC External Clock Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.15 V to 3.5 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 22. AC External Clock Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
F_{OSCEXT}	Frequency for USB applications	23.94	24	24.06	MHz	USB operation in the extended Industrial temperature range (–40 °C ≤ T_A ≤ 85 °C) requires that the system clock is sourced from an external clock oscillator.
–	Duty cycle	47	50	53	%	–
–	Power-up to IMO switch	150	–	–	µs	–

AC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.15 V to 3.5 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 23. 5 V AC Analog Output Buffer Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{ROB}	Rising settling time to 0.1%, 1 V Step, 100-pF load Power = low Power = high	 – –	 – –	 2.5 2.5	 µs µs	–
T_{SOB}	Falling settling time to 0.1%, 1 V Step, 100-pF load Power = low Power = high	 – –	 – –	 2.2 2.2	 µs µs	–
SR_{ROB}	Rising slew rate (20% to 80%), 1 V Step, 100-pF load Power = low Power = high	 0.65 0.65	 – –	 – –	 V/µs V/µs	–
SR_{FOB}	Falling slew rate (80% to 20%), 1 V Step, 100-pF load Power = low Power = high	 0.65 0.65	 – –	 – –	 V/µs V/µs	–
BW_{OBSS}	Small signal bandwidth, 20 mV_{pp}, 3-dB BW, 100-pF load Power = low Power = high	 0.8 0.8	 – –	 – –	 MHz MHz	–
BW_{OBLS}	Large signal bandwidth, 1 V_{pp}, 3-dB BW, 100-pF load Power = low Power = high	 300 300	 – –	 – –	 kHz kHz	–

Table 24. 3.3 V AC Analog Output Buffer Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{ROB}	Rising settling time to 0.1%, 1 V Step, 100-pF load Power = low Power = high	 – –	 – –	 3.8 3.8	 µs µs	–
T_{SOB}	Falling settling time to 0.1%, 1 V Step, 100-pF load Power = low Power = high	 – –	 – –	 2.6 2.6	 µs µs	–
SR_{ROB}	Rising slew rate (20% to 80%), 1 V Step, 100-pF load Power = low Power = high	 0.5 0.5	 – –	 – –	 V/µs V/µs	–
SR_{FOB}	Falling slew rate (80% to 20%), 1 V Step, 100-pF load Power = low Power = high	 0.5 0.5	 – –	 – –	 V/µs V/µs	–
BW_{OBSS}	Small signal bandwidth, 20 mV_{pp}, 3dB BW, 100-pF load Power = low Power = high	 0.7 0.7	 – –	 – –	 MHz MHz	–
BW_{OBLS}	Large signal bandwidth, 1 V_{pp}, 3dB BW, 100-pF load Power = low Power = high	 200 200	 – –	 – –	 kHz kHz	–

Figure 9. 56-pin QFN (8 × 8 × 1.0 mm) 4.5 × 5.2 E-Pad (Sawn) Package Outline, 001-53450

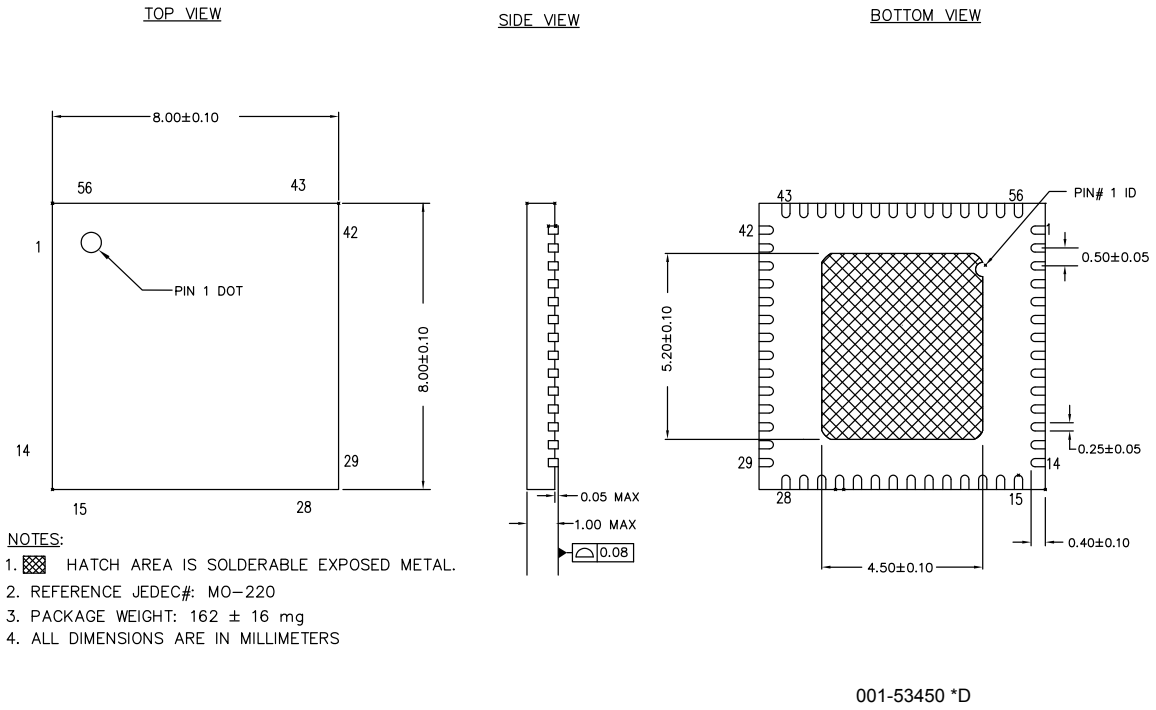
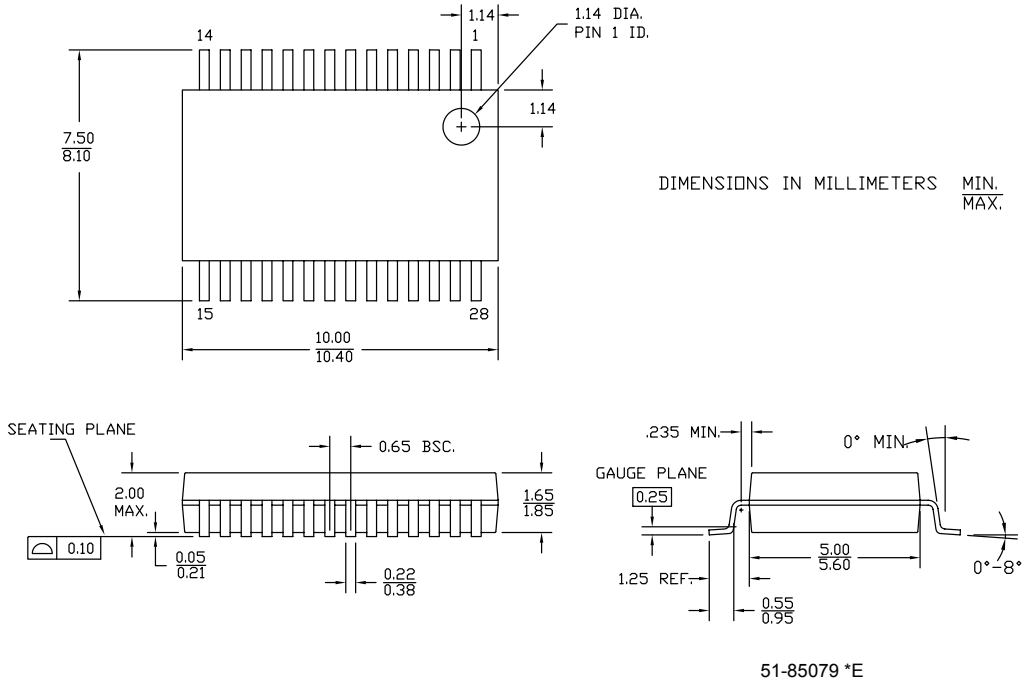


Figure 10. 28-pin SSOP (210 Mils) Package Outline, 51-85079



Thermal Impedance

Table 27. Thermal Impedance for the Package

Package	Typical θ_{JA} [18]
56-pin QFN[19]	20 °C/W
28-pin SSOP	96 °C/W

Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Table 28. Solder Reflow Peak Temperature

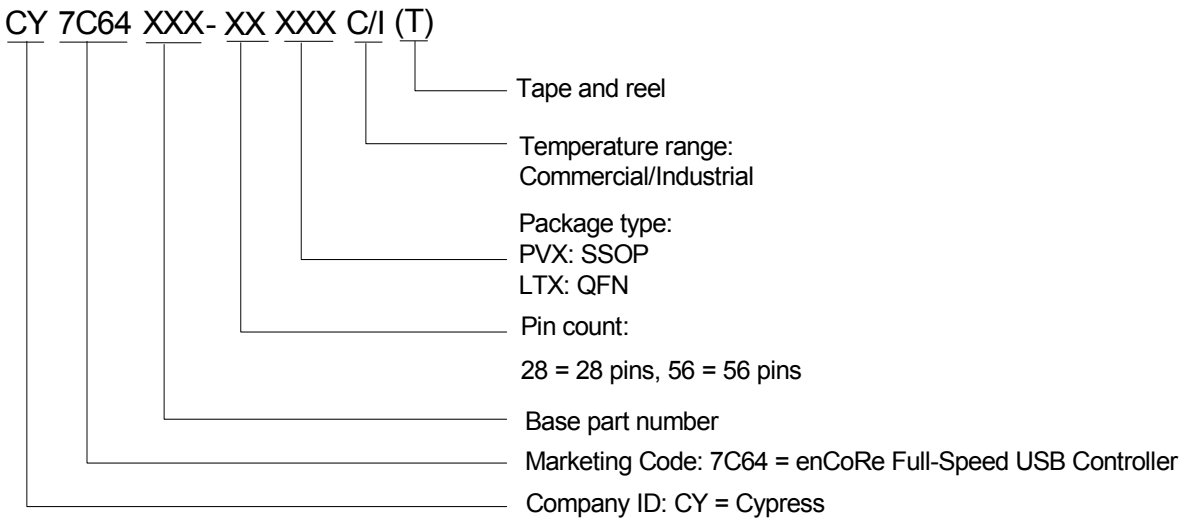
Package	Maximum Peak Temperature	Time at Maximum Peak Temperature
56-pin QFN	260 °C	20 s
28-pin SSOP	260 °C	20 s

Notes
18. $T_J = T_A + POWER \times \theta_{JA}$
19. To achieve the thermal impedance specified for the QFN package, the center thermal pad should be soldered to the PCB ground plane.

Ordering Information

Package	Ordering Code	Flash Size	SRAM (Bytes)	Temperature Range
28-pin SSOP	CY7C64215-28PVXC	16K	1K	Commercial, 0 °C to 70 °C
28-pin SSOP (Tape and Reel)	CY7C64215-28PVXCT	16K	1K	Commercial, 0 °C to 70 °C
28-pin SSOP	CY7C64215-28PVXI	16 K	1K	Industrial, –40 °C to 85 °C
28-pin SSOP (Tape and Reel)	CY7C64215-28PVXIT	16 K	1K	Industrial, –40 °C to 85 °C
56-pin QFN (Sawn)	CY7C64215-56LTXC	16K	1K	Commercial, 0 °C to 70 °C
56-pin QFN (Sawn) (Tape and Reel)	CY7C64215-56LTXCT	16K	1K	Commercial, 0 °C to 70 °C
56-pin QFN (Sawn)	CY7C64215-56LTXI	16K	1K	Industrial, –40 °C to 85 °C
56-pin QFN (Sawn) (Tape and Reel)	CY7C64215-56LTXIT	16K	1K	Industrial, –40 °C to 85 °C

Ordering Code Definitions



flash	An electrically programmable and erasable, non-volatile technology that provides users with the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is off.
Flash block	The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes.
frequency	The number of cycles or events per unit of time, for a periodic function.
gain	The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB.
I^2C	A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I2C uses only two bi-directional pins, clock and data, both running at +5V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode.
ICE	The in-circuit emulator that allows users to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer).
input/output (I/O)	A device that introduces data into or extracts data from a system.
interrupt	A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed.
interrupt service routine (ISR)	A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution.
jitter	1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams. 2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles.
low-voltage detect (LVD)	A circuit that senses V_{DD} and provides an interrupt to the system when V_{DD} falls lower than a selected threshold.
M8C	An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space.
master device	A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the ***slave device.***
microcontroller	An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and IO circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor.
mixed-signal	The reference to a circuit containing both analog and digital techniques and components.
modulator	A device that imposes a signal on a carrier.

SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal.
tri-state	A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.
UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.
user modules	Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level ***API (Application Programming Interface)*** for the peripheral function.
user space	The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.
V_{DD}	A name for a power net meaning “voltage drain.” The most positive power supply signal. Usually 5 V or 3.3 V.
V_{SS}	A name for a power net meaning “voltage source.” The most negative power supply signal.
watchdog timer	A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.

Errata

This section describes the errata for the enCoRe III CY7C64215 device. The information in this document describes hardware issues associated with Silicon Revision A.

Contact your local Cypress sales representative if you have questions.

Part Numbers Affected

Part Number	Silicon Revision
CY7C64215	A

CY7C64215 Qualification Status

Product Status: In Production

CY7C64215 Errata Summary

This table defines the errata applicability to available enCoRe III CY7C64215 family devices.

Items	Part Number	Silicon Revision	Fix Status
USB interface DP line pulses low when the enCoRe III device wakes from sleep.	CY7C64215	A	No silicon fix planned. Use workaround.
Invalid flash reads may occur if V_{DD} is pulled to –0.5 V just before power on.	CY7C64215	A	
PMA Index Register fails to auto-increment with CPU_Clock set to SysClk/1 (24 MHz).	CY7C64215	A	

1. USB interface DP line pulses low when the enCoRe III device wakes from sleep

■ Problem Definition

When the device operates at 4.75 V to 5.25 V and the 3.3-V regulator is enabled, a short low pulse may be created on the DP signal line during device wakeup. The 15- to 20-µs low pulse of the DP line may be interpreted by the host computer as a deattach or the beginning of a wakeup.

■ Parameters Affected

The bandgap reference voltage used by the 3.3-V regulator decreases during sleep due to leakage. Upon device wakeup, the bandgap is re-enabled and, after a delay for settling, the 3.3-V regulator is enabled. On some devices the 3.3-V regulator used to generate the USB DP signal may be enabled before the bandgap is fully stabilized. This can cause a low pulse on the regulator output and DP signal line until the bandgap stabilizes. In applications where V_{DD} is 3.3 V, the regulator is not used and, therefore, the DP low pulse is not generated.

■ Trigger Condition

N/A

■ Scope of Impact

N/A

■ Workaround

To prevent the DP signal from pulsing low, keep the bandgap enabled during sleep. The most efficient method is to set the No Buzz bit in the OSC_CR0 register. The No Buzz bit keeps the bandgap powered and output stable during sleep. Setting the No Buzz bit results in a nominal 100 µA increase in sleep current. Leaving the analog reference block enabled during sleep also resolves this issue because it forces the bandgap to remain enabled. The following example shows how to disable the No Buzz bit:

Assembly

```
M8C_SetBank1
or    reg[OSC_CR0], 0x20
M8C_SetBank0
```

C

```
OSC_CR0 |= 0x20;
```

■ **Fix Status**

There is no planned silicon fix; use workaround.

2. Invalid flash reads may occur if V_{DD} is pulled to –0.5 V just before power on

■ **Problem Definition**

When V_{DD} of the device is pulled below ground just before power on, the first read from each 8-KB flash page may be corrupted. This issue does not affect flash page 0 because it is the selected page upon reset.

■ **Parameters Affected**

When V_{DD} is pulled below ground before power on, an internal flash reference may deviate from its nominal voltage. The reference deviation tends to result in the first flash read from that page returning 0xFF. During the first read from each page, the reference is reset resulting in all future reads returning the correct value. A short delay of 5 µs before the first real read provides time for the reference voltage to stabilize.

■ **Trigger Condition**

N/A

■ **Scope of Impact**

N/A

■ **Workaround**

To prevent an invalid flash read, a dummy read from each flash page must occur before use of the pages. A delay of 5 µs must occur after the dummy read and before a real read. The dummy reads occur as soon as possible and must be located in flash page 0 before a read from any other flash page. An example for reading a byte of memory from each flash page is listed below. Place it in *boot.tpl* and *boot.asm* immediately after the ‘start:’ label.

```
// dummy read from each 8K Flash page
// page 1
movA, 0x20       // MSB
movX, 0x00       // LSB
romx
// wait at least 5 µs
movX, 14
loop1:
decX
jnzloop1
```

■ **Fix Status**

There is no planned silicon fix; use workaround.

3. PMA Index Register fails to auto-increment with CPU_Clock set to SysClk/1 (24 MHz)

■ **Problem Definition**

When the device operates at 4.75 V to 5.25 V and the CPU_Clock is set to SysClk/1 (24 MHz), the USB PMA Index Register may fail to increment automatically when used in an OUT endpoint configuration at full-speed. When the application program attempts to use the bReadOutEP() function, the first byte in the PMA buffer is always returned.

■ **Parameters Affected**

An internal flip-flop hold problem is associated with the index register increment function. All reads of the associated RAM originate from the first byte. The hold problem has no impact on other circuits or functions within the device.

■ **Trigger Condition**

N/A

■ **Scope of Impact**

N/A

Document History Page (continued)

Description Title: CY7C64215, enCoRe™ III Full-Speed USB Controller
Document Number: 38-08036

Rev.	ECN No.	Submission Date	Orig. of Change	Description of Change
*J	3995635	05/09/2013	CSAI	Updated Packaging Information: spec 001-12921 – Changed revision from *A to *B. spec 001-53450 – Changed revision from *B to *C. spec 51-85079 – Changed revision from *D to *E. Added Errata.
*K	4080167	07/29/2013	CSAI	Added Errata footnotes (Note 3, 5). Updated Electrical Specifications: Updated DC Electrical Characteristics: Updated DC Chip-Level Specifications: Added Note 3 and referred the same note in “Sleep Mode” in description of I_{SB} parameter in Table 7. Updated DC POR and LVD Specifications: Added Note 5 and referred the same note in V_{PPOR0}, V_{PPOR1}, V_{PPOR2} parameters in Table 15. Updated Reference Documents: Removed references of spec 001-17397 and spec 001-14503 as these specs are obsolete. Updated in new template.
*L	4247931	01/16/2014	CSAI	Updated Packaging Information: spec 001-53450 – Changed revision from *C to *D. Completing Sunset Review.
*M	4481449	08/28/2014	MVTA	Updated Packaging Information: spec 001-12921 – Changed revision from *B to *C. Updated Ordering Information (Updated part numbers). Updated in new template.

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