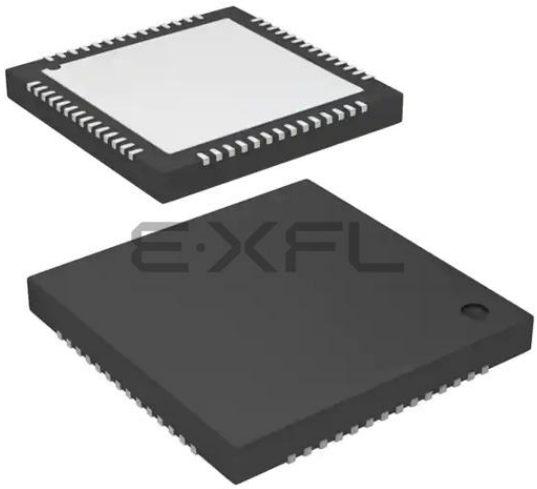

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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	USB Microcontroller
Core Processor	M8C
Program Memory Type	FLASH (16kB)
Controller Series	CY7C642xx
RAM Size	1K x 8
Interface	I²C, USB
Number of I/O	50
Voltage - Supply	3V ~ 5.25V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	56-VFQFN Exposed Pad
Supplier Device Package	56-QFN-EP (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy7c64215-56ltxct

Contents

Applications

- PC human interface devices
  - Mouse (optomechanical, optical, trackball)
  - Keyboards
  - Joysticks
- Gaming
  - Game pads
  - Console keyboards
- General purpose
  - Barcode scanners
  - POS terminal
  - Consumer electronics
  - Toys
  - Remote controls
  - USB to serial

enCoRe III Functional Overview

The enCoRe III is based on the flexible PSoC architecture and is a full-featured, full-speed (12-Mbps) USB part. Configurable analog, digital, and interconnect circuitry enable a high level of integration in a host of consumer, and communication applications.

This architecture enables the user to create customized peripheral configurations that match the requirements of each individual application. Additionally, a fast CPU, flash program memory, SRAM data memory, and configurable I/O are included in both 28-pin SSOP and 56-pin QFN packages.

enCoRe III architecture, as illustrated in the "Block Diagram" on page 1, is comprised of four main areas: enCoRe III core, digital system, analog system, and system resources including a full-speed USB port. Configurable global busing enables all the device resources to combine into a complete custom system. The enCoRe III CY7C64215 can have up to seven I/O ports that connect to the global digital and analog interconnects, providing access to four digital blocks and six analog blocks.

enCoRe III Core

The enCoRe III Core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable GPIOs.

The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four-million instructions per second (MIPS) 8-bit Harvard-architecture microprocessor. The CPU uses an interrupt controller with up to 20 vectors, to simplify programming of real-time embedded events. Program execution is timed and protected using the included sleep and watchdog timers (WDT).

Memory encompasses 16 KB of flash for program storage, 1 KB of SRAM for data storage, and up to 2 KB of EEPROM emulated using the flash. Program flash uses four protection levels on blocks of 64 bytes, enabling customized software IP protection.

enCoRe III incorporates flexible internal clock generators, including a 24-MHz internal main oscillator (IMO) accurate to 8% over temperature and voltage as well as an option for an external clock oscillator (ECO). USB operation requires the OSC LOCK bit of the USB_CR0 register to be set to obtain IMO accuracy to.25%.

The 24-MHz IMO is doubled to 48 MHz for use by the digital system, if needed. The 48-MHz clock is required to clock the USB block and must be enabled for communication. A low-power 32-kHz internal low-speed oscillator (ILO) is provided for the sleep timer and WDT. The clocks, together with programmable clock dividers (system resource), provide flexibility to integrate almost any timing requirement into enCoRe III. In USB systems, the IMO self-tunes to ±0.25% accuracy for USB communication.

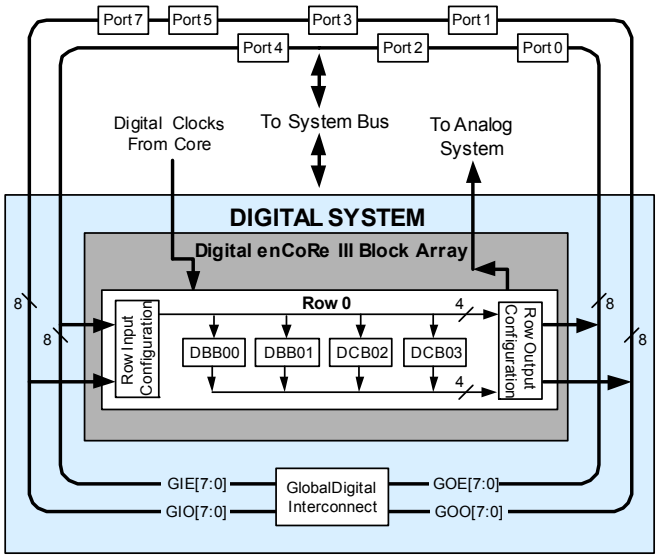
The extended temperature range for the industrial operating range (–40 °C to +85 °C) requires the use of an ECO, which is only available on the 56-pin QFN package.

enCoRe III GPIOs provide connection to the CPU, digital and analog resources of the device. Each pin's drive mode may be selected from eight options, enabling great flexibility in external interfacing. Every pin also has capability to generate a system interrupt on high-level, low-level, and change from last read.

The Digital System

The digital system is composed of four digital enCoRe III blocks. Each block is an 8-bit resource that is used alone or combined with other blocks to form 8-, 16-, 24-, and 32-bit peripherals, which are called user module references.

Figure 1. Digital System Block Diagram



The following digital configurations can be built from the blocks:

- PWMs, timers, and counters (8-bit and 16-bit)
- UART 8-bit with selectable parity
- SPI master and slave
- I^2C master
- RF interface: Interface to Cypress CYFI radio

The digital blocks are connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also enable signal multiplexing and performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Pin Information

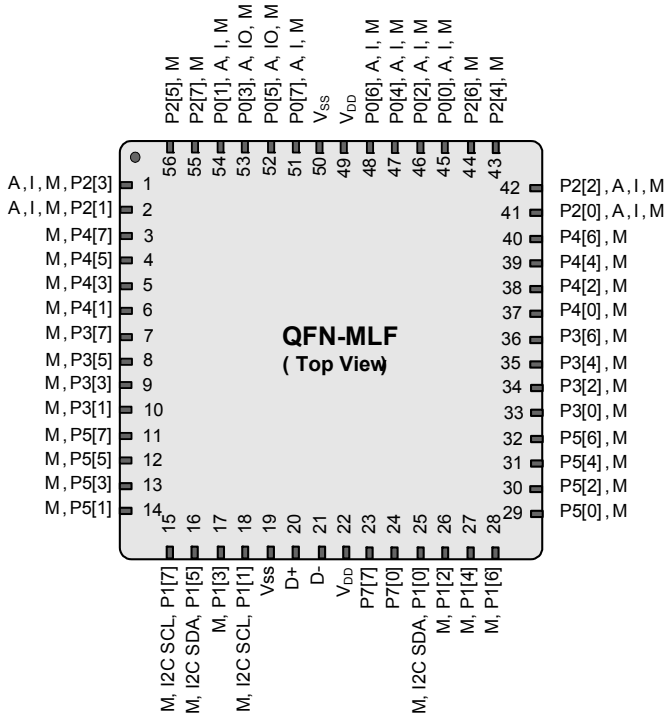
56-Pin Part Pinout

The CY7C64215 enCoRe III device is available in a 56-pin package which is listed and illustrated in the following table. Every port pin (labeled “P”) is capable of digital I/O. However, V_{SS} and V_{DD} are not capable of digital I/O.

Table 2. 56-Pin Part Pinout (QFN-MLF SAWN)[1]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I, M	P2[3]	Direct switched capacitor block input.
2	I/O	I, M	P2[1]	Direct switched capacitor block input.
3	I/O	M	P4[7]	
4	I/O	M	P4[5]	
5	I/O	M	P4[3]	
6	I/O	M	P4[1]	
7	I/O	M	P3[7]	
8	I/O	M	P3[5]	
9	I/O	M	P3[3]	
10	I/O	M	P3[1]	
11	I/O	M	P5[7]	
12	I/O	M	P5[5]	
13	I/O	M	P5[3]	
14	I/O	M	P5[1]	
15	I/O	M	P1[7]	I^2C serial clock (SCL).
16	I/O	M	P1[5]	I^2C serial data (SDA).
17	I/O	M	P1[3]	
18	I/O	M	P1[1]	I^2C SCL, ISSP-SCLK.
19	Power		V_{SS}	Ground connection.
20	USB		D+	
21	USB		D-	
22	Power		V_{DD}	Supply voltage.
23	I/O		P7[7]	
24	I/O		P7[0]	
25	I/O	M	P1[0]	I^2C SDA, ISSP-SDATA.
26	I/O	M	P1[2]	
27	I/O	M	P1[4]	Optional external clock input EXTCLK.
28	I/O	M	P1[6]	
29	I/O	M	P5[0]	
30	I/O	M	P5[2]	
31	I/O	M	P5[4]	
32	I/O	M	P5[6]	
33	I/O	M	P3[0]	
34	I/O	M	P3[2]	
35	I/O	M	P3[4]	
36	I/O	M	P3[6]	
37	I/O	M	P4[0]	
38	I/O	M	P4[2]	
39	I/O	M	P4[4]	
40	I/O	M	P4[6]	
41	I/O	I, M	P2[0]	Direct switched capacitor block input.
42	I/O	I, M	P2[2]	Direct switched capacitor block input.
43	I/O	M	P2[4]	External analog ground (AGND) input.
44	I/O	M	P2[6]	External voltage reference (VREF) input.
45	I/O	I, M	P0[0]	Analog column mux input.
46	I/O	I, M	P0[2]	Analog column mux input and column output.
47	I/O	I, M	P0[4]	Analog column mux input and column output.
48	I/O	I, M	P0[6]	Analog column mux input.
49	Power		V_{DD}	Supply voltage.
50	Power		V_{SS}	Ground connection.
51	I/O	I, M	P0[7]	Analog column mux input.
52	I/O	I/O, M	P0[5]	Analog column mux input and column output
53	I/O	I/O, M	P0[3]	Analog column mux input and column output.
54	I/O	I, M	P0[1]	Analog column mux input.
55	I/O	M	P2[7]	
56	I/O	M	P2[5]	

Figure 3. CY7C64215 56-Pin enCoRe III Device



LEGEND A = Analog, I = Input, O = Output, and M = Analog Mux Input.

Note
1. The center pad on the QFN-MLF package should be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal.

Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW	PMA0_DR	40	RW	ASC10CR0	80	RW		C0	
PRT0IE	01	RW	PMA1_DR	41	RW	ASC10CR1	81	RW		C1	
PRT0GS	02	RW	PMA2_DR	42	RW	ASC10CR2	82	RW		C2	
PRT0DM2	03	RW	PMA3_DR	43	RW	ASC10CR3	83	RW		C3	
PRT1DR	04	RW	PMA4_DR	44	RW	ASD11CR0	84	RW		C4	
PRT1IE	05	RW	PMA5_DR	45	RW	ASD11CR1	85	RW		C5	
PRT1GS	06	RW	PMA6_DR	46	RW	ASD11CR2	86	RW		C6	
PRT1DM2	07	RW	PMA7_DR	47	RW	ASD11CR3	87	RW		C7	
PRT2DR	08	RW	USB_SOF0	48	R		88			C8	
PRT2IE	09	RW	USB_SOF1	49	R		89			C9	
PRT2GS	0A	RW	USB_CR0	4A	RW		8A			CA	
PRT2DM2	0B	RW	USBIO_CR0	4B	#		8B			CB	
PRT3DR	0C	RW	USBIO_CR1	4C	RW		8C			CC	
PRT3IE	0D	RW		4D			8D			CD	
PRT3GS	0E	RW	EP1_CNT1	4E	#		8E			CE	
PRT3DM2	0F	RW	EP1_CNT	4F	RW		8F			CF	
PRT4DR	10	RW	EP2_CNT1	50	#	ASD20CR0	90	RW	CUR_PP	D0	RW
PRT4IE	11	RW	EP2_CNT	51	RW	ASD20CR1	91	RW	STK_PP	D1	RW
PRT4GS	12	RW	EP3_CNT1	52	#	ASD20CR2	92	RW		D2	
PRT4DM2	13	RW	EP3_CNT	53	RW	ASD20CR3	93	RW	IDX_PP	D3	RW
PRT5DR	14	RW	EP4_CNT1	54	#	ASC21CR0	94	RW	MVR_PP	D4	RW
PRT5IE	15	RW	EP4_CNT	55	RW	ASC21CR1	95	RW	MVW_PP	D5	RW
PRT5GS	16	RW	EP0_CR	56	#	ASC21CR2	96	RW	I2C_CFG	D6	RW
PRT5DM2	17	RW	EP0_CNT	57	#	ASC21CR3	97	RW	I2C_SCR	D7	#
	18		EP0_DR0	58	RW		98		I2C_DR	D8	RW
	19		EP0_DR1	59	RW		99		I2C_MSCR	D9	#
	1A		EP0_DR2	5A	RW		9A		INT_CLR0	DA	RW
	1B		EP0_DR3	5B	RW		9B		INT_CLR1	DB	RW
PRT7DR	1C	RW	EP0_DR4	5C	RW		9C		INT_CLR2	DC	RW
PRT7IE	1D	RW	EP0_DR5	5D	RW		9D		INT_CLR3	DD	RW
PRT7GS	1E	RW	EP0_DR6	5E	RW		9E		INT_MSK3	DE	RW
PRT7DM2	1F	RW	EP0_DR7	5F	RW		9F		INT_MSK2	DF	RW
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W	AMUXCFG	61	RW		A1		INT_MSK1	E1	RW
DBB00DR2	22	RW		62			A2		INT_VC	E2	RC
DBB00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4		DEC_DH	E4	RC
DBB01DR1	25	W	ASY_CR	65	#		A5		DEC_DL	E5	RC
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCB02DR0	28	#		68		MUL1_X	A8	W	MUL0_X	E8	W
DCB02DR1	29	W		69		MUL1_Y	A9	W	MUL0_Y	E9	W
DCB02DR2	2A	RW		6A		MUL1_DH	AA	R	MUL0_DH	EA	R
DCB02CR0	2B	#		6B		MUL1_DL	AB	R	MUL0_DL	EB	R
DCB03DR0	2C	#	TMP_DR0	6C	RW	ACC1_DR1	AC	RW	ACC0_DR1	EC	RW
DCB03DR1	2D	W	TMP_DR1	6D	RW	ACC1_DR0	AD	RW	ACC0_DR0	ED	RW
DCB03DR2	2E	RW	TMP_DR2	6E	RW	ACC1_DR3	AE	RW	ACC0_DR3	EE	RW
DCB03CR0	2F	#	TMP_DR3	6F	RW	ACC1_DR2	AF	RW	ACC0_DR2	EF	RW
	30		ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
	31		ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
	32		ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34		ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
	35		ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
	36		ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD		DAC_D	FD	RW
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.

Access is bit specific.

Absolute Maximum Ratings

Table 5. Absolute Maximum Ratings

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{STG}	Storage temperature	–55	–	+100	°C	Higher storage temperatures reduces data retention time.
$T_{BAKETEMP}$	Bake temperature	–	125	See package label	°C	–
$T_{BAKETIME}$	Bake time	See package label	–	72	Hours	–
T_A	Ambient temperature with power applied	0	–	+70	°C	–
V_{DD}	Supply voltage on V_{DD} relative to V_{SS}	–0.5	–	+6.0	V	–
V_{IO}	DC input voltage	V_{SS} – 0.5	–	V_{DD} + 0.5	V	–
V_{IO2}	DC voltage applied to tristate	V_{SS} – 0.5	–	V_{DD} + 0.5	V	–
I_{MIO}	Maximum current into any port pin	–25	–	+50	mA	–
I_{MAIO}	Maximum current into any port pin configured as an analog driver	–50	–	+50	mA	–
ESD	Electrostatic discharge voltage	2000	–	–	V	Human body model ESD.
LU	Latch up current	–	–	200	mA	–

Operating Temperature

Table 6. Operating Temperature

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{AC}	Commercial ambient temperature	0	–	+70	°C	–
T_{AI}	Industrial ambient temperature	–40	–	+85	°C	USB operation requires the use of an external clock oscillator and the 56-pin QFN package.
T_J	Junction temperature	–40	–	+100	°C	The temperature rise from ambient to junction is package specific. See “Thermal Impedance” on page 32. The user must limit the power consumption to comply with this requirement.

DC Electrical Characteristics

DC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.15 V to 3.5 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 7. DC Chip-Level Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{DD}	Supply voltage	3.0	–	5.25	V	See DC POR and LVD specifications, Table 15 on page 22. USB hardware is not functional when V_{DD} is between 3.5 V to 4.35 V.
I_{DD5}	Supply current, IMO = 24 MHz (5 V)	–	14	27	mA	Conditions are V_{DD} = 5.0 V, T_A = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz, analog power = off.
I_{DD3}	Supply current, IMO = 24 MHz (3.3 V)	–	8	14	mA	Conditions are V_{DD} = 3.3 V, T_A = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 0.367 kHz, analog power = off.
I_{SB}	Sleep [3] (mode) current with POR, LVD, sleep timer, and WDT [4].	–	3	6.5	µA	Conditions are with internal slow speed oscillator, V_{DD} = 3.3 V, 0 °C ≤ T_A ≤ 55 °C, analog power = off.
I_{SBH}	Sleep (mode) current with POR, LVD, sleep timer, and WDT at high temperature [4] .	–	4	25	µA	Conditions are with internal slow speed oscillator, V_{DD} = 3.3 V, 55 °C < T_A ≤ 70 °C, analog power = off.

Notes

3. Errata: When the device operates at4.75 V to 5.25 V and the 3.3-V regulator is enabled, a short low pulse may be created on the DP signal line during device wakeup. The 15- to 20-µs low pulse of the DP line may be interpreted by the host computer as a deattach or the beginning of a wakeup. For more details refer to Errata on page 40.
4. Standby current includes all functions (POR, LVD, WDT, sleep time) needed for reliable system operation. This should be compared with devices that have similar functions enabled.

DC GPIO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.15 V to 3.5 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 8. DC GPIO Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	–
R_{PD}	Pull-down resistor	4	5.6	8	kΩ	–
V_{OH}	High output level	V_{DD} – 1.0	–	–	V	I_{OH} = 10 mA, V_{DD} = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 80 mA maximum combined I_{OH} budget.
V_{OL}	Low output level	–	–	0.75	V	I_{OL} = 25 mA, V_{DD} = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 150 mA maximum combined I_{OL} budget.
I_{OH}	High-level source current	10	–	–	mA	–
I_{OL}	Low-level sink current	25	–	–	mA	–
V_{IL}	Input low level	–	–	0.8	V	V_{DD} = 3.15 to 5.25.
V_{IH}	Input high level	2.1	–		V	V_{DD} = 3.15 to 5.25.
V_H	Input hysteresis	–	60	–	mV	–
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 µA.
C_{IN}	Capacitive load on pins as input	–	3.5	10	pF	Package and pin dependent. Temp = 25 °C.
C_{OUT}	Capacitive load on pins as output	–	3.5	10	pF	Package and pin dependent. Temp = 25 °C.

DC Full-Speed USB Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges when the IMO is selected as system clock: 4.75 V to 5.25 V and 0 °C ≤ T_A ≤ 70 °C, or 3.15 V to 3.5 V and 0 °C ≤ T_A ≤ 70 °C, respectively.

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges when an external clock is selected as the system clock: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.15 V to 3.5 V and –40 °C ≤ T_A ≤ 85 °C.

Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 9. DC Full Speed (12 Mbps) USB Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
USB Interface						
V_{DI}	Differential input sensitivity	0.2	–	–	V	| (D+) – (D–) |
V_{CM}	Differential input common mode range	0.8	–	2.5	V	–
V_{SE}	Single-ended receiver threshold	0.8	–	2.0	V	–
C_{IN}	Transceiver capacitance	–	–	20	pF	–
I_{IO}	High Z state data line leakage	–10	–	10	µA	0 V < V_{IN} < 3.3 V.
R_{EXT}	External USB series resistor	23	–	25	Ω	In series with each USB pin.
V_{UOH}	Static output high, driven	2.8	–	3.6	V	15 kΩ ± 5% to ground. Internal pull-up enabled.
V_{UOHI}	Static output high, idle	2.7	–	3.6	V	15 kΩ ± 5% to ground. Internal pull-up enabled.
V_{UOL}	Static output low	–	–	0.3	V	15 kΩ ± 5% to ground. Internal pull-up enabled.
Z_O	USB driver output impedance	28	–	44	Ω	Including R_{EXT} resistor.
V_{CRS}	D+/D– crossover voltage	1.3	–	2.0	V	–

Table 13. 3.3-V DC Analog Reference Specifications (continued)

Reference ARF_CR [5:3]	Reference Power Settings	Symbol	Reference	Description	Min	Typ	Max	Units
0b100	All power settings. Not allowed for 3.3 V.	–	–	–	–	–	–	–
0b101	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.214	P2[4] + 1.291	P2[4] + 1.359	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.335	P2[4] – 1.292	P2[4] – 1.200	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.219	P2[4] + 1.293	P2[4] + 1.357	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.335	P2[4] – 1.295	P2[4] – 1.243	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.222	P2[4] + 1.294	P2[4] + 1.356	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.337	P2[4] – 1.296	P2[4] – 1.244	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	P2[4] + Bandgap ($P2[4] = V_{DD}/2$)	P2[4] + 1.224	P2[4] + 1.295	P2[4] + 1.355	V
		V_{AGND}	AGND	P2[4]	P2[4]	P2[4]	P2[4]	–
		V_{REFLO}	Ref Low	P2[4] – Bandgap ($P2[4] = V_{DD}/2$)	P2[4] – 1.339	P2[4] – 1.297	P2[4] – 1.244	V
0b110	RefPower = high Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap	2.510	2.595	2.655	V
		V_{AGND}	AGND	Bandgap	1.276	1.301	1.332	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.006	V_{SS} + 0.031	V
	RefPower = high Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap	2.513	2.594	2.656	V
		V_{AGND}	AGND	Bandgap	1.275	1.301	1.331	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.004	V_{SS} + 0.021	V
	RefPower = medium Opamp bias = high	V_{REFHI}	Ref High	2 × Bandgap	2.516	2.595	2.657	V
		V_{AGND}	AGND	Bandgap	1.275	1.301	1.331	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.017	V
	RefPower = medium Opamp bias = low	V_{REFHI}	Ref High	2 × Bandgap	2.520	2.595	2.658	V
		V_{AGND}	AGND	Bandgap	1.275	1.300	1.331	V
		V_{REFLO}	Ref Low	V_{SS}	V_{SS}	V_{SS} + 0.002	V_{SS} + 0.015	V
0b111	All power settings. Not allowed for 3.3 V.	–	–	–	–	–	–	–

DC Analog enCoRe III Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.15 V to 3.5 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 14. DC Analog enCoRe III Block Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
R_{CT}	Resistor unit value (CT)	–	12.2	–	kΩ	–
C_{SC}	Capacitor unit value (SC)	–	80	–	fF	–

DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.15 V to 3.5 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Note The bits PORLEV and VM in the following table refer to bits in the VLT_CR register. See the *PSoC® Technical Reference Manual* for more information on the VLT_CR register.

Table 15. DC POR and LVD Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{PPOR0R} [5] V_{PPOR1R} [5] V_{PPOR2R} [5]	V_{DD} value for PPOR trip (positive ramp) PORLEV[1:0] = 00b PORLEV[1:0] = 01b PORLEV[1:0] = 10b	 – –	 2.91 4.39 4.55	 – –	 V V V	–
V_{PPOR0} V_{PPOR1} V_{PPOR2}	V_{DD} value for PPOR trip (negative ramp) PORLEV[1:0] = 00b PORLEV[1:0] = 01b PORLEV[1:0] = 10b	 – –	 2.82 4.39 4.55	 – –	 V V V	–
V_{PH0} V_{PH1} V_{PH2}	PPOR hysteresis PORLEV[1:0] = 00b PORLEV[1:0] = 01b PORLEV[1:0] = 10b	 – – –	 92 0 0	 – – –	 mV mV mV	–
V_{LVD0} V_{LVD1} V_{LVD2} V_{LVD3} V_{LVD4} V_{LVD5} V_{LVD6} V_{LVD7}	V_{DD} value for LVD trip VM[2:0] = 000b VM[2:0] = 001b VM[2:0] = 010b VM[2:0] = 011b VM[2:0] = 100b VM[2:0] = 101b VM[2:0] = 110b VM[2:0] = 111b	 2.86 2.96 3.07 3.92 4.39 4.55 4.63 4.72	 2.92 3.02 3.13 4.00 4.48 4.64 4.73 4.81	 2.98[6] 3.08 3.20 4.08 4.57 4.74[7] 4.82 4.91	 V V V V V V V V	–

Notes
5. Errata: When VDD of the device is pulled below ground just before power on, the first read from each 8K Flash page may be corrupted. This issue does not affect Flash page 0 because it is the selected page upon reset. For more details in Errata on page 40.
6. Always greater than 50 mV above PPOR (PORLEV = 00) for falling supply.
7. Always greater than 50 mV above PPOR (PORLEV = 10) for falling supply.

AC Electrical Characteristics

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.15 V to 3.5 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 18. AC Chip-Level Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
$F_{IMO245V}$	IMO frequency for 24 MHz (5 V)	23.04	24	24.96[11, 12]	MHz	Trimmed for 5 V operation using factory trim values.
$F_{IMO243V}$	IMO frequency for 24 MHz (3.3 V)	22.08	24	25.92[11,13]	MHz	Trimmed for 3.3 V operation using factory trim values.
F_{IMOUSB}	IMO frequency with USB frequency locking enabled and USB traffic present	23.94	24	24.06[12]	MHz	USB operation for system clock source from the IMO is limited to 0°C ≤ T_A ≤ 70°C.
F_{CPU1}	CPU frequency (5 V nominal)	0.090	24	24.96[11,12]	MHz	SLIMO mode = 0.
F_{CPU2}	CPU frequency (3.3 V nominal)	0.086	12	12.96[12,13]	MHz	SLIMO mode = 0.
F_{BLK5}	Digital PSoC block frequency (5 V nominal)	0	48	49.92[11,12,14]	MHz	Refer to the AC Digital Block Specifications on page 26.
F_{BLK3}	Digital PSoC block frequency (3.3 V nominal)	0	24	25.92[12,14]	MHz	–
F_{32K1}	ILO frequency	15	32	64	kHz	–
F_{32K_U}	ILO untrimmed frequency	5	–	100	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference Manual for details on this timing.
DC_{ILO}	ILO duty cycle	20	50	80	%	–
DC_{24M}	24-MHz duty cycle	40	50	60	%	–
Step24M	24-MH trim step size	–	50	–	kHz	–
Fout48M	48-MHz output frequency	46.08	48.0	49.92[11,13]	MHz	Trimmed. Utilizing factory trim values.
F_{MAX}	Maximum frequency of signal on row input or row output	–	–	12.96	MHz	–
SR_{POWER_UP}	Power supply slew rate	–	–	250	V/ms	–
$T_{POWERUP}$	Time from end of POR to CPU executing code	–	16	100	ms	–
T_{jit_IMO}[15]	24 MHz IMO cycle-to-cycle jitter (RMS)	–	200	1200	ps	
	24 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	900	6000	ps	N = 32.
	24 MHz IMO period jitter (RMS)	–	200	900	ps	

Notes

11. 4.75 V < V_{DD} < 5.25 V.
12. Accuracy derived from Internal Main Oscillator with appropriate trim for V_{DD} range.
13. 3.0 V < V_{DD} < 3.6 V. See application note AN2012 “Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation” for information on trimming for operation at 3.3 V.
14. See the individual user module data sheets for information on maximum frequencies for user modules.
15. Refer to Cypress Jitter Specifications application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 for more information.

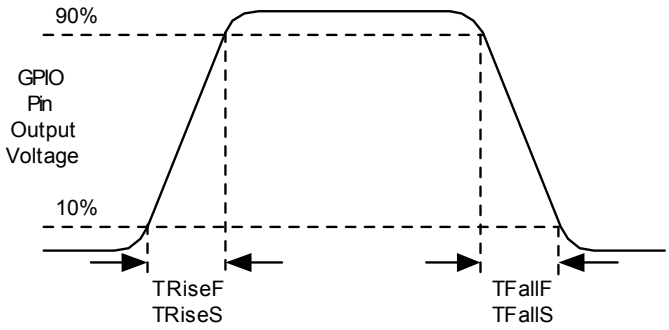
AC GPIO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.15 V to 3.5 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 19. AC GPIO Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
F_{GPIO}	GPIO operating frequency	0	–	12	MHz	Normal Strong Mode
TRiseF	Rise time, normal strong mode, Cload = 50 pF	3	–	18	ns	V_{DD} = 4.5 to 5.25 V, 10%–90%
TFallF	Fall time, normal strong mode, Cload = 50 pF	2	–	18	ns	V_{DD} = 4.5 to 5.25 V, 10%–90%
TRiseS	Rise time, slow strong mode, Cload = 50 pF	10	27	–	ns	V_{DD} = 3 to 5.25 V, 10%–90%
TFallS	Fall time, slow strong mode, Cload = 50 pF	10	22	–	ns	V_{DD} = 3 to 5.25 V, 10%–90%

Figure 6. GPIO Timing Diagram



AC Full Speed USB Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.15 V to 3.5 V and –40 °C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 20. AC Full-Speed (12 Mbps) USB Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{RFS}	Transition rise time	4	–	20	ns	For 50-pF load.
T_{FSS}	Transition fall time	4	–	20	ns	For 50-pF load.
T_{RFMFS}	Rise/fall time matching: (T_R/T_F)	90	–	111	%	For 50-pF load.
$T_{DRATEFS}$	Full-speed data rate	12 – 0.25%	12	12 + 0.25%	Mbps	–

AC Digital Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85°C, or 3.15 V to 3.5 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 21. AC Digital Block Specifications

Function	Description	Min	Typ	Max	Unit	Notes
All functions	Block input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	49.92	MHz	
	V_{DD} < 4.75 V	–	–	25.92	MHz	
Timer	Input clock frequency					
	No capture, V_{DD} ≥ 4.75 V	–	–	49.92	MHz	
	No capture, V_{DD} < 4.75 V	–	–	25.92	MHz	
	With capture	–	–	25.92	MHz	
	Capture pulse width	50[16]	–	–	ns	
Counter	Input clock frequency					
	No enable input, V_{DD} ≥ 4.75 V	–	–	49.92	MHz	
	No enable input, V_{DD} < 4.75 V	–	–	25.92	MHz	
	With enable input	–	–	25.92	MHz	
	Enable input pulse width	50[16]	–	–	ns	
	Kill pulse width					
	Asynchronous restart mode	20	–	–	ns	
	Synchronous restart mode	50[16]	–	–	ns	
	Disable mode	50[16]	–	–	ns	
	Input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	49.92	MHz	
	V_{DD} < 4.75 V	–	–	25.92	MHz	
CRCPRS (PRS Mode)	Input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	49.92	MHz	
	V_{DD} < 4.75 V	–	–	25.92	MHz	
CRCPRS (CRC Mode)	Input clock frequency	–	–	24.6	MHz	
SPIM	Input clock frequency	–	–	8.2	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2.
SPIS	Input clock (SCLK) frequency	–	–	4.1	MHz	The input clock is the SPI SCLK in SPIS mode.
	Width of SS_negated between transmissions	50[16]	–	–	ns	
Transmitter	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8.
	V_{DD} ≥ 4.75 V, 2 stop bits	–	–	49.92	MHz	
	V_{DD} ≥ 4.75 V, 1 stop bit	–	–	24.6	MHz	
	V_{DD} < 4.75 V	–	–	24.6	MHz	
Receiver	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8.
	V_{DD} ≥ 4.75 V, 2 stop bits	–	–	49.92	MHz	
	V_{DD} ≥ 4.75 V, 1 stop bit	–	–	24.6	MHz	
	V_{DD} < 4.75 V	–	–	24.6	MHz	

Note
16. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

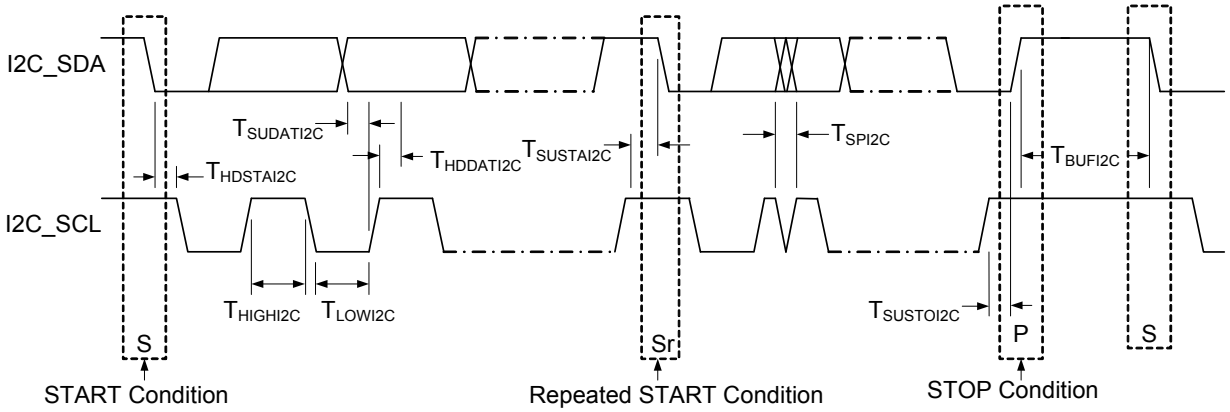
AC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.15 V to 3.5 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 26. AC Characteristics of the I²C SDA and SCL Pins for V_{DD}

Parameter	Description	Standard-Mode		Fast-Mode		Unit	Notes
		Min	Max	Min	Max		
F_{SCLI2C}	SCL clock frequency	0	100	0	400	kHz	–
$T_{HDSTAI2C}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs	–
T_{LOWI2C}	LOW period of the SCL clock	4.7	–	1.3	–	µs	–
$T_{HIGHI2C}$	HIGH period of the SCL clock	4.0	–	0.6	–	µs	–
$T_{SUSTAI2C}$	Setup time for a repeated START condition	4.7	–	0.6	–	µs	–
$T_{HDDATI2C}$	Data hold time	0	–	0	–	µs	–
$T_{SUDATI2C}$	Data setup time	250	–	100[17]	–	ns	–
$T_{SUSTOI2C}$	Setup time for STOP condition	4.0	–	0.6	–	µs	–
T_{BUFI2C}	Bus free time between a STOP and START condition	4.7	–	1.3	–	µs	–
T_{SPI2C}	Pulse width of spikes are suppressed by the input filter.	–	–	0	50	ns	–

Figure 7. Definition for Timing for Fast-/Standard-Mode on the I²C Bus



Note

17. A Fast-Mode I²C-bus device can be used in a Standard-Mode I²C-bus system, but the requirement $T_{SUDATI2C} \geq 250$ ns must then be met. This automatically is the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + T_{SUDATI2C} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I²C-bus specification) before the SCL line is released.

Figure 9. 56-pin QFN (8 × 8 × 1.0 mm) 4.5 × 5.2 E-Pad (Sawn) Package Outline, 001-53450

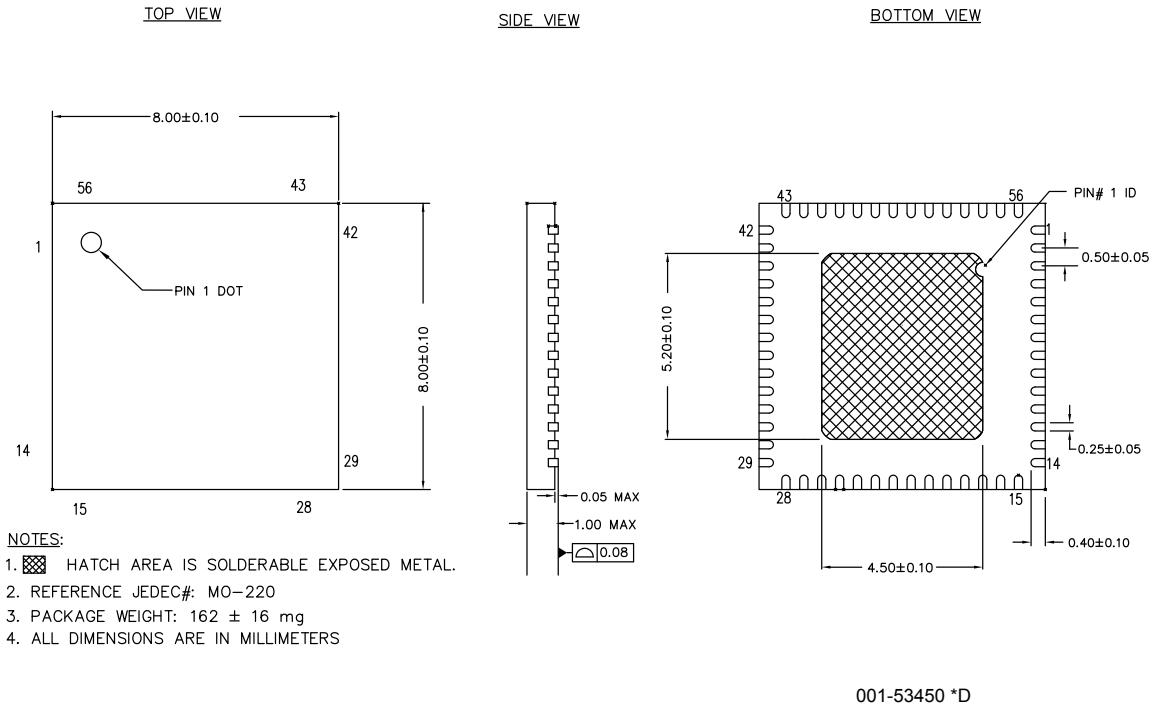
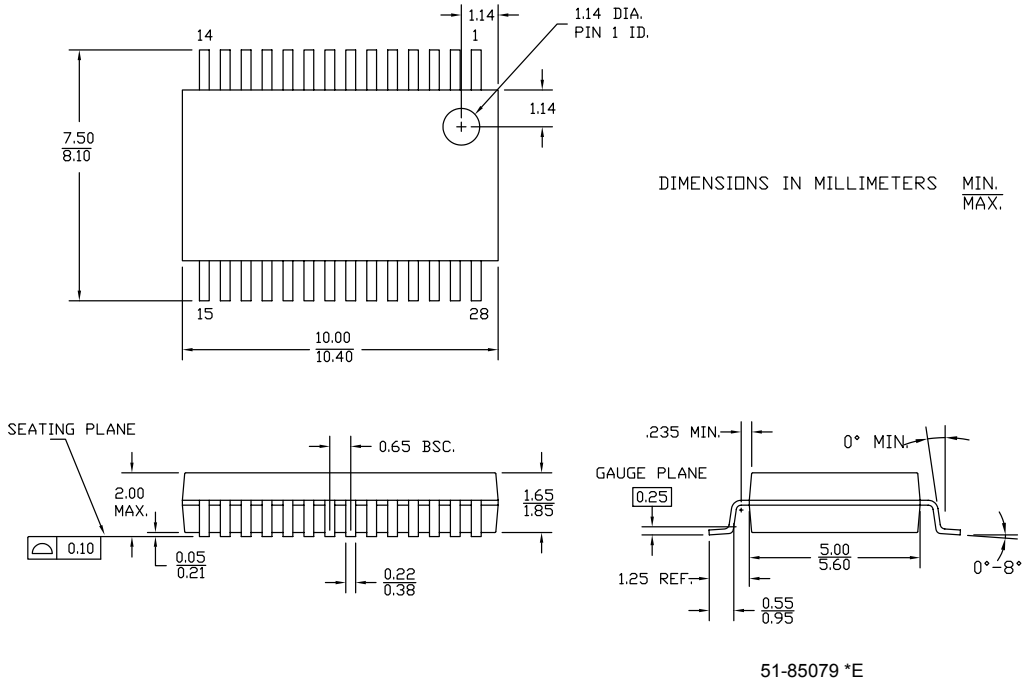


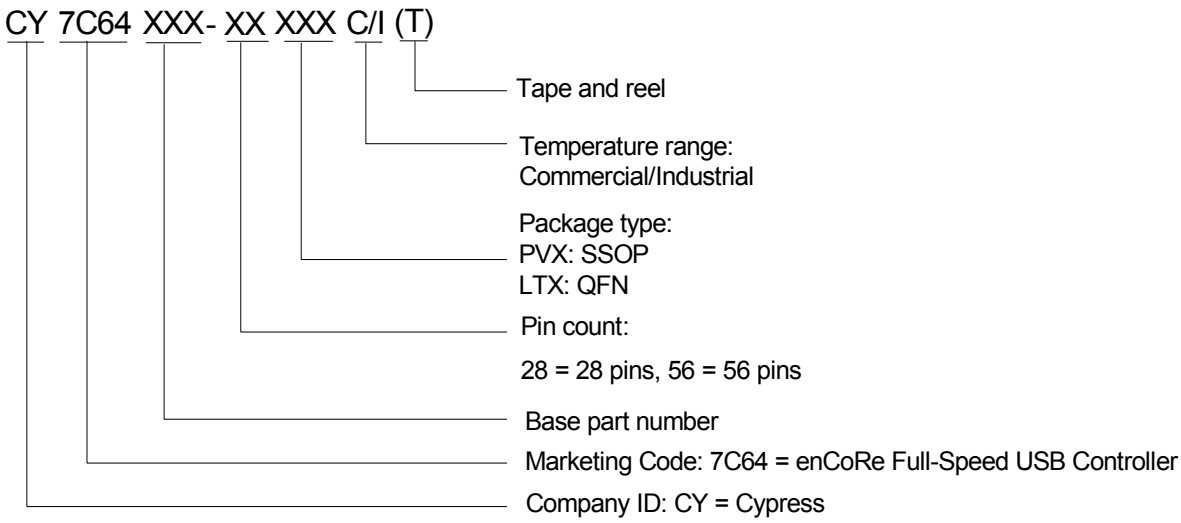
Figure 10. 28-pin SSOP (210 Mils) Package Outline, 51-85079



Ordering Information

Package	Ordering Code	Flash Size	SRAM (Bytes)	Temperature Range
28-pin SSOP	CY7C64215-28PVXC	16K	1K	Commercial, 0 °C to 70 °C
28-pin SSOP (Tape and Reel)	CY7C64215-28PVXCT	16K	1K	Commercial, 0 °C to 70 °C
28-pin SSOP	CY7C64215-28PVXI	16 K	1K	Industrial, –40 °C to 85 °C
28-pin SSOP (Tape and Reel)	CY7C64215-28PVXIT	16 K	1K	Industrial, –40 °C to 85 °C
56-pin QFN (Sawn)	CY7C64215-56LTXC	16K	1K	Commercial, 0 °C to 70 °C
56-pin QFN (Sawn) (Tape and Reel)	CY7C64215-56LTXCT	16K	1K	Commercial, 0 °C to 70 °C
56-pin QFN (Sawn)	CY7C64215-56LTXI	16K	1K	Industrial, –40 °C to 85 °C
56-pin QFN (Sawn) (Tape and Reel)	CY7C64215-56LTXIT	16K	1K	Industrial, –40 °C to 85 °C

Ordering Code Definitions



Document Conventions

Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	ms	milli-second
dB	decibels	mV	milli-volts
fF	femto farad	nA	nanoampere
kHz	kilohertz	ns	nanosecond
kΩ	kilohm	Ω	ohm
MHz	megahertz	pF	picofarad
µA	microampere	ps	picosecond
µs	microsecond	%	percent
µV	microvolts	V	volts
mA	milli-ampere	W	watts
mm	milli-meter		

Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, ‘01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’ or ‘b’ are decimal.

active high	5. A logic signal having its asserted state as the logic 1 state. 6. A logic signal having the logic 1 state as the higher voltage of the two states.
analog blocks	The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.
analog-to-digital (ADC)	A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation.
API (Application Programming Interface)	A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.
asynchronous	A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.
Bandgap reference	A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference.
bandwidth	1. The frequency range of a message or information processing system measured in hertz. 2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.
bias	1. A systematic deviation of a value from a reference value. 2. The amount by which the average of a set of values departs from a reference value. 3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device.
block	1. A functional unit that performs a single function, such as an oscillator. 2. A functional unit that may be configured to perform one of several functions, such as a digital PSoC block or an analog PSoC block.

flash	An electrically programmable and erasable, non-volatile technology that provides users with the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is off.
Flash block	The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes.
frequency	The number of cycles or events per unit of time, for a periodic function.
gain	The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB.
I^2C	A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I2C uses only two bi-directional pins, clock and data, both running at +5V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode.
ICE	The in-circuit emulator that allows users to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer).
input/output (I/O)	A device that introduces data into or extracts data from a system.
interrupt	A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed.
interrupt service routine (ISR)	A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution.
jitter	1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams. 2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles.
low-voltage detect (LVD)	A circuit that senses V_{DD} and provides an interrupt to the system when V_{DD} falls lower than a selected threshold.
M8C	An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space.
master device	A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the ***slave device.***
microcontroller	An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and IO circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor.
mixed-signal	The reference to a circuit containing both analog and digital techniques and components.
modulator	A device that imposes a signal on a carrier.

noise	1. A disturbance that affects a signal and that may distort the information carried by the signal. 2. The random variations of one or more characteristics of any entity such as voltage, current, or data.
oscillator	A circuit that may be crystal controlled and is used to generate a clock frequency.
parity	A technique for testing transmitting data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity).
phase-locked loop (PLL)	An electronic circuit that controls an ***oscillator*** so that it maintains a constant phase angle relative to a reference signal.
pinouts	The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names.
port	A group of pins, usually eight.
power on reset (POR)	A circuit that forces the PSoC device to reset when the voltage is lower than a pre-set level. This is one type of hardware reset.
PSoC®	Cypress Semiconductor's PSoC® is a registered trademark and Programmable System-on-Chip™ is a trademark of Cypress.
PSoC Designer™	The software for Cypress' Programmable System-on-Chip technology.
pulse width modulator (PWM)	An output in the form of duty cycle which varies as a function of the applied measurand
RAM	An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in.
register	A storage device with a specific capacity, such as a bit or byte.
reset	A means of bringing a system back to a know state. See hardware reset and software reset.
ROM	An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in.
serial	1. Pertaining to a process in which all events occur one after the other. 2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel.
settling time	The time it takes for an output signal or value to stabilize after the input has changed from one value to another.
shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.
SRAM	An acronym for static random access memory. A memory device allowing users to store and retrieve data at a high rate of speed. The term static is used because, after a value has been loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.

Document History Page

Description Title: CY7C64215, enCoRe™ III Full-Speed USB Controller Document Number: 38-08036				
Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	131325	See ECN	XGR	New data sheet.
*A	385256	See ECN	BHA	Changed status from Advance Information to Preliminary. Added standard data sheet items. Changed Part number from CY7C642xx to CY7C64215.
*B	2547630	08/04/08	AZIEL / PYRS	Operational voltage range for USB specified under “Full Speed USB (12Mbps)”. CMP_GO_EN1 register removed as it has no functionality on Radon. Figure “CPU Frequency” adjusted to show invalid operating region for USB with footnote describing reason. DC electrical characteristic, V_{DD}. Note added describing where USB hardware is non-functional.
*C	2620679	12/12/08	CMCC / PYRS	Added Package Handling information. Deleted note regarding link to amkor.com for MLF package dimensions.
*D	2717887	06/11/2009	DPT	Added 56 -Pin Sawn QFN (8 X 8 mm) package diagram and added CY7C64215-56LTXC part information in the Ordering Information table.
*E	2852393	01/15/2010	BHA / XUT	■ Added Table of Contents. ■ Added external clock oscillator option and Industrial Temperature information to the Features, Pin Information, Electrical Specifications, Operating Temperature, DC Electrical Characteristics, AC Electrical Characteristics, and Ordering Information sections. ■ Updated DC GPIO, AC Chip, and AC Programming Specifications follows: ❒ Replaced TRAMP (time) with SRPOWER_UP (slew rate) specification. ❒ Added I_{OH}, I_{OL}, DCILO, F32K_U, TPOWERUP, TERASEALL, TPROGRAM_HOT, and TPROGRAM_COLD specifications. ❒ Updated V_{DD} ranges on Figure 5 and Table 8. ❒ Added notes for VM and VDI on Table 10. ❒ Removed TR/TF from Table 20. ■ Update Ordering Information for: CY7C64215-56LFXCT, CY7C64215-28PVXCT, CY7C64215-56LTXIT Tape and Reel. ■ Updated 28-Pin SSOP and 56-Pin QFN PUNCH and SAWN package diagrams. ■ Updated copyright and Sales, Solutions, and Legal Information URLs.
*F	2892683	03/15/2010	NJF	Updated Cypress website links. Added $T_{BAKETEMP}$ and $T_{BAKETIME}$ parameters in Absolute Maximum Ratings. Updated AC Chip-Level Specifications Removed inactive parts from Ordering Information Updated note in Packaging Information.
*G	3070717	10/25/2010	XUT	Removed reference to CYFISPI in Features. Updated datasheet as per Cypress style guide and new datasheet template.
*H	3090908	11/19/10	CSAI	Updated AC Chip-Level Specifications table. Added DC I^2C Specification.
*I	3143408	01/17/11	NJF	Added DC I^2C Specifications table. Added Tjit_IMO specification, removed existing jitter specifications. Updated Analog reference tables. Updated Units of Measure, Acronyms, Glossary, and References sections. Updated solder reflow specifications. No specific changes were made to AC Digital Block Specifications table and I^2C Timing Diagram. They were updated for clearer understanding.

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