



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f2401vn020ec



Timer Operating Modes	58
Reading the Timer Count Values	66
Timer Output Signal Operation	66
Timer Control Register Definitions	66
Timer 0-3 High and Low Byte Registers	66
Timer Reload High and Low Byte Registers	67
Timer 0-3 PWM High and Low Byte Registers	69
Timer 0-3 Control Registers	70
Watch-Dog Timer	72
Overview	72
Operation	72
Watch-Dog Timer Refresh	73
Watch-Dog Timer Time-Out Response	73
Watch-Dog Timer Reload Unlock Sequence	74
Watch-Dog Timer Control Register Definitions	75
Watch-Dog Timer Control Register	75
Watch-Dog Timer Reload Upper, High and Low Byte Registers ..	76
UART	78
Overview	78
Architecture	78
Operation	79
Data Format	79
Transmitting Data using the Polled Method	80
Transmitting Data using the Interrupt-Driven Method	81
Receiving Data using the Polled Method	82
Receiving Data using the Interrupt-Driven Method	82
Receiving Data using the Direct Memory Access Controller (DMA)	83
Multiprocessor (9-bit) Mode	84
UART Interrupts	85
UART Baud Rate Generator	85
UART Control Register Definitions	86
UARTx Transmit Data Register	86
UARTx Receive Data Register	87
UARTx Status 0 and Status 1 Registers	87
UARTx Control 0 and Control 1 Registers	89
UARTx Baud Rate High and Low Byte Registers	91
Infrared Encoder/Decoder	95
Overview	95
Architecture	95
Operation	96



Figure 31.	Flash Controller Operation Flow Chart	140
Figure 32.	On-Chip Debugger Block Diagram	151
Figure 33.	Interfacing the On-Chip Debugger's DBG Pin with an RS-232 Interface (1)	152
Figure 34.	Interfacing the On-Chip Debugger's DBG Pin with an RS-232 Interface (2)	153
Figure 35.	OCD Data Format	154
Figure 36.	Recommended Crystal Oscillator Configuration (20MHz operation)	166
Figure 37.	Nominal ICC Versus System Clock Frequency	170
Figure 38.	Nominal Halt Mode ICC Versus System Clock Frequency	171
Figure 39.	Port Input Sample Timing	176
Figure 40.	GPIO Port Output Timing	177
Figure 41.	On-Chip Debugger Timing	178
Figure 42.	SPI Master Mode Timing	179
Figure 43.	SPI Slave Mode Timing	180
Figure 44.	I ² C Timing	181
Figure 45.	Flags Register	201
Figure 46.	Opcode Map Cell Description	202
Figure 47.	First Opcode Map	204
Figure 48.	Second Opcode Map after 1FH	205
Figure 49.	40-Lead Plastic Dual-Inline Package (PDIP)	206
Figure 50.	44-Lead Low-Profile Quad Flat Package (LQFP)	207
Figure 51.	44-Lead Plastic Lead Chip Carrier Package (PLCC)	207
Figure 52.	64-Lead Low-Profile Quad Flat Package (LQFP)	208
Figure 53.	68-Lead Plastic Lead Chip Carrier Package (PLCC)	209
Figure 54.	80-Lead Quad-Flat Package (QFP)	210



List of Tables

Table 1.	Z8F640x Family Part Selection Guide	2
Table 2.	Z8F640x Family Package Options	6
Table 3.	Signal Descriptions	13
Table 4.	Pin Characteristics of the Z8F640x family	15
Table 5.	Z8F640x Family Program Memory Maps	18
Table 6.	Z8F640x Family Data Memory Maps	19
Table 7.	Register File Address Map	20
Table 8.	Reset and STOP Mode Recovery Characteristics and Latency	25
Table 9.	Reset Sources and Resulting Reset Type	26
Table 10.	STOP Mode Recovery Sources and Resulting Action	29
Table 11.	Port Availability by Device and Package Type	33
Table 12.	Port Alternate Function Mapping	35
Table 13.	Port A-H GPIO Address Registers (PxADDR)	37
Table 14.	GPIO Port Registers and Sub-Registers	37
Table 15.	Port A-H Control Registers (PxCTL)	38
Table 16.	Port A-H Data Direction Sub-Registers	39
Table 17.	Port A-H Alternate Function Sub-Registers	39
Table 18.	Port A-H Output Control Sub-Registers	40
Table 19.	Port A-H High Drive Enable Sub-Registers	41
Table 20.	Port A-H Input Data Registers (PxIN)	42
Table 21.	Port A-H STOP Mode Recovery Source Enable Sub-Registers	42
Table 22.	Port A-H Output Data Register (PxOUT)	43
Table 23.	Interrupt Vectors in Order of Priority	45
Table 24.	Interrupt Request 0 Register (IRQ0)	48
Table 25.	Interrupt Request 1 Register (IRQ1)	49
Table 26.	Interrupt Request 2 Register (IRQ2)	50
Table 27.	IRQ0 Enable and Priority Encoding	51
Table 28.	IRQ0 Enable High Bit Register (IRQ0ENH)	51
Table 29.	IRQ0 Enable Low Bit Register (IRQ0ENL)	52
Table 30.	IRQ1 Enable and Priority Encoding	52
Table 31.	IRQ1 Enable Low Bit Register (IRQ1ENL)	53



Table 101. Absolute Maximum Ratings	167
Table 102. DC Characteristics	169
Table 103. AC Characteristics	172
Table 104. Power-On Reset and Voltage Brown-Out Electrical Characteristics and Timing	173
Table 105. Flash Memory Electrical Characteristics and Timing . . .	173
Table 106. Watch-Dog Timer Electrical Characteristics and Timing	174
Table 107. Analog-to-Digital Converter Electrical Characteristics and Timing	174
Table 108. GPIO Port Input Timing	176
Table 109. GPIO Port Output Timing	177
Table 110. On-Chip Debugger Timing	178
Table 111. SPI Master Mode Timing	179
Table 112. SPI Slave Mode Timing	180
Table 113. I2C Timing	181
Table 114. Assembly Language Syntax Example 1	183
Table 115. Assembly Language Syntax Example 2	183
Table 116. Notational Shorthand	184
Table 117. Additional Symbols	185
Table 118. Condition Codes	186
Table 119. Arithmetic Instructions	187
Table 120. Bit Manipulation Instructions	188
Table 121. Block Transfer Instructions	188
Table 122. CPU Control Instructions	189
Table 123. Load Instructions	189
Table 124. Logical Instructions	190
Table 125. Program Control Instructions	190
Table 126. Rotate and Shift Instructions	191
Table 127. eZ8 CPU Instruction Summary	191
Table 128. Opcode Map Abbreviations	203
Table 129. Ordering Information	211



Use of All Uppercase Letters

The use of all uppercase letters designates the names of states and commands.

- Example 1: The bus is considered BUSY after the Start condition.
- Example 2: A START command triggers the processing of the initialization sequence.

Bit Numbering

Bits are numbered from 0 to $n-1$ where n indicates the total number of bits. For example, the 8 bits of a register are numbered from 0 to 7.

Safeguards

It is important that all users understand the following safety terms, which are defined here.



Caution: Indicates a procedure or file may become corrupted if the user does not follow directions.

Trademarks

ZiLOG, eZ8, Z8 Encore!, and Z8 are trademarks of [ZiLOG, Inc.](#) in the U.S.A. and other countries. All other trademarks are the property of their respective corporations.



- Software stack allows much greater depth in subroutine calls and interrupts than hardware stacks
- Compatible with existing Z8 code
- Expanded internal Register File allows access of up to 4KB
- New instructions improve execution efficiency for code developed using higher-level programming languages, including C
- Pipelined instruction fetch and execution
- New instructions for improved performance including BIT, BSWAP, BTJ, CPC, LDC, LDCI, LEA, MULT, and SRL
- New instructions support 12-bit linear addressing of the Register File
- Up to 10 MIPS operation
- C-Compiler friendly
- 2-9 clock cycles per instruction

For more information regarding the eZ8 CPU, refer to the *eZ8 CPU User Manual* available for download at www.zilog.com.

General Purpose I/O

The Z8 Encore!® features seven 8-bit ports (Ports A-G) and one 4-bit port (Port H) for general purpose I/O (GPIO). Each pin is individually programmable.

Flash Controller

The Flash Controller programs and erases the Flash memory.

10-Bit Analog-to-Digital Converter

The Analog-to-Digital Converter (ADC) converts an analog input signal to a 10-bit binary number. The ADC accepts inputs from up to 12 different analog input sources.

UARTs

Each UART is full-duplex and capable of handling asynchronous data transfers. The UARTs support 8- and 9-bit data modes and selectable parity.

I²C

The inter-integrated circuit (I²C®) controller makes the Z8 Encore!® compatible with the I²C protocol. The I²C controller consists of two bidirectional bus lines, a serial data (SDA) line and a serial clock (SCL) line.

System and Short Resets

During a System Reset, the Z8F640x family device is held in Reset for 514 cycles of the Watch-Dog Timer oscillator followed by 16 cycles of the system clock (crystal oscillator). A Short Reset differs from a System Reset only in the number of Watch-Dog Timer oscillator cycles required to exit Reset. A Short Reset requires only 66 Watch-Dog Timer oscillator cycles. Unless specifically stated otherwise, System Reset and Short Reset are referred to collectively as Reset.

During Reset, the eZ8 CPU and on-chip peripherals are idle; however, the on-chip crystal oscillator and Watch-Dog Timer oscillator continue to run. The system clock begins operating following the Watch-Dog Timer oscillator cycle count. The eZ8 CPU and on-chip peripherals remain idle through the 16 cycles of the system clock.

Upon Reset, control registers within the Register File that have a defined Reset value are loaded with their reset values. Other control registers (including the Stack Pointer, Register Pointer, and Flags) and general-purpose RAM are undefined following Reset. The eZ8 CPU fetches the Reset vector at Program Memory addresses 0002H and 0003H and loads that value into the Program Counter. Program execution begins at the Reset vector address.

Reset Sources

Table 8 lists the reset sources and type of Reset as a function of the Z8F640x family device operating mode. The text following provides more detailed information on the individual Reset sources. Please note that Power-On Reset / Voltage Brown-Out events always have priority over all other possible reset sources to insure a full system reset occurs.

Table 8. Reset Sources and Resulting Reset Type

Operating Mode	Reset Source	Reset Type
Normal or Halt modes	Power-On Reset / Voltage Brown-Out	System Reset
	Watch-Dog Timer time-out when configured for Reset	Short Reset
	$\overline{\text{RESET}}$ pin assertion	Short Reset
	On-Chip Debugger initiated Reset (OCDCTL[1] set to 1)	System Reset except the On-Chip Debugger is unaffected by the reset
Stop mode	Power-On Reset / Voltage Brown-Out	System Reset
	$\overline{\text{RESET}}$ pin assertion	System Reset
	DBG pin driven Low	System Reset

Architecture

Figure 65 illustrates a block diagram of the interrupt controller.

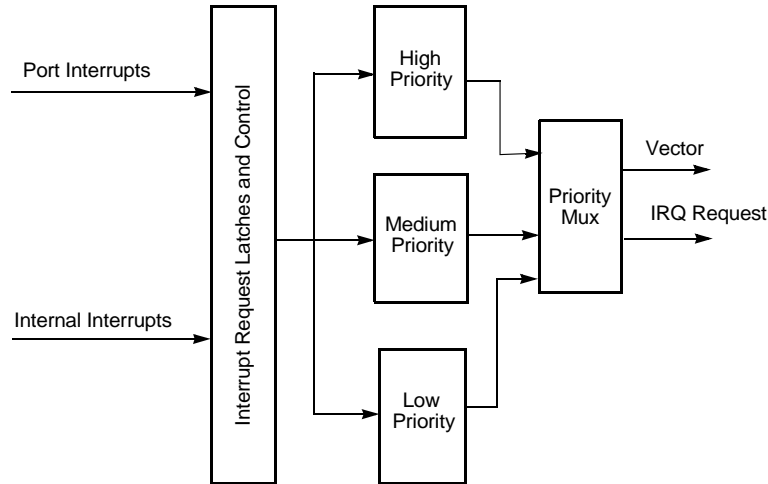


Figure 65. Interrupt Controller Block Diagram

Operation

Master Interrupt Enable

The master interrupt enable bit (IRQE) in the Interrupt Control register globally enables and disables interrupts.

Interrupts are globally enabled by any of the following actions:

- Execution of an EI (Enable Interrupt) instruction
- Execution of an IRET (Return from Interrupt) instruction
- Writing a 1 to the IRQE bit in the Interrupt Control register

Interrupts are globally disabled by any of the following actions:

- Execution of a DI (Disable Interrupt) instruction
- eZ8 CPU acknowledgement of an interrupt service request from the interrupt controller
- Writing a 0 to the IRQE bit in the Interrupt Control register
- Reset



- Disable the timer
 - Configure the timer for PWM mode.
 - Set the prescale value.
 - Set the initial logic level (High or Low) and PWM High/Low transition for the Timer Output alternate function.
2. Write to the Timer High and Low Byte registers to set the starting count value (typically 0001H). This only affects the first pass in PWM mode. After the first timer reset in PWM mode, counting always begins at the reset value of 0001H.
 3. Write to the PWM High and Low Byte registers to set the PWM value.
 4. Write to the Timer Reload High and Low Byte registers to set the Reload value (PWM period). The Reload value must be greater than the PWM value.
 5. If desired, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
 6. Configure the associated GPIO port pin for the Timer Output alternate function.
 7. Write to the Timer Control register to enable the timer and initiate counting.

The PWM period is given by the following equation:

$$\text{PWM Period (s)} = \frac{\text{Reload Value} \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

If an initial starting value other than 0001H is loaded into the Timer High and Low Byte registers, the One-Shot mode equation must be used to determine the first PWM time-out period.

If TPOL is set to 0, the ratio of the PWM output High time to the total period is given by:

$$\text{PWM Output High Time Ratio (\%)} = \frac{\text{Reload Value} - \text{PWM Value}}{\text{Reload Value}} \times 100$$

If TPOL is set to 1, the ratio of the PWM output High time to the total period is given by:

$$\text{PWM Output High Time Ratio (\%)} = \frac{\text{PWM Value}}{\text{Reload Value}} \times 100$$

Capture Mode

In Capture mode, the current timer count value is recorded when the desired external Timer Input transition occurs. The Capture count value is written to the Timer PWM High and Low Byte Registers. The timer input is the system clock. The TPOL bit in the Timer Control register determines if the Capture occurs on a rising edge or a falling edge of the



0 = Disable Multiprocessor mode.

1 = Enable Multiprocessor mode.

MPE—Multiprocessor Enable

0 = The UART processes all received data bytes.

1 = The UART processes only data bytes in which the multiprocessor data bit (9th bit) is set to 1.

MPBT—Multiprocessor Bit Transmitter

This bit is applicable only when Multiprocessor (9-bit) mode is enabled.

0 = Send a 0 in the multiprocessor bit location of the data stream (9th bit).

1 = Send a 1 in the multiprocessor bit location of the data stream (9th bit).

Reserved

These bits are reserved and must be 0.

$\overline{\text{RDAIRQ}}$ —Receive Data Interrupt $\overline{\text{Enable}}$

0 = Received data and receiver errors generates an interrupt request to the Interrupt Controller.

1 = Received data does not generate an interrupt request to the Interrupt Controller. Only receiver errors generate an interrupt request. The associated DMA will still be notified that received data is available.

IREN—Infrared Encoder/Decoder Enable

0 = Infrared Encoder/Decoder is disabled. UART operates normally operation.

1 = Infrared Encoder/Decoder is enabled. The UART transmits and receives data through the Infrared Encoder/Decoder.

UARTx Baud Rate High and Low Byte Registers

The UARTx Baud Rate High and Low Byte registers (Tables 56 and 57) combine to create a 16-bit baud rate divisor value (BRG[15:0]) that sets the data transmission rate (baud rate) of the UART.

Table 56. UARTx Baud Rate High Byte Register (UxBRH)

BITS	7	6	5	4	3	2	1	0
FIELD	BRH							
RESET	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	F46H and F4EH							

The Master and Slave are each capable of exchanging a byte of data during a sequence of eight clock cycles. In both Master and Slave SPI devices, data is shifted on one edge of the SCK and is sampled on the opposite edge where data is stable. Edge polarity is determined by the SPI phase and polarity control.

Slave Select

The active Low Slave Select (\overline{SS}) input signal is used to select a Slave SPI device. \overline{SS} must be Low prior to all data communication to and from the Slave device. \overline{SS} must stay Low for the full duration of each character transferred. The \overline{SS} signal may stay Low during the transfer of multiple characters or may deassert between each character.

When the SPI on the Z8F640x family device is configured as the only Master in an SPI system, the \overline{SS} pin can be set as either an input or an output. For communication between the Z8F640x family device SPI Master and external Slave devices, the \overline{SS} signal, as an output, can assert the \overline{SS} input pin on one of the Slave devices. Other GPIO output pins can also be employed to select external SPI Slave devices.

When the SPI on the Z8F640x family device is configured as one Master in a multi-master SPI system, the \overline{SS} pin on the should be set as an input. The \overline{SS} input signal on the Master must be High. If the \overline{SS} signal goes Low (indicating another Master is driving the SPI bus), a Mode Fault error flag is set in the SPI Status register.

SPI Clock Phase and Polarity Control

The SPI supports four combinations of serial clock phase and polarity using two bits in the SPI Control register. The clock polarity bit, CLKPOL, selects an active high or active low clock and has no effect on the transfer format. Table 59 lists the SPI Clock Phase and Polarity Operation parameters. The clock phase bit, PHASE, selects one of two fundamentally different transfer formats. For proper data transmission, the clock phase and polarity must be identical for the SPI Master and the SPI Slave. The Master always places data on the MOSI line a half-cycle before the clock edge (SCK signal), in order for the Slave to latch the data.

Table 59. SPI Clock Phase (PHASE) and Clock Polarity (CLKPOL) Operation

PHASE	CLKPOL	SCK Transmit Edge	SCK Receive Edge	SCK Idle State
0	0	Falling	Rising	Low
0	1	Rising	Falling	High
1	0	Rising	Falling	Low
1	1	Falling	Rising	High

DMA Status Register

The DMA Status register indicates the DMA channel that generated the interrupt and the ADC Analog Input that is currently undergoing conversion. Reads from this register reset the Interrupt Request Indicator bits (IRQA, IRQ1, and IRQ0) to 0. Therefore, software interrupt service routines that read this register must process all three interrupt sources from the DMA.

Table 79. DMA_ADC Status Register (DMAA_STAT)

BITS	7	6	5	4	3	2	1	0
FIELD	CADC[3:0]				Reserved	IRQA	IRQ1	IRQ0
RESET	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R
ADDR	FBFH							

CADC[3:0]—Current ADC Analog Input

This field identifies the Analog Input that the ADC is currently converting.

Reserved

This bit is reserved and must be 0.

IRQA—DMA_ADC Interrupt Request Indicator

This bit is automatically reset to 0 each time a read from this register occurs.

0 = DMA_ADC is not the source of the interrupt from the DMA Controller.

1 = DMA_ADC completed transfer of data from the last ADC Analog Input and generated an interrupt.

IRQ1—DMA1 Interrupt Request Indicator

This bit is automatically reset to 0 each time a read from this register occurs.

0 = DMA1 is not the source of the interrupt from the DMA Controller.

1 = DMA1 completed transfer of data to/from the End Address and generated an interrupt.

IRQ0—DMA0 Interrupt Request Indicator

This bit is automatically reset to 0 each time a read from this register occurs.

0 = DMA0 is not the source of the interrupt from the DMA Controller.

1 = DMA0 completed transfer of data to/from the End Address and generated an interrupt.

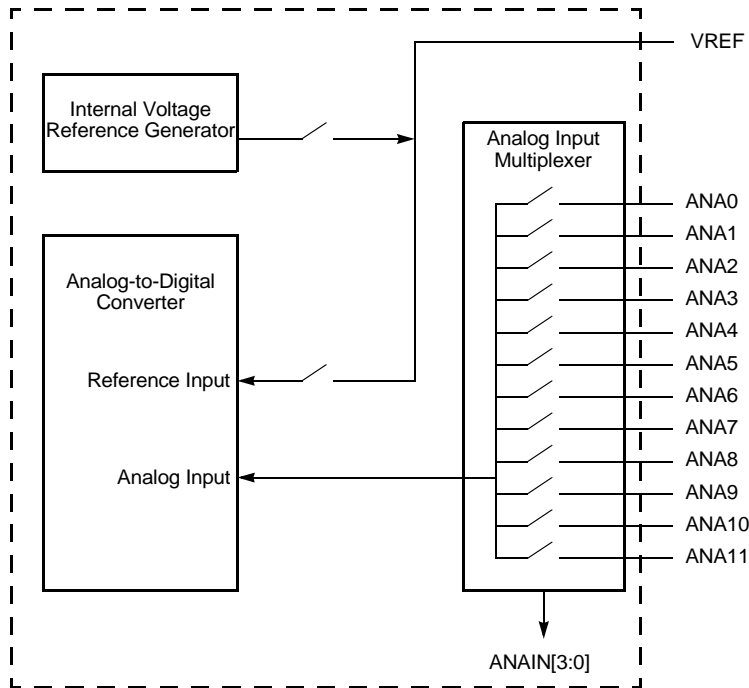


Figure 83. Analog-to-Digital Converter Block Diagram

Operation

Automatic Power-Down

If the ADC is idle (no conversions in progress) for 160 consecutive system clock cycles, portions of the ADC are automatically powered-down. From this power-down state, the ADC requires 40 system clock cycles to power-up. The ADC powers up when a conversion is requested using the ADC Control register.

Single-Shot Conversion

When configured for single-shot conversion, the ADC performs a single analog-to-digital conversion on the selected analog input channel. After completion of the conversion, the ADC shuts down. The steps for setting up the ADC and initiating a single-shot conversion are as follows:

Flash Control Register Definitions

Flash Control Register

The Flash Controller must be unlocked via the Flash Control register before programming or erasing the Flash memory. Writing the sequence 73H 8CH, sequentially, to the Flash Control register unlocks the Flash Controller. When the Flash Controller is unlocked, writing to the Flash Control register can initiate either Page Erase or Mass Erase of the Flash memory. Writing an invalid value or an invalid sequence returns the Flash Controller to its locked state. The Write-only Flash Control Register shares its Register File address with the Read-only Flash Status Register.

Table 85. Flash Control Register (FCTL)

BITS	7	6	5	4	3	2	1	0
FIELD	FCMD							
RESET	0	0	0	0	0	0	0	0
R/W	W	W	W	W	W	W	W	W
ADDR	FF8H							

FCMD—Flash Command

73H = First unlock command.

8CH = Second unlock command.

95H = Page erase command (must be third command in sequence to initiate Page Erase).

63H = Mass erase command (must be third command in sequence to initiate Mass Erase).

Flash Frequency High and Low Byte Registers

The Flash Frequency High and Low Byte registers combine to form a 16-bit value, FFREQ, to control timing for Flash program and erase operations. The 16-bit binary Flash Frequency value must contain the system clock frequency (in kHz) and is calculated using the following equation:

$$\text{FFREQ}[15:0] = \{\text{FFREQH}[7:0], \text{FFREQL}[7:0]\} = \frac{\text{System Clock Frequency}}{1000}$$



Caution: Flash programming and erasure is not supported for system clock frequencies below 32KHz (32768Hz) or above 20MHz. The Flash Frequency High and Low Byte registers must be loaded with the correct value to insure proper operation of the Z8F640x family device.

Table 88. Flash Frequency High Byte Register (FFREQH)

BITS	7	6	5	4	3	2	1	0
FIELD	FFREQH							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	FFAH							

FFREQH—Flash Frequency High Byte
High byte of the 16-bit Flash Frequency value.

Table 89. Flash Frequency Low Byte Register (FFREQL)

BITS	7	6	5	4	3	2	1	0
FIELD	FFREQL							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	FFBH							

FFREQL—Flash Frequency Low Byte
Low byte of the 16-bit Flash Frequency value.

Figure 92 illustrates the typical current consumption in Halt mode while operating at 25°C, 3.3V, versus the system clock frequency.

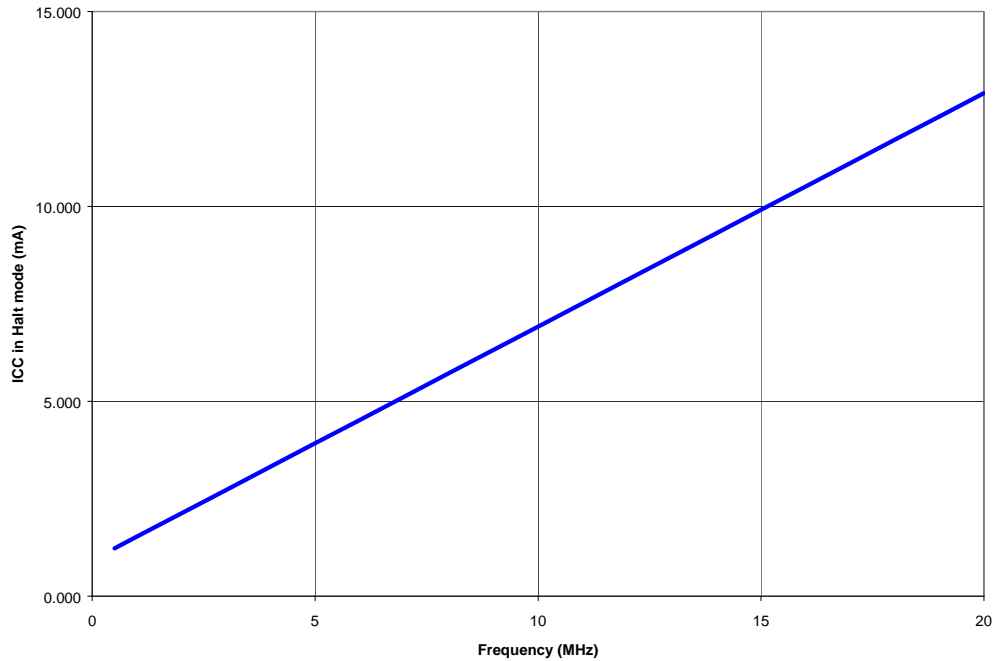


Figure 92. Nominal Halt Mode ICC Versus System Clock Frequency

Table 115. Notational Shorthand

Notation	Description	Operand	Range
b	Bit	b	b represents a value from 0 to 7 (000B to 111B).
cc	Condition Code	—	See Condition Codes overview in the eZ8 CPU User Manual.
DA	Direct Address	Addr	Addr. represents a number in the range of 0000H to FFFFH
ER	Extended Addressing Register	Reg	Reg. represents a number in the range of 000H to FFH
IM	Immediate Data	#Data	Data is a number between 00H to FFH
Ir	Indirect Working Register	@Rn	n = 0 –15
IR	Indirect Register	@Reg	Reg. represents a number in the range of 00H to FFH
Irr	Indirect Working Register Pair	@RRp	p = 0, 2, 4, 6, 8, 10, 12, or 14
IRR	Indirect Register Pair	@Reg	Reg. represents an even number in the range 00H to FEH
p	Polarity	p	Polarity is a single bit binary value of either 0B or 1B.
r	Working Register	Rn	n = 0 – 15
R	Register	Reg	Reg. represents a number in the range of 00H to FFH
RA	Relative Address	X	X represents an index in the range of +127 to –128 which is an offset relative to the address of the next instruction
rr	Working Register Pair	RRp	p = 0, 2, 4, 6, 8, 10, 12, or 14
RR	Register Pair	Reg	Reg. represents an even number in the range of 00H to FEH
Vector	Vector Address	Vector	Vector represents a number in the range of 00H to FFH
X	Indexed	#Index	The register or register pair to be indexed is offset by the signed Index value (#Index) in a +127 to -128 range.

Table 116 contains additional symbols that are used throughout the Instruction Summary and Instruction Set Description sections.



Table 128. Ordering Information (Continued)

Part	Flash KB (Bytes)	RAM KB (Bytes)	Max. Speed (MHz)	Temp (°C)	Voltage (V)	Package	Part Number
Z8 Encore!® with 64KB Flash, Standard Temperature							
Z8 Encore!®	64 (65,536)	4 (4096)	20	0 to +70	3.0 - 3.6	PDIP-40	Z8F6401PM020SC
Z8 Encore!®	64 (65,536)	4 (4096)	20	0 to +70	3.0 - 3.6	LQFP-44	Z8F6401AN020SC
Z8 Encore!®	64 (65,536)	4 (4096)	20	0 to +70	3.0 - 3.6	PLCC-44	Z8F6401VN020SC
Z8 Encore!®	64 (65,536)	4 (4096)	20	0 to +70	3.0 - 3.6	LQFP-64	Z8F6402AR020SC
Z8 Encore!®	64 (65,536)	4 (4096)	20	0 to +70	3.0 - 3.6	PLCC-68	Z8F6402VS020SC
Z8 Encore!®	64 (65,536)	4 (4096)	20	0 to +70	3.0 - 3.6	QFP-80	Z8F6403FT020SC
Z8 Encore!® with 16KB Flash, Extended Temperature							
Z8 Encore!®	16 (16,384)	2 (2048)	20	-40 to +105	3.0 - 3.6	PDIP-40	Z8F1601PM020EC
Z8 Encore!®	16 (16,384)	2 (2048)	20	-40 to +105	3.0 - 3.6	LQFP-44	Z8F1601AN020EC
Z8 Encore!®	16 (16,384)	2 (2048)	20	-40 to +105	3.0 - 3.6	PLCC-44	Z8F1601VN020EC
Z8 Encore!®	16 (16,384)	2 (2048)	20	-40 to +105	3.0 - 3.6	LQFP-64	Z8F1602AR020EC
Z8 Encore!®	16 (16,384)	2 (2048)	20	-40 to +105	3.0 - 3.6	PLCC-68	Z8F1602VS020EC
Z8 Encore!® with 24KB Flash, Extended Temperature							
Z8 Encore!®	24 (24,576)	2 (2048)	20	-40 to +105	3.0 - 3.6	PDIP-40	Z8F2401PM020EC
Z8 Encore!®	24 (24,576)	2 (2048)	20	-40 to +105	3.0 - 3.6	LQFP-44	Z8F2401AN020EC
Z8 Encore!®	24 (24,576)	2 (2048)	20	-40 to +105	3.0 - 3.6	PLCC-44	Z8F2401VN020EC
Z8 Encore!®	24 (24,576)	2 (2048)	20	-40 to +105	3.0 - 3.6	LQFP-64	Z8F2402AR020EC
Z8 Encore!®	24 (24,576)	2 (2048)	20	-40 to +105	3.0 - 3.6	PLCC-68	Z8F2402VS020EC
Z8 Encore!® with 32KB Flash, Extended Temperature							
Z8 Encore!®	32 (32,768)	2 (2048)	20	-40 to +105	3.0 - 3.6	PDIP-40	Z8F3201PM020EC
Z8 Encore!®	32 (32,768)	2 (2048)	20	-40 to +105	3.0 - 3.6	LQFP-44	Z8F3201AN020EC
Z8 Encore!®	32 (32,768)	2 (2048)	20	-40 to +105	3.0 - 3.6	PLCC-44	Z8F3201VN020EC
Z8 Encore!®	32 (32,768)	2 (2048)	20	-40 to +105	3.0 - 3.6	LQFP-64	Z8F3202AR020EC
Z8 Encore!®	32 (32,768)	2 (2048)	20	-40 to +105	3.0 - 3.6	PLCC-68	Z8F3202VS020EC



- extended addressing register 184
- external pin reset 29
- eZ8 CPU features 3
- eZ8 CPU instruction classes 187
- eZ8 CPU instruction notation 183
- eZ8 CPU instruction set 182
- eZ8 CPU instruction summary 191

F

- FCTL register 144
- features, Z8 Encore!® 1
- first opcode map 204
- FLAGS 185
- flags register 185
- flash
 - controller 4
 - option bit address space 148
 - option bit configuration - reset 148
 - program memory address 0000H 149
 - program memory address 0001H 150
- flash memory 138
 - arrangement 139
 - byte programming 142
 - code protection 141
 - configurations 138
 - control register definitions 144
 - controller bypass 143
 - electrical characteristics and timing 173
 - flash control register 144
 - flash option bits 142
 - flash status register 145
 - flow chart 140
 - frequency high and low byte registers 147
 - mass erase 143
 - operation 139
 - operation timing 141
 - page erase 143
 - page select register 146
- FPS register 146
- FSTAT register 145

G

- gated mode 71
- general-purpose I/O 33
- GPIO 4, 33
 - alternate functions 34
 - architecture 34
 - control register definitions 36
 - input data sample timing 176
 - interrupts 36
 - port A-H address registers 37
 - port A-H alternate function sub-registers 39
 - port A-H control registers 38
 - port A-H data direction sub-registers 39
 - port A-H high drive enable sub-registers 41
 - port A-H input data registers 42
 - port A-H output control sub-registers 40
 - port A-H output data registers 43
 - port A-H stop mode recovery sub-registers 41
 - port availability by device 33
 - port input timing 176
 - port output timing 177

H

- H 185
- HALT 189
- HALT mode 31, 189
- hexadecimal number prefix/suffix 185

I

- I²C 4
 - 10-bit address read transaction 116
 - 10-bit address transaction 114
 - 10-bit addressed slave data transfer format 114
 - 10-bit receive data format 116
 - 7-bit address transaction 112
 - 7-bit address, reading a transaction 115
 - 7-bit addressed slave data transfer format 113
 - 7-bit receive data transfer format 115
 - baud high and low byte registers 121
 - C status register 118
 - control register definitions 118



- SDA and SCL (IrDA) signals 111
 - second opcode map after 1FH 205
 - serial clock 101
 - serial peripheral interface (SPI) 99
 - set carry flag 188, 189
 - set register pointer 189
 - shift right arithmetic 191
 - shift right logical 191
 - signal descriptions 13
 - single assertion (pulse) interrupt sources 47
 - single-shot conversion (ADC) 133
 - SIO 5
 - slave data transfer formats (I2C) 114
 - slave select 102
 - software trap 190
 - source operand 185
 - SP 185
 - SPI
 - architecture 99
 - baud rate generator 105
 - baud rate high and low byte register 110
 - clock phase 102
 - configured as slave 100
 - control register 107
 - control register definitions 106
 - data register 106
 - error detection 105
 - interrupts 105
 - mode fault error 105
 - mode register 109
 - multi-master operation 104
 - operation 100
 - overflow error 105
 - signals 101
 - single master, multiple slave system 100
 - single master, single slave system 99
 - status register 108
 - timing, PHASE = 0 103
 - timing, PHASE=1 104
 - SPI controller signals 13
 - SPI mode (SPIMODE) 109
 - SPIBRH register 110
 - SPIBRL register 110
 - SPICTL register 107
 - SPIDATA register 106
 - SPIMODE register 109
 - SPISTAT register 108
 - SRA 191
 - src 185
 - SRL 191
 - SRP 189
 - SS, SPI signal 101
 - stack pointer 185
 - status register, I2C 118
 - STOP 189
 - stop mode 31, 189
 - stop mode recovery
 - sources 29
 - using a GPIO port pin transition 30
 - using watch-dog timer time-out 29
 - SUB 188
 - subtract 188
 - subtract - extended addressing 188
 - subtract with carry 188
 - subtract with carry - extended addressing 188
 - SUBX 188
 - SWAP 191
 - swap nibbles 191
 - symbols, additional 185
 - system and short resets 26
- T**
- TCM 188
 - TCMX 188
 - technical support 213
 - test complement under mask 188
 - test under mask 188
 - timer signals 14
 - timers 5, 57
 - architecture 57
 - block diagram 58
 - capture mode 62, 71
 - capture/compare mode 65, 71
 - compare mode 63, 71
 - continuous mode 59, 70
 - counter mode 60
 - counter modes 70