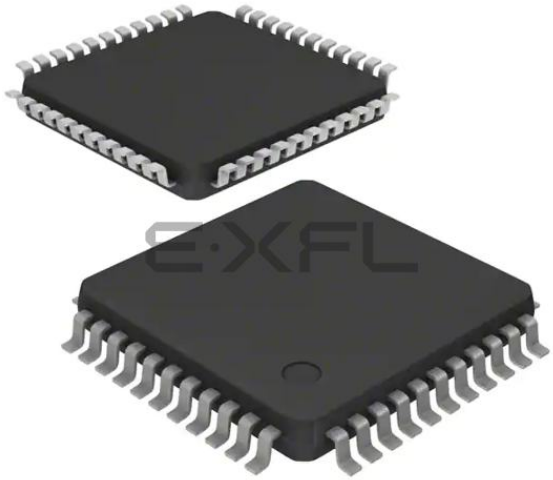

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | eZ8 |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | I²C, IrDA, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 31 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 8x10b |
| Oscillator Type | Internal |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-LQFP |
| Supplier Device Package | 44-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z8f3201an020sc00tr |

- Power-On Reset (POR)
- 3.0-3.6V operating voltage with 5V-tolerant inputs
- 0° to +70°C standard temperature and -40° to +105°C extended temperature operating ranges

## Part Selection Guide

Table 1 identifies the basic features and package styles available for each device within the Z8F640x family product line.

**Table 1. Z8F640x Family Part Selection Guide**

| Part Number | Flash (KB) | RAM (KB) | I/O | 16-bit Timers with PWM | ADC Inputs | UARTs with IrDA | $I^2C$ | SPI | 40/44-pin packages | 64/68-pin packages | 80-pin package |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Z8F1601 | 16 | 2 | 31 | 3 | 8 | 2 | 1 | 1 | X | | |
| Z8F1602 | 16 | 2 | 46 | 4 | 12 | 2 | 1 | 1 | | X | |
| Z8F2401 | 24 | 2 | 31 | 3 | 8 | 2 | 1 | 1 | X | | |
| Z8F2402 | 24 | 2 | 46 | 4 | 12 | 2 | 1 | 1 | | X | |
| Z8F3201 | 32 | 2 | 31 | 3 | 8 | 2 | 1 | 1 | X | | |
| Z8F3202 | 32 | 2 | 46 | 4 | 12 | 2 | 1 | 1 | | X | |
| Z8F4801 | 48 | 4 | 31 | 3 | 8 | 2 | 1 | 1 | X | | |
| Z8F4802 | 48 | 4 | 46 | 4 | 12 | 2 | 1 | 1 | | X | |
| Z8F4803 | 48 | 4 | 60 | 4 | 12 | 2 | 1 | 1 | | | X |
| Z8F6401 | 64 | 4 | 31 | 3 | 8 | 2 | 1 | 1 | X | | |
| Z8F6402 | 64 | 4 | 46 | 4 | 12 | 2 | 1 | 1 | | X | |
| Z8F6403 | 64 | 4 | 60 | 4 | 12 | 2 | 1 | 1 | | | X |

**Table 3. Pin Characteristics of the Z8F640x family**

| Symbol Mnemonic | Direction | Reset Direction | Active Low or Active High | Tri-State Output | Internal Pull-up or Pull-down | Schmitt Trigger Input | Open Drain Output |
|---|---|---|---|---|---|---|---|
| PF[7:0] | I/O | I | N/A | Yes | No | Yes | Yes, Programmable |
| PG[7:0] | I/O | I | N/A | Yes | No | Yes | Yes, Programmable |
| PH[3:0] | I/O | I | N/A | Yes | No | Yes | Yes, Programmable |
| $\overline{\text{RESET}}$ | I | I | Low | N/A | Pull-up | Yes | N/A |
| VDD | N/A | N/A | N/A | N/A | No | No | N/A |
| XIN | I | I | N/A | N/A | No | No | N/A |
| XOUT | O | O | N/A | Yes, in Stop mode | No | No | No |

*x* represents integer 0, 1,... to indicate multiple pins with symbol mnemonics that differ only by the integer

Middle byte, Bits[15:8], of the 24-bit WDT reload value.

**Table 49. Watch-Dog Timer Reload Low Byte Register (WDTL)**

| BITS | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| FIELD | WDTL | | | | | | | |
| RESET | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| R/W | R/W* | R/W* | R/W* | R/W* | R/W* | R/W* | R/W* | R/W* |
| ADDR | FF3H | | | | | | | |
| R/W* - Read returns the current WDT count value. Write sets the desired Reload Value. | | | | | | | | |

WDTL—WDT Reload Low

Least significant byte (LSB), Bits[7:0], of the 24-bit WDT reload value.

**Table 53. UART*x* Status 1 Register (U*x*STAT1)**

| BITS | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| FIELD | Reserved | | | | | | | MPRX |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R | R | R | R | R | R | R | R |
| ADDR | F44H and F4CH | | | | | | | |

Reserved
These bits are reserved and must be 0.

MPRX—Multiprocessor Receive
This status bit is for the receiver and reflects the actual status of the last multiprocessor bit received. Reading from the UART Data register resets this bit to 0.

## UART*x* Control 0 and Control 1 Registers

The UART*x* Control 0 and Control 1 registers (Tables 54 and 55) configure the properties of the UART's transmit and receive operations. The UART Control registers must ben be written while the UART is enabled.

**Table 54. UART*x* Control 0 Register (U*x*CTL0)**

| BITS | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| FIELD | TEN | REN | CTSE | PEN | PSEL | SBRK | STOP | LBEN |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| ADDR | F42H and F4AH | | | | | | | |

TEN—Transmit Enable
This bit enables or disables the transmitter. The enable is also controlled by the $\overline{\text{CTS}}$ signal and the CTSE bit. If the $\overline{\text{CTS}}$ signal is low and the CTSE bit is 1, the transmitter is enabled.
0 = Transmitter disabled.
1 = Transmitter enabled.

REN—Receive Enable
This bit enables or disables the receiver.
0 = Receiver disabled.
1 = Receiver enabled.

# *Infrared Encoder/Decoder*

## Overview

The Z8F640x family products contain two fully-functional, high-performance UART to Infrared Encoder/Decoders (Endecs). Each Infrared Endec is integrated with an on-chip UART to allow easy communication between the Z8F640x family device and IrDA Physical Layer Specification Version 1.3-compliant infrared transceivers. Infrared communication provides secure, reliable, low-cost, point-to-point communication between PCs, PDAs, cell phones, printers and other infrared enabled devices.

## Architecture

Figure 71 illustrates the architecture of the Infrared Endec.

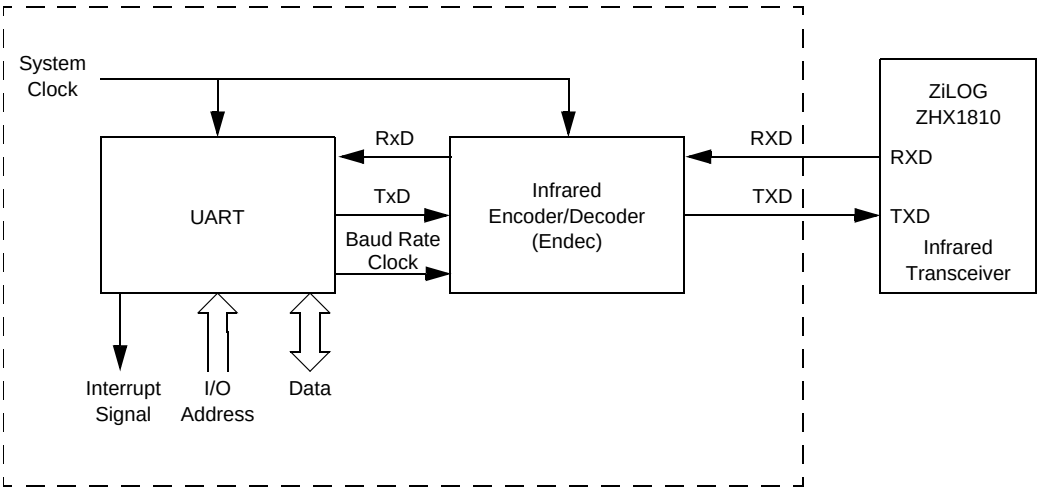


**Figure 71. Infrared Data Communication System Block Diagram**

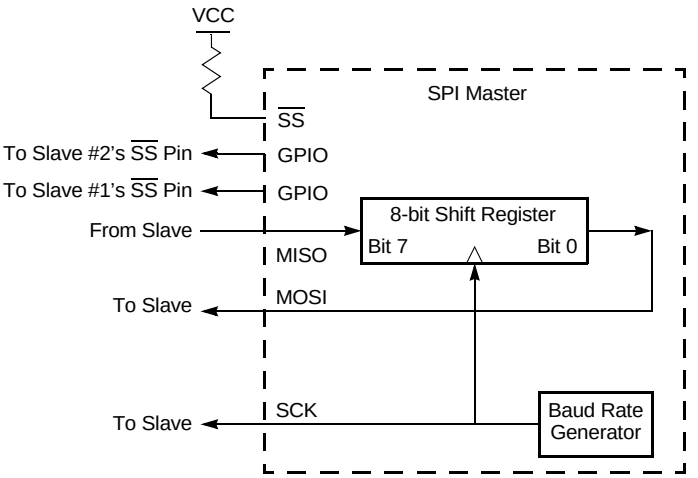


**Figure 75. SPI Configured as a Master in a Single Master, Multiple Slave System**

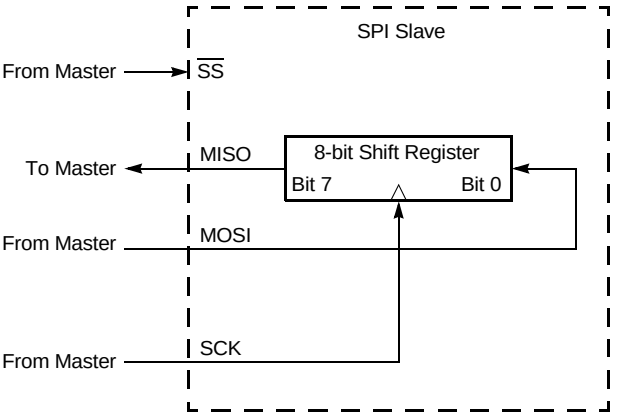


**Figure 76. SPI Configured as a Slave**

## Operation

The SPI is a full-duplex, synchronous, character-oriented channel that supports a four-wire interface (serial clock, transmit, receive and Slave select). The SPI block consists of trans-

1. Disable the SPI by clearing the SPIEN bit in the SPI Control register to 0.
2. Load the desired 16-bit count value into the SPI Baud Rate High and Low Byte registers.
3. Enable the Baud Rate Generator timer function and associated interrupt by setting the BIRQ bit in the SPI Control register to 1.

## SPI Control Register Definitions

### SPI Data Register

The SPI Data register stores both the outgoing (transmit) data and the incoming (received) data. Reads from the SPI Data register always return the current contents of the 8-bit shift register.

With the SPI configured as a Master, writing a data byte to this register initiates the data transmission. With the SPI configured as a Slave, writing a data byte to this register loads the shift register in preparation for the next data transfer with the external Master. In either the Master or Slave modes, if a transmission is already in progress, writes to this register are ignored and the Overrun error flag, OVR, is set in the SPI Status register.

When the character length is less than 8 bits (as set by the NUMBITS field in the SPI Mode register), the transmit character must be left justified in the SPI Data register. A received character of less than 8 bits will be right justified. For example, if the SPI is configured for 4-bit characters, the transmit characters must be written to SPIDATA[7:4] and the received characters are read from SPIDATA[3:0].

**Table 60. SPI Data Register (SPIDATA)**

| BITS | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| FIELD | DATA | | | | | | | |
| RESET | X | X | X | X | X | X | X | X |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| ADDR | F60H | | | | | | | |

DATA—Data
Transmit and/or receive data.

## SPI Control Register

The SPI Control register configures the SPI for transmit and receive operations.

**Table 61. SPI Control Register (SPICTL)**

| BITS | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| FIELD | IRQE | STR | BIRQ | PHASE | CLKPOL | WOR | MMEN | SPIEN |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| ADDR | F61H | | | | | | | |

IRQE—Interrupt Request Enable
0 = SPI interrupts are disabled. No interrupt requests are sent to the Interrupt Controller.
1 = SPI interrupts are enabled. Interrupt requests are sent to the Interrupt Controller.

STR—Start an SPI Interrupt Request
0 = No effect.
1 = Setting this bit to 1 also sets the IRQ bit in the SPI Status register to 1. Setting this bit forces the SPI to send an interrupt request to the Interrupt Control. This bit can be used by software for a function similar to transmit buffer empty in a UART.

BIRQ—BRG Timer Interrupt Request
If the SPI is enabled, this bit has no effect. If the SPI is disabled:
0 = The Baud Rate Generator timer function is disabled.
1 = The Baud Rate Generator timer function and time-out interrupt are enabled.

PHASE—Phase Select
Sets the phase relationship of the data to the clock. Refer to the **SPI Clock Phase and Polarity Control** section for more information on operation of the PHASE bit.

CLKPOL—Clock Polarity
0 = SCK idles Low (0).
1 = SCK idle High (1).

WOR—Wire-OR (Open-Drain) Mode Enabled
0 = SPI signal pins not configured for open-drain.
1 = All four SPI signal pins (SCK, $\overline{SS}$, MISO, MOSI) configured for open-drain function. This setting is typically used for multi-master and/or multi-slave configurations.

MMEN—SPI Master Mode Enable
0 = SPI configured in Slave mode.
1 = SPI configured in Master mode.

1 = DMA*x* is enabled and initiates a data transfer upon receipt of a request from the trigger source.

DLE—DMA*x* Loop Enable
0 = DMA*x* reloads the original Start Address and is then disabled after the End Address data is transferred.
1 = DMA*x*, after the End Address data is transferred, reloads the original Start Address and continues operating.

DDIR—DMA*x* Data Transfer Direction
0 = Register File → on-chip peripheral control register.
1 = on-chip peripheral control register → Register File.

IRQEN—DMA*x* Interrupt Enable
0 = DMA*x* does not generate any interrupts.
1 = DMA*x* generates an interrupt when the End Address data is transferred.

WSEL—Word Select
0 = DMA*x* transfers a single byte per request.
1 = DMA*x* transfers a two-byte word per request. The address for the on-chip peripheral control register must be an even address.

RSS—Request Trigger Source Select
The Request Trigger Source Select field determines the peripheral that can initiate a DMA request transfer. The corresponding interrupts do not need to be enabled within the Interrupt Controller to initiate a DMA transfer. However, if the Request Trigger Source can enable or disable the interrupt request sent to the Interrupt Controller, the interrupt request must be enabled within the Request Trigger Source block.
000 = Timer 0.
001 = Timer 1.
010 = Timer 2.
011 = Timer 3.
100 = DMA0 Control register: UART0 Received Data register contains valid data. DMA1 Control register: UART0 Transmit Data register empty.
101 = DMA0 Control register: UART1 Received Data register contains valid data. DMA1 Control register: UART1 Transmit Data register empty.
110 = DMA0 Control register: $I^2C$ Receiver Interrupt. DMA1 Control register: $I^2C$ Transmitter Interrupt register empty.
111 = Reserved.

## DMA*x* I/O Address Register

The DMA*x* I/O Address register contains the low byte of the on-chip peripheral address for data transfer. The full 12-bit Register File address is given by {FH, DMA*x*_IO[7:0]}.

## DMA_ADC Control Register

The DMA_ADC Control register enables and sets options (DMA enable and interrupt enable) for ADC operation.

**Table 78. DMA_ADC Control Register (DMAACTL)**

| BITS | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| FIELD | DAEN | IRQEN | Reserved | | ADC_IN | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| ADDR | FBEH | | | | | | | |

DAEN—DMA_ADC Enable
0 = DMA_ADC is disabled and the ADC Analog Input Number (ADC_IN) is reset to 0.
1 = DMA_ADC is enabled.

IRQEN—Interrupt Enable
0 = DMA_ADC does not generate any interrupts.
1 = DMA_ADC generates an interrupt after transferring data from the last ADC Analog Input specified by the ADC_IN field.

Reserved
These bits are reserved and must be 0.

ADC_IN—ADC Analog Input Number
These bits set the number of ADC Analog Inputs to be used in the continuous update (data conversion followed by DMA data transfer). The conversion always begins with ADC Analog Input 0 and then progresses sequentially through the other selected ADC Analog Inputs.
0000 = ADC Analog Input 0 updated.
0001 = ADC Analog Inputs 0-1 updated.
0010 = ADC Analog Inputs 0-2 updated.
0011 = ADC Analog Inputs 0-3 updated.
0100 = ADC Analog Inputs 0-4 updated.
0101 = ADC Analog Inputs 0-5 updated.
0110 = ADC Analog Inputs 0-6 updated.
0111 = ADC Analog Inputs 0-7 updated.
1000 = ADC Analog Inputs 0-8 updated.
1001 = ADC Analog Inputs 0-9 updated.
1010 = ADC Analog Inputs 0-10 updated.
1011 = ADC Analog Inputs 0-11 updated.
1100-1111 = Reserved.

1. Enable the desired analog inputs by configuring the general-purpose I/O pins for alternate function. This configuration disables the digital input and output drivers.
2. Write to the ADC Control register to configure the ADC and begin the conversion. The bit fields in the ADC Control register can be written simultaneously:
   – Write to ANAIN[3:0] to select one of the 12 analog input sources.
   – Clear CONT to 0 to select a single-shot conversion.
   – Write to VREF to enable or disable the internal voltage reference generator.
   – Set CEN to 1 to start the conversion.
3. CEN remains 1 while the conversion is in progress. A single-shot conversion requires 5129 system clock cycles to complete. If a single-shot conversion is requested from an ADC powered-down state, the ADC uses 40 additional clock cycles to power-up before beginning the 5129 cycle conversion.
4. When the conversion is complete, the ADC control logic performs the following operations:
   – 10-bit data result written to {ADCD_H[7:0], ADCD_L[7:6]}.
   – CEN resets to 0 to indicate the conversion is complete.
   – An interrupt request is sent to the Interrupt Controller.
5. If the ADC remains idle for 160 consecutive system clock cycles, it is automatically powered-down.

## Continuous Conversion

When configured for continuous conversion, the ADC continuously performs an analog-to-digital conversion on the selected analog input. Each new data value over-writes the previous value stored in the ADC Data registers. An interrupt is generated only at the end of the first conversion after enabling.

**Caution:** In Continuous mode, users must be aware that ADC updates are limited by the input signal bandwidth of the ADC and the latency of the ADC and its digital filter. Step changes at the input are not seen at the next output from the ADC. The response of the ADC (in all modes) is limited by the input signal bandwidth and the latency.

The steps for setting up the ADC and initiating continuous conversion are as follows:

1. Enable the desired analog input by configuring the general-purpose I/O pins for alternate function. This disables the digital input and output driver.
2. Write to the ADC Control register to configure the ADC for continuous conversion. The bit fields in the ADC Control register may be written simultaneously:
   – Write to ANAIN[3:0] to select one of the 12 analog input sources.

– Set CONT to 1 to select continuous conversion.
– Write to VREF to enable or disable the internal voltage reference generator.
– Set CEN to 1 to start the conversions.

3. When the first conversion in continuous operation is complete (after 5129 system clock cycles, plus the 40 cycles for power-up, if necessary), the ADC control logic performs the following operations:
   – CEN resets to 0 to indicate the first conversion is complete. CEN remains 0 for all subsequent conversions in continuous operation.
   – An interrupt request is sent to the Interrupt Controller to indicate the ***first*** conversion is complete. An interrupt request is not sent for subsequent conversions in continuous operation.
4. Thereafter, the ADC writes a new 10-bit data result to {ADCD_H[7:0], ADCD_L[7:6]} every 256 system clock cycles.
5. To disable continuous conversion, clear the CONT bit in the ADC Control register to 0.

### DMA Control of the ADC

The Direct Memory Access (DMA) Controller can control operation of the ADC including analog input selection and conversion enable. For more information on the DMA and configuring for ADC operations refer to the **Direct Memory Access Controller** chapter.

## ADC Control Register Definitions

### ADC Control Register

The ADC Control register selects the analog input channel and initiates the analog-to-digital conversion.

**Table 80. ADC Control Register (ADCCTL)**

| BITS | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| FIELD | CEN | Reserved | $\overline{\text{VREF}}$ | CONT | ANAIN[3:0] | | | |
| RESET | 0 | 0 | 0 | 0 | 0000 | | | |
| R/W | R/W | R/W | R/W | R/W | R/W | | | |
| ADDR | F70H | | | | | | | |

CEN—Conversion Enable
0 = Conversion is complete. Writing a 0 produces no effect. The ADC automatically clears

**Caution:** The byte at each address of the Flash memory cannot be programmed (any bits written to 0) more than twice before an erase cycle occurs.

### Page Erase

The Flash memory can be erased one page (512 bytes) at a time. Page Erasing the Flash memory sets all bytes in that page to the value FFH. The Flash Page Select register identifies the page to be erased. With the Flash Controller unlocked, writing the value 95H to the Flash Control register initiates the Page Erase operation. While the Flash Controller executes the Page Erase operation, the eZ8 CPU idles but the system clock and on-chip peripherals continue to operate. The eZ8 CPU resumes operation after the Page Erase operation completes. If the Page Erase operation is performed through the On-Chip Debugger, poll the Flash Status register to determine when the Page Erase operation is complete. When the Page Erase is complete, the Flash Controller returns to its locked state.

### Mass Erase

The Flash memory can also be Mass Erased using the Flash Controller. Mass Erasing the Flash memory sets all bytes to the value FFH. With the Flash Controller unlocked, writing the value 63H to the Flash Control register initiates the Mass Erase operation. While the Flash Controller executes the Mass Erase operation, the eZ8 CPU idles but the system clock and on-chip peripherals continue to operate. Typically, the Flash Memory is Mass Erased using the On-Chip Debugger. Via the On-Chip Debugger, poll the Flash Status register to determine when the Mass Erase operation is complete. Although the Flash can be Mass Erased by user program code, when the Mass Erase is complete the user program code is completely erased. When the Mass Erase is complete, the Flash Controller returns to its locked state.

### Flash Controller Bypass

The Flash Controller can be bypassed and the control signals for the Flash memory brought out to the GPIO pins. Bypassing the Flash Controller allows faster Row Programming algorithms by controlling the Flash programming signals directly.

Row programing is recommended for gang programming applications and large volume customers who do not require in-circuit initial programming of the Flash memory. Mass Erase and Page Erase operations are also supported when the Flash Controller is bypassed.

Please refer to the document entitled *Third-Party Flash Programming Support for Z8 Encore!*™ for more information on bypassing the Flash Controller. This document is available for download at www.zilog.com.

### Program Memory Address 0000H

**Table 90. Option Bits At Program Memory Address 0000H**

| BITS | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| FIELD | WDT_RES | WDT_AO | Reserved | | | RP | FHSWP | FWP |
| RESET | U | U | U | U | U | U | U | U |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| ADDR | Program Memory 0000H | | | | | | | |

Note: U = Unchanged by Reset. R/W = Read/Write.

WDT_RES—Watch-Dog Timer Reset
0 = Watch-Dog Timer time-out generates an interrupt request. Interrupts must be globally enabled for the eZ8 CPU to acknowledge the interrupt request.
1 = Watch-Dog Timer time-out causes a Short Reset. This setting is the default for unprogrammed (erased) Flash.

WDT_AO—Watch-Dog Timer Always On
0 = Watch-Dog Timer is automatically enabled upon application of system power. Watch-Dog Timer can not be disabled.
1 = Watch-Dog Timer is enabled upon execution of the WDT instruction. Once enabled, the Watch-Dog Timer can only be disabled by a Reset or Stop Mode Recovery. This setting is the default for unprogrammed (erased) Flash.

Reserved
These Option Bits are reserved for future use and must always be set to 1. This setting is the default for unprogrammed (erased) Flash.

RP—Read Protect
0 = User program code is inaccessible. Limited control features are available through the On-Chip Debugger.
1 = User program code is accessible. All On-Chip Debugger commands are enabled. This setting is the default for unprogrammed (erased) Flash.

- Power-on reset
- Voltage Brownout reset
- Asserting the $\overline{\text{RESET}}$ pin Low to initiate a Reset.
- Driving the DBG pin Low while the Z8F640x family device is in Stop mode initiates a System Reset.

## OCD Data Format

The OCD interface uses the asynchronous data format defined for RS-232. Each character is transmitted as 1 Start bit, 8 data bits (least-significant bit first), and 1.5 Stop bits (Figure 89)

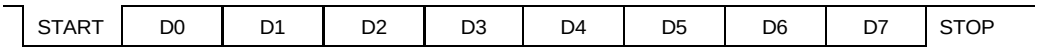


**Figure 89. OCD Data Format**

## OCD Auto-Baud Detector/Generator

To run over a range of baud rates (data bits per second) with various system clock frequencies, the On-Chip Debugger has an Auto-Baud Detector/Generator. After a reset, the OCD is idle until it receives data. The OCD requires that the first character sent from the host is the character 80H. The character 80H has eight continuous bits Low (one Start bit plus 7 data bits). The Auto-Baud Detector measures this period and sets the OCD Baud Rate Generator accordingly.

The Auto-Baud Detector/Generator is clocked by the Z8F640x family device system clock. The minimum baud rate is the system clock frequency divided by 512. For optimal operation, the maximum recommended baud rate is the system clock frequency divided by 8. The theoretical maximum baud rate is the system clock frequency divided by 4. This theoretical maximum is possible for low noise designs with clean signals. Table 92 lists minimum and recommended maximum baud rates for sample crystal frequencies.

**Table 92. OCD Baud-Rate Limits**

| System Clock Frequency (MHz) | Recommended Maximum Baud Rate (kbits/s) | Minimum Baud Rate (kbits/s) |
|---|---|---|
| 20.0 | 2500 | 39.1 |
| 1.0 | 125.0 | 1.96 |
| 0.032768 (32KHz) | 4.096 | 0.064 |

**Table 100. Absolute Maximum Ratings**

| Parameter | Minimum | Maximum | Units | Notes |
|---|---|---|---|---|
| **68-Pin PLCC Maximum Ratings at $70^0$C to $105^0$C** | | | | |
| Total power dissipation | | 500 | mW | |
| Maximum current into $V_{DD}$ or out of $V_{SS}$ | | 140 | mA | |
| **64-Pin LQFP Maximum Ratings at -40°C to 70°C** | | | | |
| Total power dissipation | | 1000 | mW | |
| Maximum current into $V_{DD}$ or out of $V_{SS}$ | | 275 | mA | |
| **64-Pin LQFP Maximum Ratings at $70^0$C to $105^0$C** | | | | |
| Total power dissipation | | 540 | mW | |
| Maximum current into $V_{DD}$ or out of $V_{SS}$ | | 150 | mA | |
| **44-Pin PLCC Maximum Ratings at -40°C to 70°C** | | | | |
| Total power dissipation | | 750 | mW | |
| Maximum current into $V_{DD}$ or out of $V_{SS}$ | | 200 | mA | |
| **44-Pin PLCC Maximum Ratings at $70^0$C to $105^0$C** | | | | |
| Total power dissipation | | 295 | mW | |
| Maximum current into $V_{DD}$ or out of $V_{SS}$ | | 83 | mA | |
| **44-pin LQFP Maximum Ratings at -40°C to 70°C** | | | | |
| Total power dissipation | | 750 | mW | |
| Maximum current into $V_{DD}$ or out of $V_{SS}$ | | 200 | mA | |
| **44-pin LQFP Maximum Ratings at $70^0$C to $105^0$C** | | | | |
| Total power dissipation | | 410 | mW | |
| Maximum current into $V_{DD}$ or out of $V_{SS}$ | | 114 | mA | |
| **40-Pin PDIP Maximum Ratings at -40°C to 70°C** | | | | |
| Total power dissipation | | 1000 | mW | |
| Maximum current into $V_{DD}$ or out of $V_{SS}$ | | 275 | mA | |
| **40-Pin PDIP Maximum Ratings at 70°C to 105°C** | | | | |
| Total power dissipation | | 540 | mW | |
| Maximum current into $V_{DD}$ or out of $V_{SS}$ | | 150 | mA | |

Notes:
1. This voltage applies to all pins except the following: $V_{DD}$, $AV_{DD}$, pins supporting analog input (Port B and Port H), $\overline{\text{RESET}}$, and where noted otherwise.

## DC Characteristics

Table 101 lists the DC characteristics of the Z8F640x family devices. All voltages are referenced to $V_{SS}$, the primary system ground.

**Table 101. DC Characteristics**

| Symbol | Parameter | $T_A$ = -40°C to 105°C | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Minimum | Typical | Maximum | | |
| $V_{DD}$ | Supply Voltage | 3.0 | – | 3.6 | V | |
| $V_{IL1}$ | Low Level Input Voltage | -0.3 | – | 0.3*$V_{DD}$ | V | For all input pins except $\overline{\text{RESET}}$, DBG, and XIN. |
| $V_{IL2}$ | Low Level Input Voltage | -0.3 | – | 0.2*$V_{DD}$ | V | For $\overline{\text{RESET}}$, DBG, and XIN. |
| $V_{IH1}$ | High Level Input Voltage | 0.7*$V_{DD}$ | – | 5.5 | V | Port A, C, D, E, F, and G pins. |
| $V_{IH2}$ | High Level Input Voltage | 0.7*$V_{DD}$ | – | $V_{DD}$+0.3 | V | Port B and H pins. |
| $V_{IH3}$ | High Level Input Voltage | 0.8*$V_{DD}$ | – | $V_{DD}$+0.3 | V | $\overline{\text{RESET}}$, DBG, and XIN pins. |
| $V_{OL1}$ | Low Level Output Voltage | – | – | 0.4 | V | $V_{DD}$ = 3.0V; $I_{OL}$ = 2mA<br>High Output Drive disabled. |
| $V_{OH1}$ | High Level Output Voltage | 2.4 | – | – | V | $V_{DD}$ = 3.0V; $I_{OH}$ = -2mA<br>High Output Drive disabled. |
| $V_{OL2}$ | Low Level Output Voltage | – | – | 0.6 | V | $V_{DD}$ = 3.3V; $I_{OL}$ = 20mA<br>High Output Drive enabled.<br>$T_A$ = -40°C to +70°C |
| $V_{OL3}$ | Low Level Output Voltage | – | – | 0.6 | V | $V_{DD}$ = 3.3V; $I_{OL}$ = 15mA<br>High Output Drive enabled.<br>$T_A$ = 70°C to +105°C |
| $V_{OH2}$ | High Level Output Voltage | 2.4 | – | – | V | $V_{DD}$ = 3.3V; $I_{OH}$ = -20mA<br>High Output Drive enabled.<br>$T_A$ = -40°C to +70°C |
| $V_{OH3}$ | High Level Output Voltage | 2.4 | – | – | V | $V_{DD}$ = 3.3V; $I_{OH}$ = -15mA<br>High Output Drive enabled.<br>$T_A$ = 70°C to +105°C |
| $I_{IL}$ | Input Leakage Current | -5 | – | +5 | µA | $V_{DD}$ = 3.6V;<br>$V_{IN}$ = VDD or VSS[1] |
| $I_{TL}$ | Tri-State Leakage Current | -5 | – | +5 | µA | $V_{DD}$ = 3.6V |
| $C_{PAD}$ | GPIO Port Pad Capacitance | – | 8.0[2] | – | pF | |
| $C_{XIN}$ | XIN Pad Capacitance | – | 8.0[2] | – | pF | |
| $C_{XOUT}$ | XOUT Pad Capacitance | – | 9.5[2] | – | pF | |

## AC Characteristics

The section provides information on the AC characteristics and timing of the Z8 Encore!™. All AC timing information assumes a standard load of 50pF on all outputs.

**Table 102. AC Characteristics**

| Symbol | Parameter | $V_{DD}$ = 3.0 - 3.6V<br>$T_A$ =-40$^0$C to 105$^0$C | | Units | Conditions |
|---|---|---|---|---|---|
| | | Minimum | Maximum | | |
| $F_{sysclk}$ | System Clock Frequency | – | 20.0 | MHz | Read-only from Flash memory. |
| | | 0.032768 | 20.0 | MHz | Program or erasure of the Flash memory. |
| $F_{XTAL}$ | Crystal Oscillator Frequency | 1.0 | 20.0 | MHz | System clock frequencies below the crystal oscillator minimum require an external clock driver. |
| $T_{XIN}$ | System Clock Period | 50 | – | ns | $T_{CLK} = 1/F_{sysclk}$ |
| $T_{XINH}$ | System Clock High Time | 20 | 30 | ns | $T_{CLK}$ = 50ns |
| $T_{XINL}$ | System Clock Low Time | 20 | 30 | ns | $T_{CLK}$ = 50ns |
| $T_{XINR}$ | System Clock Rise Time | – | 3 | ns | $T_{CLK}$ = 50ns |
| $T_{XINF}$ | System Clock Fall Time | – | 3 | ns | $T_{CLK}$ = 50ns |

## General Purpose I/O Port Input Data Sample Timing

Figure 93 illustrates timing of the GPIO Port input sampling. The input value on a GPIO Port pin is sampled on the rising edge of the system clock. The Port value is then available to the eZ8 CPU on the second rising clock edge following the change of the Port value.

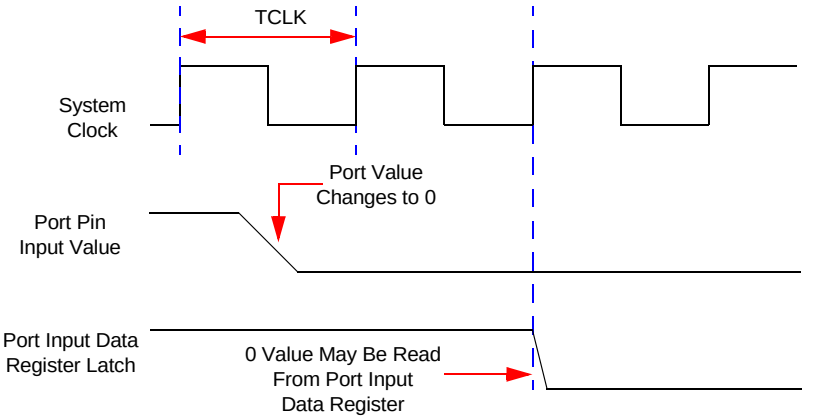


**Figure 93. Port Input Sample Timing**

**Table 107. GPIO Port Input Timing**

| | | Delay (ns) | |
|---|---|---|---|
| **Parameter** | **Abbreviation** | **Minimum** | **Maximum** |
| $T_{S\_PORT}$ | Port Input Transition to XIN Rise Setup Time (Not pictured) | 5 | – |
| $T_{H\_PORT}$ | XIN Rise to Port Input Transition Hold Time (Not pictured) | 5 | – |
| $T_{SMR}$ | GPIO Port Pin Pulse Width to Insure Stop Mode Recovery (for GPIO Port Pins enabled as SMR sources) | 1µs | |