



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.620", 15.75mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f3201pm020sc



Table 67.	I2C Data Register (I2CDATA)	118
Table 68.	I2C Status Register (I2CSTAT)	118
Table 69.	I2C Control Register (I2CCTL)	119
Table 70.	I2C Baud Rate High Byte Register (I2CBRH)	121
Table 71.	I2C Baud Rate Low Byte Register (I2CBRL)	121
Table 72.	DMAx Control Register (DMAxCTL)	124
Table 73.	DMAx I/O Address Register (DMAxIO)	126
Table 74.	DMAx Address High Nibble Register (DMAxH)	126
Table 75.	DMAx End Address Low Byte Register (DMAxEND)	128
Table 76.	DMAx Start/Current Address Low Byte Register (DMAxSTART)	128
Table 77.	DMA_ADC Register File Address Example	129
Table 78.	DMA_ADC Address Register (DMAA_ADDR)	129
Table 79.	DMA_ADC Control Register (DMAACTL)	130
Table 80.	DMA_ADC Status Register (DMAA_STAT)	131
Table 81.	ADC Control Register (ADCCTL)	135
Table 82.	ADC Data High Byte Register (ADCD_H)	137
Table 83.	ADC Data Low Bits Register (ADCD_L)	137
Table 84.	Z8F640x family Flash Memory Configurations	138
Table 85.	Flash Code Protection Using the Option Bits	142
Table 86.	Flash Control Register (FCTL)	144
Table 87.	Flash Status Register (FSTAT)	145
Table 88.	Flash Page Select Register (FPS)	146
Table 89.	Flash Frequency High Byte Register (FFREQH)	147
Table 90.	Flash Frequency Low Byte Register (FFREQL)	147
Table 91.	Option Bits At Program Memory Address 0000H	149
Table 92.	Options Bits at Program Memory Address 0001H	150
Table 93.	OCD Baud-Rate Limits	154
Table 94.	On-Chip Debugger Commands	156
Table 95.	OCD Control Register (OCDCTL)	161
Table 96.	OCD Status Register (OCDSTAT)	162
Table 97.	OCD Watchpoint Control/Address (WPTCTL)	163
Table 98.	OCD Watchpoint Address (WPTADDR)	164
Table 99.	OCD Watchpoint Data (WPTDATA)	164
Table 100.	Recommended Crystal Oscillator Specifications (20MHz Operation)	166



Table 101. Absolute Maximum Ratings	167
Table 102. DC Characteristics	169
Table 103. AC Characteristics	172
Table 104. Power-On Reset and Voltage Brown-Out Electrical Characteristics and Timing	173
Table 105. Flash Memory Electrical Characteristics and Timing . . .	173
Table 106. Watch-Dog Timer Electrical Characteristics and Timing	174
Table 107. Analog-to-Digital Converter Electrical Characteristics and Timing	174
Table 108. GPIO Port Input Timing	176
Table 109. GPIO Port Output Timing	177
Table 110. On-Chip Debugger Timing	178
Table 111. SPI Master Mode Timing	179
Table 112. SPI Slave Mode Timing	180
Table 113. I2C Timing	181
Table 114. Assembly Language Syntax Example 1	183
Table 115. Assembly Language Syntax Example 2	183
Table 116. Notational Shorthand	184
Table 117. Additional Symbols	185
Table 118. Condition Codes	186
Table 119. Arithmetic Instructions	187
Table 120. Bit Manipulation Instructions	188
Table 121. Block Transfer Instructions	188
Table 122. CPU Control Instructions	189
Table 123. Load Instructions	189
Table 124. Logical Instructions	190
Table 125. Program Control Instructions	190
Table 126. Rotate and Shift Instructions	191
Table 127. eZ8 CPU Instruction Summary	191
Table 128. Opcode Map Abbreviations	203
Table 129. Ordering Information	211

Block Diagram

Figure 55 illustrates the block diagram of the architecture of the Z8 Encore!™.

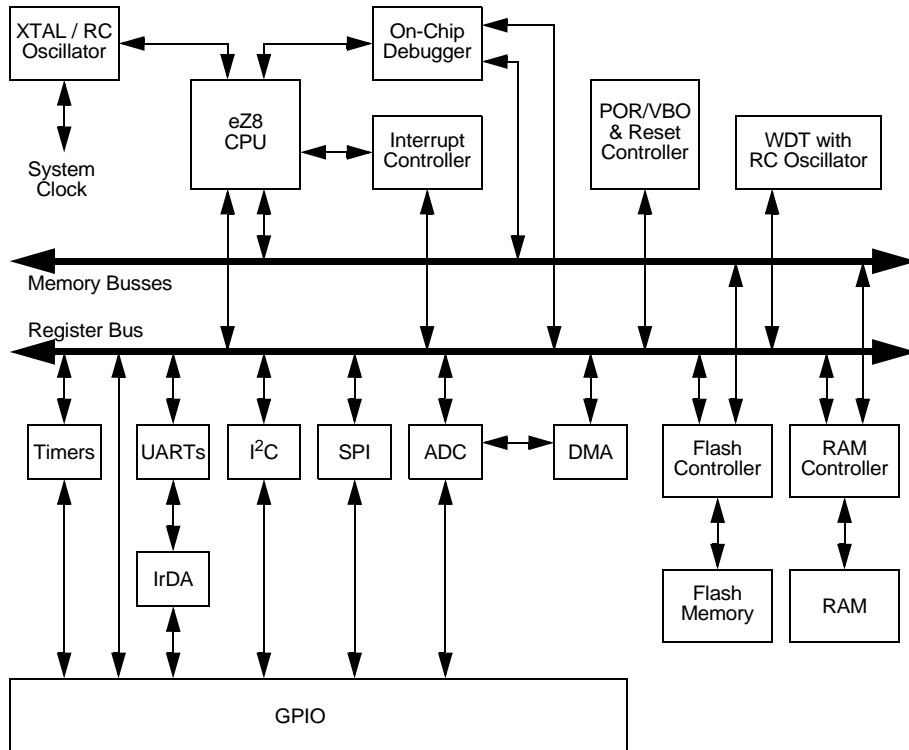


Figure 55. Z8 Encore!® Block Diagram

CPU and Peripheral Overview

eZ8 CPU Features

The eZ8, ZiLOG's latest 8-bit Central Processing Unit (CPU), meets the continuing demand for faster and more code-efficient microcontrollers. The eZ8 CPU executes a superset of the original Z8 instruction set. The eZ8 CPU features include:

- Direct register-to-register architecture allows each register to function as an accumulator, improving execution time and decreasing the required program memory



Signal Descriptions

Table 2 describes the Z8F640x family signals. Refer to the section **Pin Configurations on page 7** to determine the signals available for the specific package styles.

Table 2. Signal Descriptions

Signal Mnemonic	I/O	Description
General-Purpose I/O Ports A-H		
PA[7:0]	I/O	Port A[7:0]. These pins are used for general-purpose I/O.
PB[7:0]	I/O	Port B[7:0]. These pins are used for general-purpose I/O.
PC[7:0]	I/O	Port C[7:0]. These pins are used for general-purpose I/O.
PD[7:0]	I/O	Port D[7:0]. These pins are used for general-purpose I/O.
PE[7:0]	I/O	Port E[7:0]. These pins are used for general-purpose I/O.
PF[7:0]	I/O	Port F[7:0]. These pins are used for general-purpose I/O.
PG[7:0]	I/O	Port G[7:0]. These pins are used for general-purpose I/O.
PH[3:0]	I/O	Port H[3:0]. These pins are used for general-purpose I/O.
I²C Controller		
SCL	O	Serial Clock. This is the output clock for the I ² C. This pin is multiplexed with a general-purpose I/O pin. When the general-purpose I/O pin is configured for alternate function to enable the SCL function, this pin is open-drain.
SDA	I/O	Serial Data. This open-drain pin is used to transfer data between the I ² C and a slave. This pin is multiplexed with a general-purpose I/O pin. When the general-purpose I/O pin is configured for alternate function to enable the SDA function, this pin is open-drain.
SPI Controller		
\overline{SS}	I/O	Slave Select. This signal can be an output or an input. If the Z8 Encore! is the SPI master, this pin may be configured as the Slave Select output. If the Z8 Encore! is the SPI slave, this pin is the input slave select. It is multiplexed with a general-purpose I/O pin.
SCK	I/O	SPI Serial Clock. The SPI master supplies this pin. If the Z8 Encore! is the SPI master, this pin is an output. If the Z8 Encore! is the SPI slave, this pin is an input. It is multiplexed with a general-purpose I/O pin.
MOSI	I/O	Master Out Slave In. This signal is the data output from the SPI master device and the data input to the SPI slave device. It is multiplexed with a general-purpose I/O pin.
MISO	I/O	Master In Slave Out. This pin is the data input to the SPI master device and the data output from the SPI slave device. It is multiplexed with a general-purpose I/O pin.



Table 3. Pin Characteristics of the Z8F640x family

Symbol Mnemonic	Direction	Reset Direction	Active Low or Active High	Tri-State Output	Internal Pull-up or Pull-down	Schmitt Trigger Input	Open Drain Output
PF[7:0]	I/O	I	N/A	Yes	No	Yes	Yes, Programmable
PG[7:0]	I/O	I	N/A	Yes	No	Yes	Yes, Programmable
PH[3:0]	I/O	I	N/A	Yes	No	Yes	Yes, Programmable
$\overline{\text{RESET}}$	I	I	Low	N/A	Pull-up	Yes	N/A
VDD	N/A	N/A	N/A	N/A	No	No	N/A
XIN	I	I	N/A	N/A	No	No	N/A
XOUT	O	O	N/A	Yes, in Stop mode	No	No	No

x represents integer 0, 1,... to indicate multiple pins with symbol mnemonics that differ only by the integer



Address Space

Overview

The eZ8 CPU can access three distinct address spaces:

- The Register File contains addresses for the general-purpose registers and the eZ8 CPU, peripheral, and general-purpose I/O port control registers.
- The Program Memory contains addresses for all memory locations having executable code and/or data.
- The Data Memory contains addresses for all memory locations that hold data only.

These three address spaces are covered briefly in the following subsections. For more detailed information regarding the eZ8 CPU and its address space, refer to the *eZ8 CPU User Manual* available for download at www.zilog.com.

Register File

The Register File address space in the Z8 Encore!® is 4KB (4096 bytes). The Register File is composed of two sections—control registers and general-purpose registers. When instructions are executed, registers are read from when defined as sources and written to when defined as destinations. The architecture of the eZ8 CPU allows all general-purpose registers to function as accumulators, address pointers, index registers, stack areas, or scratch pad memory.

The upper 256 bytes of the 4KB Register File address space are reserved for control of the eZ8 CPU, the on-chip peripherals, and the I/O ports. These registers are located at addresses from F00H to FFFH. Some of the addresses within the 256-byte control register section are reserved (unavailable). Reading from an reserved Register File addresses returns an undefined value. Writing to reserved Register File addresses is not recommended and can produce unpredictable results.

The on-chip RAM always begins at address 000H in the Register File address space. The Z8F640x family products contain 2KB to 4KB of on-chip RAM depending upon the device. Reading from Register File addresses outside the available RAM addresses (and not within in the control register address space) returns an undefined value. Writing to these Register File addresses produces no effect. Refer to the **Part Selection Guide** section of the **Introduction** chapter to determine the amount of RAM available for the specific Z8F640x family device.

Port A-H Data Direction Sub-Registers

The Port A-H Data Direction sub-register is accessed through the Port A-H Control register by writing 01H to the Port A-H Address register (Table 15).

Table 15. Port A-H Data Direction Sub-Registers

BITS	7	6	5	4	3	2	1	0
FIELD	DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0
RESET	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	If 01H in Port A-H Address Register, accessible via Port A-H Control Register							

DD[7:0]—Data Direction

These bits control the direction of the associated port pin. Port Alternate Function operation overrides the Data Direction register setting.

0 = Output. Data in the Port A-H Output Data register is driven onto the port pin.

1 = Input. The port pin is sampled and the value written into the Port A-H Input Data Register. The output driver is tri-stated.

Port A-H Alternate Function Sub-Registers

The Port A-H Alternate Function sub-register (Table 16) is accessed through the Port A-H Control register by writing 02H to the Port A-H Address register. The Port A-H Alternate Function sub-registers select the alternate functions for the selected pins. Refer to the **GPIO Alternate Functions** section to determine the alternate function associated with each port pin.



Caution: Do not enable alternate function for GPIO port pins which do not have an associated alternate function. Failure to follow this guideline may result in unpredictable operation.

Table 16. Port A-H Alternate Function Sub-Registers

BITS	7	6	5	4	3	2	1	0
FIELD	AF7	AF6	AF5	AF4	AF3	AF2	AF1	AF0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	If 02H in Port A-H Address Register, accessible via Port A-H Control Register							

set to 2-byte transfers, the temporary holding register for the Timer Reload High Byte is not bypassed.

Table 40. Timer 0-3 Reload High Byte Register (TxRH)

BITS	7	6	5	4	3	2	1	0
FIELD	TRH							
RESET	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	F02H, F0AH, F12H, F1AH							

Table 41. Timer 0-3 Reload Low Byte Register (TxRL)

BITS	7	6	5	4	3	2	1	0
FIELD	TRL							
RESET	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	F03H, F0BH, F13H, F1BH							

TRH and TRL—Timer Reload Register High and Low

These two bytes form the 16-bit Reload value, {TRH[7:0], TRL[7:0]}. This value is used to set the maximum count value which initiates a timer reload to 0001H. In Compare mode, these two byte form the 16-bit Compare value.

UARTx Receive Data Register

Data bytes received through the RXD_x pin are stored in the UART_x Receive Data register (Table 51). The Read-only UART_x Receive Data register shares a Register File address with the Write-only UART_x Transmit Data register.

Table 51. UARTx Receive Data Register (UxRXD)

BITS	7	6	5	4	3	2	1	0
FIELD	RXD							
RESET	X	X	X	X	X	X	X	X
R/W	R	R	R	R	R	R	R	R
ADDR	F40H and F48H							

RXD—Receive Data
UART receiver data byte from the RXD_x pin

UARTx Status 0 and Status 1 Registers

The UART_x Status 0 and Status 1 registers (Table 52 and 53) identify the current UART operating configuration and status.

Table 52. UARTx Status 0 Register (UxSTAT0)

BITS	7	6	5	4	3	2	1	0
FIELD	RDA	PE	OE	FE	BRKD	TDRE	TXE	CTS
RESET	0	0	0	0	0	1	1	X
R/W	R	R	R	R	R	R	R	R
ADDR	F41H and F49H							

RDA—Receive Data Available
This bit indicates that the UART Receive Data register has received data. Reading the UART Receive Data register clears this bit.
0 = The UART Receive Data register is empty.
1 = There is a byte in the UART Receive Data register.

PE—Parity Error
This bit indicates that a parity error has occurred. Reading the UART Receive Data register clears this bit.

The Master and Slave are each capable of exchanging a byte of data during a sequence of eight clock cycles. In both Master and Slave SPI devices, data is shifted on one edge of the SCK and is sampled on the opposite edge where data is stable. Edge polarity is determined by the SPI phase and polarity control.

Slave Select

The active Low Slave Select (\overline{SS}) input signal is used to select a Slave SPI device. \overline{SS} must be Low prior to all data communication to and from the Slave device. \overline{SS} must stay Low for the full duration of each character transferred. The \overline{SS} signal may stay Low during the transfer of multiple characters or may deassert between each character.

When the SPI on the Z8F640x family device is configured as the only Master in an SPI system, the \overline{SS} pin can be set as either an input or an output. For communication between the Z8F640x family device SPI Master and external Slave devices, the \overline{SS} signal, as an output, can assert the \overline{SS} input pin on one of the Slave devices. Other GPIO output pins can also be employed to select external SPI Slave devices.

When the SPI on the Z8F640x family device is configured as one Master in a multi-master SPI system, the \overline{SS} pin on the should be set as an input. The \overline{SS} input signal on the Master must be High. If the \overline{SS} signal goes Low (indicating another Master is driving the SPI bus), a Mode Fault error flag is set in the SPI Status register.

SPI Clock Phase and Polarity Control

The SPI supports four combinations of serial clock phase and polarity using two bits in the SPI Control register. The clock polarity bit, CLKPOL, selects an active high or active low clock and has no effect on the transfer format. Table 59 lists the SPI Clock Phase and Polarity Operation parameters. The clock phase bit, PHASE, selects one of two fundamentally different transfer formats. For proper data transmission, the clock phase and polarity must be identical for the SPI Master and the SPI Slave. The Master always places data on the MOSI line a half-cycle before the clock edge (SCK signal), in order for the Slave to latch the data.

Table 59. SPI Clock Phase (PHASE) and Clock Polarity (CLKPOL) Operation

PHASE	CLKPOL	SCK Transmit Edge	SCK Receive Edge	SCK Idle State
0	0	Falling	Rising	Low
0	1	Rising	Falling	High
1	0	Rising	Falling	Low
1	1	Falling	Rising	High

SPI Mode Register

The SPI Mode register configures the character bit width and the direction and value of the \overline{SS} pin.

Table 63. SPI Mode Register (SPIMODE)

BITS	7	6	5	4	3	2	1	0
FIELD	Reserved			NUMBITS[2:0]			SSIO	SSV
RESET	0			0	0	0	0	0
R/W	R			R/W	R/W	R/W	R/W	R/W
ADDR	F63H							

Reserved

These bits are reserved and must be 0.

NUMBITS[2:0]—Number of Data Bits Per Character to Transfer

This field contains the number of bits to shift for each character transfer. Refer to the SPI Data Register description for information on valid bit positions when the character length is less than 8-bits.

000 = 8 bits

001 = 1 bit

010 = 2 bits

011 = 3 bits

100 = 4 bits

101 = 5 bits

110 = 6 bits

111 = 7 bits.

SSIO—Slave Select I/O

0 = \overline{SS} pin configured as an input.

1 = \overline{SS} pin configured as an output (Master mode only).

SSV—Slave Select Value

If SSIO = 1 and SPI configured as a Master:

0 = \overline{SS} pin driven Low (0).

1 = \overline{SS} pin driven High (1).

This bit has no effect if SSIO = 0 or SPI configured as a Slave.

ADC Data High Byte Register

The ADC Data High Byte register contains the upper eight bits of the 10-bit ADC output. During a conversion, this value is invalid. Access to the ADC Data High Byte register is read-only. The full 10-bit ADC result is given by {ADCD_H[7:0], ADCD_L[7:6]}.

Table 81. ADC Data High Byte Register (ADCD_H)

BITS	7	6	5	4	3	2	1	0
FIELD	ADCD_H							
RESET	X							
R/W	R							
ADDR	F72H							

ADCD_H—ADC Data High Byte

This byte contains the upper eight bits of the 10-bit ADC output. These bits are not valid during a conversion. These bits are undefined after a Reset.

ADC Data Low Bits Register

The ADC Data Low Bits register contains the lower two bits of the conversion value. During a conversion this value is invalid. Access to the ADC Data Low Bits register is read-only. The full 10-bit ADC result is given by {ADCD_H[7:0], ADCD_L[7:6]}.

Table 82. ADC Data Low Bits Register (ADCD_L)

BITS	7	6	5	4	3	2	1	0
FIELD	ADCD_L		Reserved					
RESET	X		X					
R/W	R		R					
ADDR	F73H							

ADCD_L—ADC Data Low Bits

These are the least significant two bits of the 10-bit ADC output. During a conversion, this value is invalid. These bits are undefined after a Reset.

Reserved

These bits are reserved and are always undefined.



Flash Memory

Overview

The Z8F640x family features up to 64KB (65,536 bytes) of non-volatile Flash memory with read/write/erase capability. The Flash Memory can be programmed and erased in-circuit by either user code or through the On-Chip Debugger.

The Flash memory array is arranged in pages with 512 bytes per page. The 512-byte page is the minimum Flash block size that can be erased. Each page is divided into 8 rows of 64 bytes. The Flash memory also contains a High Sector that can be enabled for writes and erase separately from the rest of the Flash array. The first 2 bytes of the Flash Program memory are used as Option Bits. Refer to the **Option Bits** chapter for more information on their operation.

Table 83 describes the Flash memory configuration for each device in the Z8F640x family. Figure 84 illustrates the Flash memory arrangement.

Table 83. Z8F640x family Flash Memory Configurations

Part Number	Flash Size KB (Bytes)	Flash Pages	Program Memory Addresses	Flash High Sector Size KB (Bytes)	High Sector Addresses
Z8F160x	16 (16,384)	32	0000H - 3FFFH	1 (1024)	3C00H - 3FFFH
Z8F240x	24 (24,576)	48	0000H - 5FFFH	2 (2048)	5800H - 5FFFH
Z8F320x	32 (32,768)	64	0000H - 7FFFH	2 (2048)	7800H - 7FFFH
Z8F480x	48 (49,152)	96	0000H - BFFFH	4 (4096)	B000H - BFFFH
Z8F640x	64 (65,536)	128	0000H - FFFFH	8 (8192)	E000H - FFFFH



Program Memory Address 0000H

Table 90. Option Bits At Program Memory Address 0000H

BITS	7	6	5	4	3	2	1	0
FIELD	WDT_RES	WDT_AO	Reserved			RP	FHSWP	FWP
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	Program Memory 0000H							

Note: U = Unchanged by Reset. R/W = Read/Write.

WDT_RES—Watch-Dog Timer Reset

0 = Watch-Dog Timer time-out generates an interrupt request. Interrupts must be globally enabled for the eZ8 CPU to acknowledge the interrupt request.

1 = Watch-Dog Timer time-out causes a Short Reset. This setting is the default for unprogrammed (erased) Flash.

WDT_AO—Watch-Dog Timer Always On

0 = Watch-Dog Timer is automatically enabled upon application of system power. Watch-Dog Timer can not be disabled.

1 = Watch-Dog Timer is enabled upon execution of the WDT instruction. Once enabled, the Watch-Dog Timer can only be disabled by a Reset or Stop Mode Recovery. This setting is the default for unprogrammed (erased) Flash.

Reserved

These Option Bits are reserved for future use and must always be set to 1. This setting is the default for unprogrammed (erased) Flash.

RP—Read Protect

0 = User program code is inaccessible. Limited control features are available through the On-Chip Debugger.

1 = User program code is accessible. All On-Chip Debugger commands are enabled. This setting is the default for unprogrammed (erased) Flash.

RPEN—Read Protect Option Bit Enabled

0 = The Read Protect Option Bit is disabled (1).

0 = The Read Protect Option Bit is enabled (0), disabling many OCD commands.

Reserved

These bits are always 0.

OCD Watchpoint Control Register

The OCD Watchpoint Control register is used to configure the debug Watchpoint.

Table 96. OCD Watchpoint Control/Address (WPTCTL)

BITS	7	6	5	4	3	2	1	0
FIELD	WPW	WPR	WPDM	Reserved	WPTADDR[11:8]			
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

WPW—Watchpoint Break on Write

This bit cannot be set if the Read Protect Option Bit is enabled.

0 = Watchpoint Break on Register File write is disabled.

1 = Watchpoint Break on Register File write is enabled.

WPR—Watchpoint Break on Read

This bit cannot be set if the Read Protect Option Bit is enabled.

0 = Watchpoint Break on Register File read is disabled.

1 = Watchpoint Break on Register File write is enabled.

WPDM—Watchpoint Data Match

If this bit is set, then the Watchpoint only generates a Debug Break if the data being read or written matches the specified Watchpoint data. Either the WPR and/or WPW bits must also be set for this bit to affect operation. This bit cannot be set if the Read Protect Option Bit is enabled.

0 = Watchpoint Break on read and/or write does not require a data match.

1 = Watchpoint Break on read and/or write requires a data match.

Reserved

This bit is reserved and must be 0.

RADDR[11:8]—Register address

These bits specify the upper 4 bits of the Register File address to match when generating a Watchpoint Debug Break. The full 12-bit Register File address is given by {WPTCTL3:0, WPTADDR[7:0]}.

Figure 92 illustrates the typical current consumption in Halt mode while operating at 25°C, 3.3V, versus the system clock frequency.

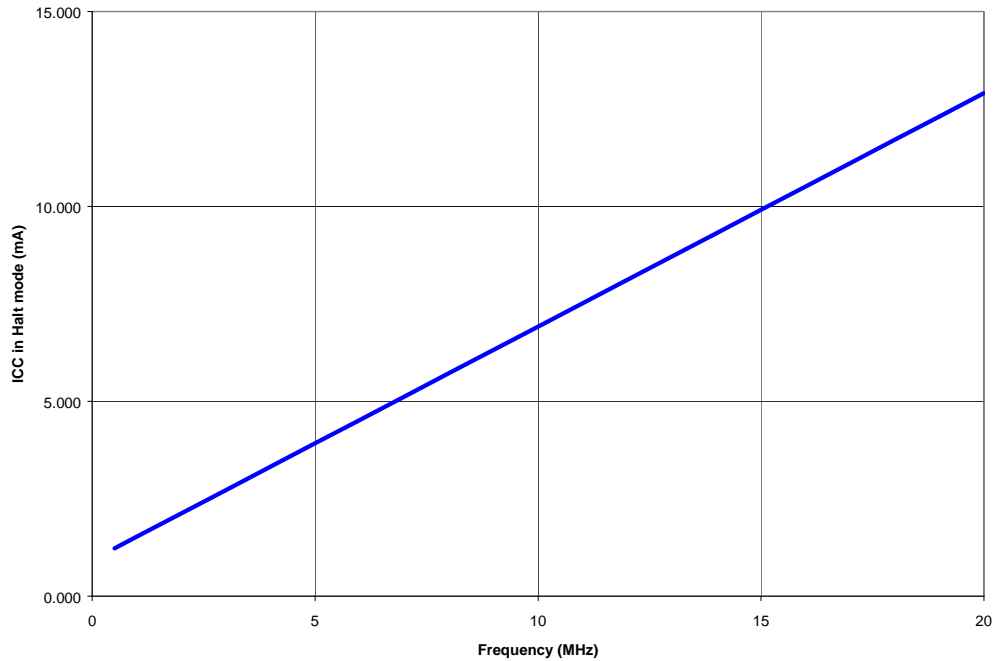


Figure 92. Nominal Halt Mode ICC Versus System Clock Frequency

Table 116. Additional Symbols

Symbol	Definition
dst	Destination Operand
src	Source Operand
@	Indirect Address Prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flags Register
RP	Register Pointer
#	Immediate Operand Prefix
B	Binary Number Suffix
%	Hexadecimal Number Prefix
H	Hexadecimal Number Suffix

Assignment of a value is indicated by an arrow. For example,

$$\text{dst} \leftarrow \text{dst} + \text{src}$$

indicates the source data is added to the destination data and the result is stored in the destination location.



Table 125. Rotate and Shift Instructions

Mnemonic	Operands	Instruction
BSWAP	dst	Bit Swap
RL	dst	Rotate Left
RLC	dst	Rotate Left through Carry
RR	dst	Rotate Right
RRC	dst	Rotate Right through Carry
SRA	dst	Shift Right Arithmetic
SRL	dst	Shift Right Logical
SWAP	dst	Swap Nibbles

eZ8 CPU Instruction Summary

Table 126 summarizes the eZ8 CPU instructions. The table identifies the addressing modes employed by the instruction, the effect upon the Flags register, the number of CPU clock cycles required for the instruction fetch, and the number of CPU clock cycles required for the instruction execution.

Table 126. eZ8 CPU Instruction Summary

Assembly Mnemonic	Symbolic Operation	Address Mode		Opcode(s) (Hex)	Flags						Fetch Cycles	Instr. Cycles
		dst	src		C	Z	S	V	D	H		
ADC dst, src	dst ← dst + src + C	r	r	12	*	*	*	*	0	*	2	3
		r	Ir	13							2	4
		R	R	14							3	3
		R	IR	15							3	4
		R	IM	16							3	3
		IR	IM	17							3	4
ADCX dst, src	dst ← dst + src + C	ER	ER	18	*	*	*	*	0	*	4	3
		ER	IM	19							4	3
Flags Notation:	* = Value is a function of the result of the operation. - = Unaffected X = Undefined				0 = Reset to 0 1 = Set to 1							



- cc 184
- CCF 189
- characteristics, electrical 167
- clear 189
- clock phase (SPI) 102
- CLR 189
- COM 190
- compare 71
- compare - extended addressing 187
- compare mode 71
- compare with carry 187
- compare with carry - extended addressing 187
- complement 190
- complement carry flag 188, 189
- condition code 184
- continuous assertion interrupt sources 47
- continuous conversion (ADC) 134
- continuous mode 70
- control register definition, UART 86
- control register, I2C 119
- counter modes 70
- CP 187
- CPC 187
- CPCX 187
- CPU and peripheral overview 3
- CPU control instructions 189
- CPX 187
- customer feedback form 216
- customer information 216
- customer service 213

D

- DA 184, 187
- data memory 19
- data register, I2C 118
- DC characteristics 169
- debugger, on-chip 151
- DEC 187
- decimal adjust 187
- decrement 187
- decrement and jump non-zero 190
- decrement word 187
- DECW 187

- destination operand 185
- device, port availability 33
- DI 189
- direct address 184
- direct memory access controller 122
- disable interrupts 189
- DJNZ 190
- DMA
 - address high nibble register 126
 - configuring for DMA_ADC data transfer 124
 - configuring DMA0-1 data transfer 123
 - control of ADC 135
 - control register 124
 - control register definitions 124
 - controller 5
 - DMA_ADC address register 128
 - DMA_ADC control register 130
 - DMA_ADC operation 123
 - end address low byte register 128
 - I/O address register 125
 - operation 122
 - start/current address low byte register 127
 - status register 131
- DMAA_STAT register 131
- DMACTL register 130
- DMAxCTL register 124
- DMAxEND register 128
- DMAxH register 126
- DMAxI/O address (DMAxIO) 126
- DMAxIO register 126
- DMAxSTART register 128
- document number description 215
- dst 185

E

- EI 189
- electrical characteristics 167
 - ADC 174
 - flash memory and timing 173
 - GPIO input data sample timing 176
 - watch-dog timer 174
- enable interrupt 189
- ER 184



- extended addressing register 184
- external pin reset 29
- eZ8 CPU features 3
- eZ8 CPU instruction classes 187
- eZ8 CPU instruction notation 183
- eZ8 CPU instruction set 182
- eZ8 CPU instruction summary 191

F

- FCTL register 144
- features, Z8 Encore!® 1
- first opcode map 204
- FLAGS 185
- flags register 185
- flash
 - controller 4
 - option bit address space 148
 - option bit configuration - reset 148
 - program memory address 0000H 149
 - program memory address 0001H 150
- flash memory 138
 - arrangement 139
 - byte programming 142
 - code protection 141
 - configurations 138
 - control register definitions 144
 - controller bypass 143
 - electrical characteristics and timing 173
 - flash control register 144
 - flash option bits 142
 - flash status register 145
 - flow chart 140
 - frequency high and low byte registers 147
 - mass erase 143
 - operation 139
 - operation timing 141
 - page erase 143
 - page select register 146
- FPS register 146
- FSTAT register 145

G

- gated mode 71
- general-purpose I/O 33
- GPIO 4, 33
 - alternate functions 34
 - architecture 34
 - control register definitions 36
 - input data sample timing 176
 - interrupts 36
 - port A-H address registers 37
 - port A-H alternate function sub-registers 39
 - port A-H control registers 38
 - port A-H data direction sub-registers 39
 - port A-H high drive enable sub-registers 41
 - port A-H input data registers 42
 - port A-H output control sub-registers 40
 - port A-H output data registers 43
 - port A-H stop mode recovery sub-registers 41
 - port availability by device 33
 - port input timing 176
 - port output timing 177

H

- H 185
- HALT 189
- HALT mode 31, 189
- hexadecimal number prefix/suffix 185

I

- I²C 4
 - 10-bit address read transaction 116
 - 10-bit address transaction 114
 - 10-bit addressed slave data transfer format 114
 - 10-bit receive data format 116
 - 7-bit address transaction 112
 - 7-bit address, reading a transaction 115
 - 7-bit addressed slave data transfer format 113
 - 7-bit receive data transfer format 115
 - baud high and low byte registers 121
 - C status register 118
 - control register definitions 118