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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	31
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f6401an020sc



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Braces

The curly braces, { }, indicate a single register or bus created by concatenating some combination of smaller registers, buses, or individual bits.

- Example: the 12-bit register address {0H, RP[7:4], R1[3:0]} is composed of a 4-bit hexadecimal value (0H) and two 4-bit register values taken from the Register Pointer (RP) and Working Register R1. 0H is the most significant nibble (4-bit value) of the 12-bit register, and R1[3:0] is the least significant nibble of the 12-bit register.

Parentheses

The parentheses, (), indicate an indirect register address lookup.

- Example: (R1) is the memory location referenced by the address contained in the Working Register R1.

Parentheses/Bracket Combinations

The parentheses, (), indicate an indirect register address lookup and the square brackets, [], indicate a register or bus.

- *Example:* assume PC[15:0] contains the value 1234h. (PC[15:0]) then refers to the contents of the memory location at address 1234h.

Use of the Words *Set*, *Reset* and *Clear*

The word *set* implies that a register bit or a condition contains a logical 1. The words *reset* or *clear* imply that a register bit or a condition contains a logical 0. When either of these terms is followed by a number, the word *logical* may not be included; however, it is implied.

Notation for Bits and Similar Registers

A field of bits within a register is designated as: Register[n:n].

- Example: ADDR[15:0] refers to bits 15 through bit 0 of the Address.

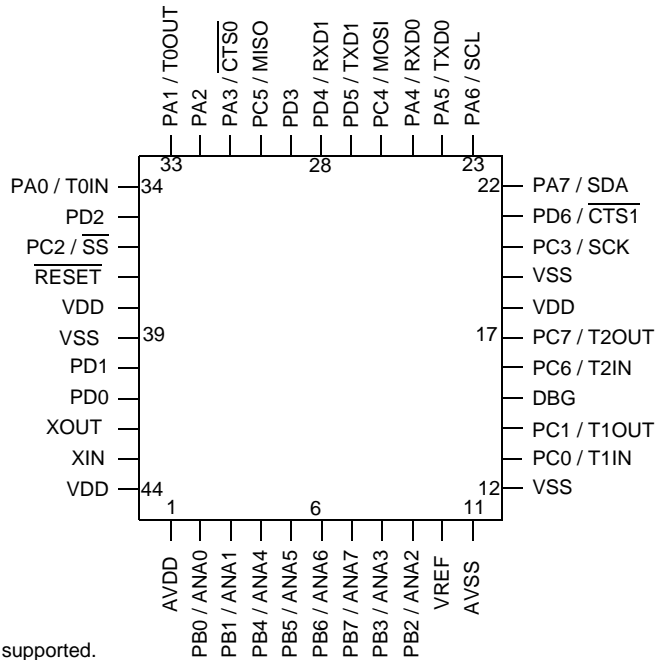
Use of the Terms *LSB*, *MSB*, *lsb*, and *msb*

In this document, the terms *LSB* and *MSB*, when appearing in upper case, mean *least significant byte* and *most significant byte*, respectively. The lowercase forms, *lsb* and *msb*, mean *least significant bit* and *most significant bit*, respectively.

Use of Initial Uppercase Letters

Initial uppercase letters designate settings, modes, and conditions in general text.

- Example 1: Stop mode.
- Example 2: The receiver forces the SCL line to Low.
- The Master can generate a Stop condition to abort the transfer.



Note: Timer 3 is not supported.

Figure 58. Z8Fxx01 in 44-Pin Low-Profile Quad Flat Package (LQFP)

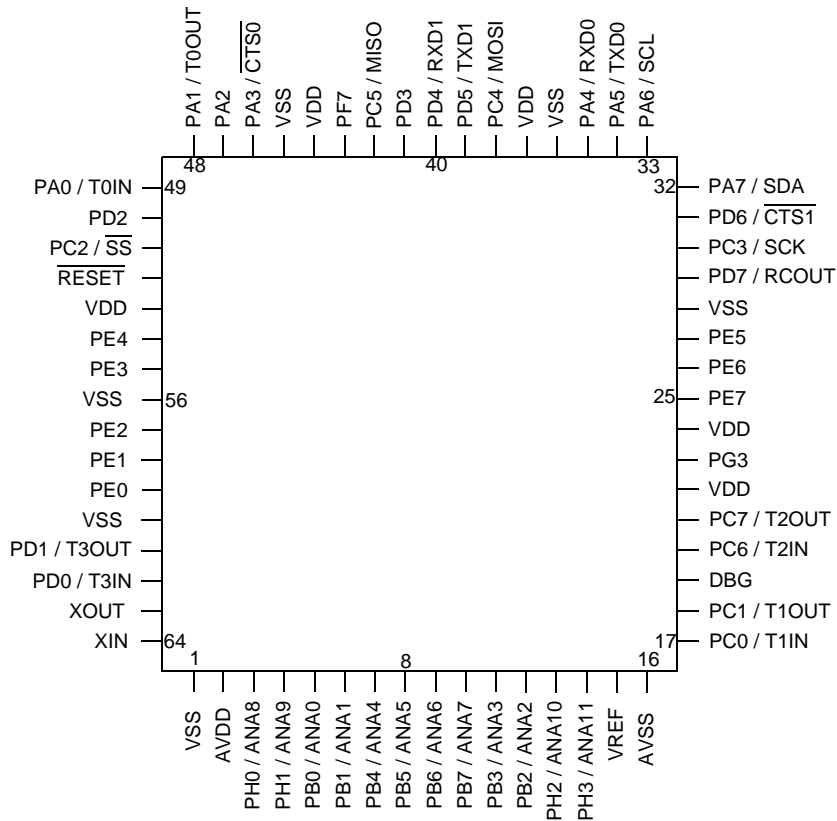


Figure 59. Z8Fxx02 in 64-Pin Low-Profile Quad Flat Package (LQFP)

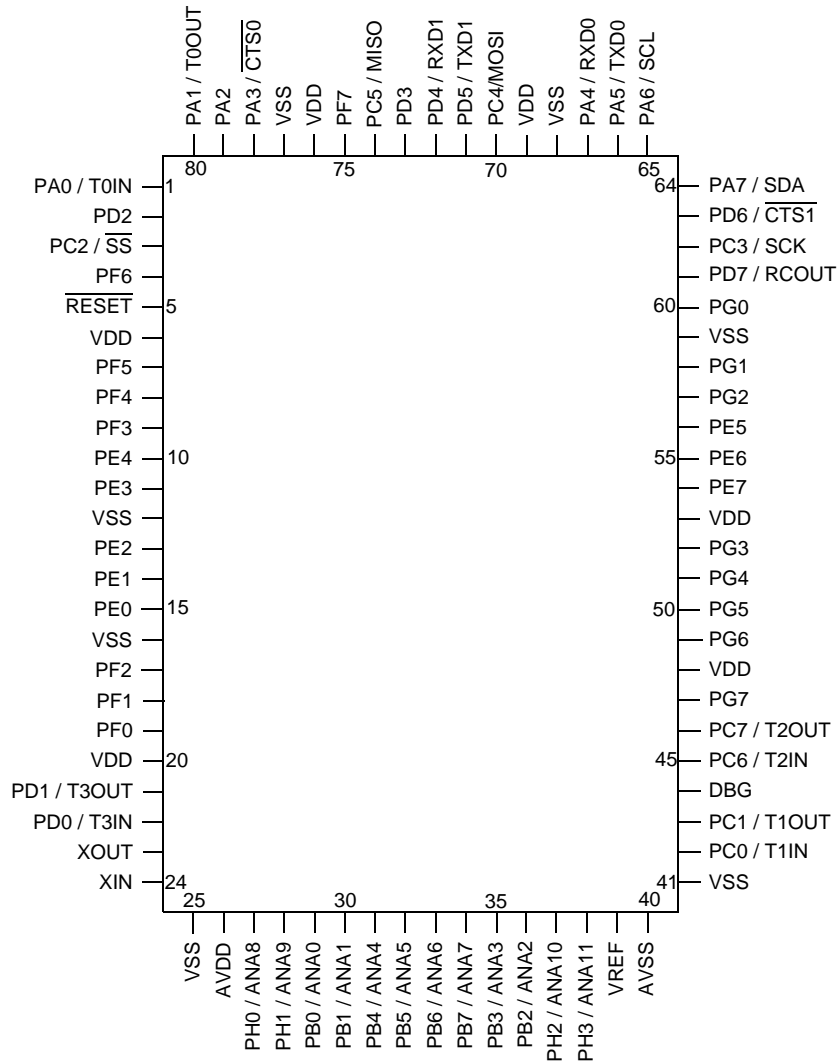


Figure 61. Z8Fxx03 in 80-Pin Quad Flat Package (QFP)



Table 6. Register File Address Map (Continued)

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page #
Timer 3 (not available in 40- and 44- Pin Packages)				
F18	Timer 3 High Byte	T3H	00	66
F19	Timer 3 Low Byte	T3L	01	66
F1A	Timer 3 Reload High Byte	T3RH	FF	67
F1B	Timer 3 Reload Low Byte	T3RL	FF	67
F1C	Timer 3 PWM High Byte	T3PWMH	00	69
F1D	Timer 3 PWM Low Byte	T3PWML	00	69
F1E	Reserved	—	XX	
F1F	Timer 3 Control	T3CTL	00	70
F20-F3F	Reserved	—	XX	
UART 0				
F40	UART0 Transmit Data	U0TXD	XX	86
	UART0 Receive Data	U0RXD	XX	87
F41	UART0 Status 0	U0STAT0	0000011Xb	87
F42	UART0 Control 0	U0CTL0	00	89
F43	UART0 Control 1	U0CTL1	00	89
F44	UART0 Status 1	U0STAT1	00	87
F45	Reserved	—	XX	
F46	UART0 Baud Rate High Byte	U0BRH	FF	91
F47	UART0 Baud Rate Low Byte	U0BRL	FF	91
UART 1				
F48	UART1 Transmit Data	U1TXD	XX	86
	UART1 Receive Data	U1RXD	XX	87
F49	UART1 Status 0	U1STAT0	0000011Xb	87
F4A	UART1 Control 0	U1CTL0	00	89
F4B	UART1 Control 1	U1CTL1	00	89
F4C	UART1 Status 1	U1STAT1	00	87
F4D	Reserved	—	XX	
F4E	UART1 Baud Rate High Byte	U1BRH	FF	91
F4F	UART1 Baud Rate Low Byte	U1BRL	FF	91
I²C				
F50	I ² C Data	I2CDATA	00	118
F51	I ² C Status	I2CSTAT	80	118
F52	I ² C Control	I2CCTL	00	119
F53	I ² C Baud Rate High Byte	I2CBRH	FF	121
F54	I ² C Baud Rate Low Byte	I2CBRL	FF	121
F55-F5F	Reserved	—	XX	
Serial Peripheral Interface (SPI)				
F60	SPI Data	SPIDATA	XX	106
F61	SPI Control	SPICTL	00	107
XX=Undefined				

AF[7:0]—Port Alternate Function enabled

0 = The port pin is in normal mode and the DDx bit in the Port A-H Data Direction sub-register determines the direction of the pin.

1 = The alternate function is selected. Port pin operation is controlled by the alternate function.

Port A-H Output Control Sub-Registers

The Port A-H Output Control sub-register (Table 17) is accessed through the Port A-H Control register by writing 03H to the Port A-H Address register. Setting the bits in the Port A-H Output Control sub-registers to 1 configures the specified port pins for open-drain operation. These sub-registers affect the pins directly and, as a result, alternate functions are also affected.

Table 17. Port A-H Output Control Sub-Registers

BITS	7	6	5	4	3	2	1	0
FIELD	POC7	POC6	POC5	POC4	POC3	POC2	POC1	POC0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	If 03H in Port A-H Address Register, accessible via Port A-H Control Register							

POC[7:0]—Port Output Control

These bits function independently of the alternate function bit and disables the drains if set to 1.

0 = The drains are enabled for any output mode.

1 = The drain of the associated pin is disabled (open-drain mode).

- Execution of a Trap instruction
- Illegal instruction trap

Interrupt Vectors and Priority

The Z8F640x family device interrupt controller supports three levels of interrupt priority. Level 3 is the highest priority, Level 2 is the second highest priority, and Level 1 is the lowest priority. If all of the interrupts were enabled with identical interrupt priority (all as Level 2 interrupts, for example), then interrupt priority would be assigned from highest to lowest as specified in Table 22. Level 3 interrupts always have higher priority than Level 2 interrupts which, in turn, always have higher priority than Level 1 interrupts. Within each interrupt priority level (Level 1, Level 2, or Level 3), priority is assigned as specified in Table 22.

Reset, Watch-Dog Timer interrupt (if enabled), and Illegal Instruction Trap always have highest (Level 3) priority.

Interrupt Assertion Types

Two types of interrupt assertion - single assertion (pulse) and continuous assertion - are used within the Z8F640x family device. The type of interrupt assertion for each interrupt source is listed in Table 22.

Single Assertion (Pulse) Interrupt Sources

Some interrupt sources assert their interrupt requests for only a single system clock period (single pulse). When the interrupt request is acknowledged by the eZ8 CPU, the corresponding bit in the Interrupt Request register is cleared until the next interrupt occurs. Writing a 0 to the corresponding bit in the Interrupt Request register likewise clears the interrupt request.

Continuous Assertion Interrupt Sources

Other interrupt sources continuously assert their interrupt requests until cleared at the source. For these continuous assertion interrupt sources, interrupt acknowledgement by the eZ8 CPU does not clear the corresponding bit in the Interrupt Request register. Writing a 0 to the corresponding bit in the Interrupt Request register only clears the interrupt for a single clock cycle. Since the source is continuously asserting the interrupt request, the interrupt request bit is set to 1 again during the next clock cycle.

The only way to clear continuous assertion interrupts is at the source of the interrupt (for example, in the UART or SPI peripherals). The source of the interrupt must be cleared first. After the interrupt is cleared at the source, the corresponding bit in the Interrupt Request register must also be cleared to 0. Both the interrupt source and the IRQ register must be cleared.

Watch-Dog Timer Control Register Definitions

Watch-Dog Timer Control Register

The Watch-Dog Timer Control (WDTCTL) register, detailed in Table 46, is a Read-Only register that indicates the source of the most recent Reset event, indicates a Stop Mode Recovery event, and indicates a Watch-Dog Timer time-out. Reading this register resets the upper four bits to 0.

Writing the 55H, AAH unlock sequence to the Watch-Dog Timer Control (WDTCTL) register address unlocks the three Watch-Dog Timer Reload Byte registers (WDTU, WDTL, and WDTL) to allow changes to the time-out period. These write operations to the WDTCTL register address produce no effect on the bits in the WDTCTL register. The locking mechanism prevents spurious writes to the Reload registers.

Table 46. Watch-Dog Timer Control Register (WDTCTL)

BITS	7	6	5	4	3	2	1	0
FIELD	POR	STOP	WDT	EXT	Reserved			
RESET	X	X	X	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R
ADDR	FF0							

POR—Power-On Reset Indicator

If this bit is set to 1, a Power-On Reset event occurred. This bit is reset to 0 if a WDT time-out or Stop Mode Recovery occurs. This bit is also reset to 0 when the register is read.

STOP—STOP Mode Recovery Indicator

If this bit is set to 1, a STOP Mode Recovery occurred. If the STOP and WDT bits are both set to 1, the STOP Mode Recovery occurred due to a WDT time-out. If the STOP bit is 1 and the WDT bit is 0, the STOP Mode Recovery was not caused by a WDT time-out. This bit is reset by a Power-On Reset or a WDT time-out that occurred while not in STOP mode. Reading this register also resets this bit.

WDT—Watch-Dog Timer Time-Out Indicator

If this bit is set to 1, a WDT time-out occurred. A Power-On Reset resets this pin. A Stop Mode Recovery from a change in an input pin also resets this bit. Reading this register resets this bit.

EXT—External Reset Indicator

If this bit is set to 1, a Reset initiated by the external RESET pin occurred. A Power-On Reset or a Stop Mode Recovery from a change in an input pin resets this bit. Reading this register resets this bit.

When the DMA is configured for two-byte word transfers, the DMAx I/O Address register must contain an even numbered address.

Table 72. DMAx I/O Address Register (DMAxIO)

BITS	7	6	5	4	3	2	1	0
FIELD	DMA_IO							
RESET	X	X	X	X	X	X	X	X
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	FB1H, FB9H							

DMA_IO—DMA on-chip peripheral control register address

This byte sets the low byte of the on-chip peripheral control register address on Register File Page FH (addresses F00H to FFFH).

DMAx Address High Nibble Register

The DMAx Address High register specifies the upper four bits of address for the Start/Current and End Addresses of DMAx.

Table 73. DMAx Address High Nibble Register (DMAxH)

BITS	7	6	5	4	3	2	1	0
FIELD	DMA_END_H				DMA_START_H			
RESET	X	X	X	X	X	X	X	X
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	FB2H, FHAH							

DMA_END_H—DMAx End Address High Nibble

These bits, used with the DMAx End Address Low register, form a 12-bit End Address. The full 12-bit address is given by {DMA_END_H[3:0], DMA_END[7:0]}.

DMA_START_H—DMAx Start/Current Address High Nibble

These bits, used with the DMAx Start/Current Address Low register, form a 12-bit Start/Current Address. The full 12-bit address is given by {DMA_START_H[3:0], DMA_START[7:0]}.

Table 76 provides an example of the Register File addresses if the DMA_ADC Address register contains the value 72H.

Table 76. DMA_ADC Register File Address Example

ADC Analog Input	Register File Address (Hex) ¹
0	720H-721H
1	722H-723H
2	724H-725H
3	726H-727H
4	728H-729H
5	72AH-72BH
6	72CH-72DH
7	72EH-72FH
8	730H-731H
9	732H-733H
10	734H-735H
11	736H-737H

¹ DMAA_ADDR set to 72H.

Table 77. DMA_ADC Address Register (DMAA_ADDR)

BITS	7	6	5	4	3	2	1	0
FIELD	DMAA_ADDR							Reserved
RESET	X	X	X	X	X	X	X	X
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	FBDH							

DMAA_ADDR—DMA_ADC Address

These bits specify the seven most-significant bits of the 12-bit Register File addresses used for storing the ADC output data. The ADC Analog Input Number defines the five least-significant bits of the Register File address. Full 12-bit address is {DMAA_ADDR[7:1], 4-bit ADC Analog Input Number, 0}.

Reserved

This bit is reserved and must be 0.

DMA Status Register

The DMA Status register indicates the DMA channel that generated the interrupt and the ADC Analog Input that is currently undergoing conversion. Reads from this register reset the Interrupt Request Indicator bits (IRQA, IRQ1, and IRQ0) to 0. Therefore, software interrupt service routines that read this register must process all three interrupt sources from the DMA.

Table 79. DMA_ADC Status Register (DMAA_STAT)

BITS	7	6	5	4	3	2	1	0
FIELD	CADC[3:0]				Reserved	IRQA	IRQ1	IRQ0
RESET	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R
ADDR	FBFH							

CADC[3:0]—Current ADC Analog Input

This field identifies the Analog Input that the ADC is currently converting.

Reserved

This bit is reserved and must be 0.

IRQA—DMA_ADC Interrupt Request Indicator

This bit is automatically reset to 0 each time a read from this register occurs.

0 = DMA_ADC is not the source of the interrupt from the DMA Controller.

1 = DMA_ADC completed transfer of data from the last ADC Analog Input and generated an interrupt.

IRQ1—DMA1 Interrupt Request Indicator

This bit is automatically reset to 0 each time a read from this register occurs.

0 = DMA1 is not the source of the interrupt from the DMA Controller.

1 = DMA1 completed transfer of data to/from the End Address and generated an interrupt.

IRQ0—DMA0 Interrupt Request Indicator

This bit is automatically reset to 0 each time a read from this register occurs.

0 = DMA0 is not the source of the interrupt from the DMA Controller.

1 = DMA0 completed transfer of data to/from the End Address and generated an interrupt.

On-Chip Debugger

Overview

The Z8F640x family devices have an integrated On-Chip Debugger (OCD) that provides advanced debugging features including:

- Reading and writing of the Register File
- Reading and writing of Program and Data Memory
- Setting of Breakpoints and Watchpoints
- Execution of eZ8 CPU instructions.

Architecture

The On-Chip Debugger consists of four primary functional blocks: transmitter, receiver, auto-baud generator, and debug controller. Figure 86 illustrates the architecture of the On-Chip Debugger

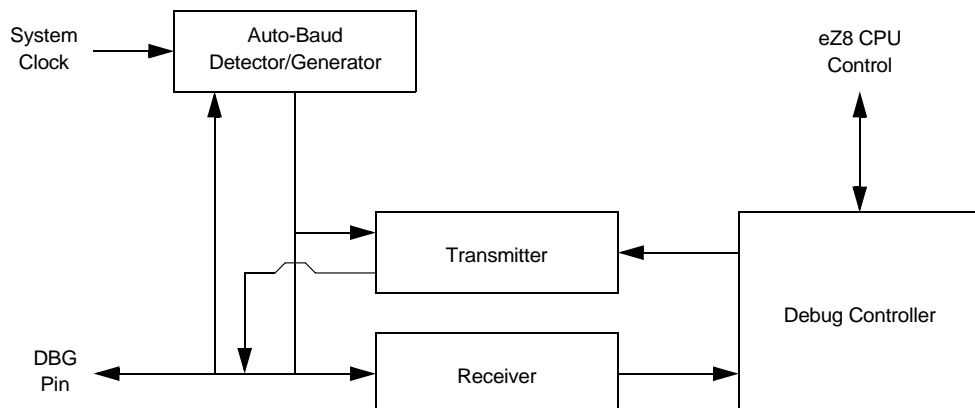


Figure 86. On-Chip Debugger Block Diagram

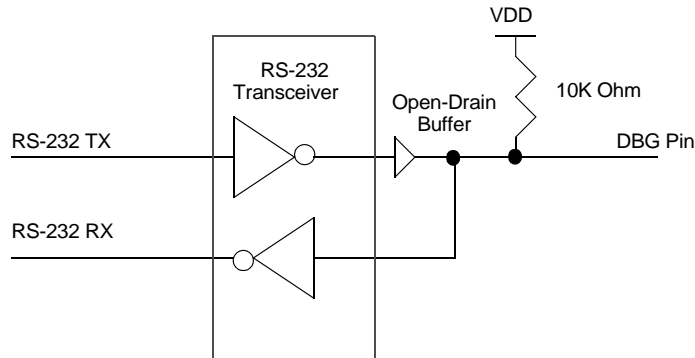


Figure 88. Interfacing the On-Chip Debugger's DBG Pin with an RS-232 Interface (2)

Debug Mode

The operating characteristics of the Z8F640x family devices in Debug mode are:

- The eZ8 CPU fetch unit stops, idling the eZ8 CPU, unless directed by the OCD to execute specific instructions.
- The system clock operates unless in Stop mode.
- All enabled on-chip peripherals operate unless in Stop mode.
- Automatically exits Halt mode.
- Constantly refreshes the Watch-Dog Timer, if enabled.

Entering Debug Mode

The Z8F640x family device enters Debug mode following any of the following operations:

- Writing the DBGMODE bit in the OCD Control Register to 1 using the OCD interface.
- eZ8 CPU execution of a BRK (Breakpoint) instruction (when enabled).
- Break upon a Watchpoint match.
- If the DBG pin is Low when the Z8F640x family device exits Reset, the On-Chip Debugger automatically puts the device into Debug mode.

Exiting Debug Mode

The device exits Debug mode following any of the following operations:

- Clearing the DBGMODE bit in the OCD Control Register to 0.



```
DBG <-- 03H
DBG --> RuntimeCounter[15:8]
DBG --> RuntimeCounter[7:0]
```

- **Write OCD Control Register (04H)**—The Write OCD Control Register command writes the data that follows to the OCDCTL register. When the Read Protect Option Bit is enabled, the DBGMODE bit (OCDCTL[7]) can only be set to 1, it cannot be cleared to 0 and the only method of putting the Z8F640x family device back into normal operating mode is to reset the device.

```
DBG <-- 04H
DBG <-- OCDCTL[7:0]
```

- **Read OCD Control Register (05H)**—The Read OCD Control Register command reads the value of the OCDCTL register.

```
DBG <-- 05H
DBG --> OCDCTL[7:0]
```

- **Write Program Counter (06H)**—The Write Program Counter command writes the data that follows to the eZ8 CPU's Program Counter (PC). If the Z8F640x family device is not in Debug mode or if the Read Protect Option Bit is enabled, the Program Counter (PC) values are discarded.

```
DBG <-- 06H
DBG <-- ProgramCounter[15:8]
DBG <-- ProgramCounter[7:0]
```

- **Read Program Counter (07H)**—The Read Program Counter command reads the value in the eZ8 CPU's Program Counter (PC). If the Z8F640x family device is not in Debug mode or if the Read Protect Option Bit is enabled, this command returns FFFFH.

```
DBG <-- 07H
DBG --> ProgramCounter[15:8]
DBG --> ProgramCounter[7:0]
```

- **Write Register (08H)**—The Write Register command writes data to the Register File. Data can be written 1-256 bytes at a time (256 bytes can be written by setting size to zero). If the Z8F640x family device is not in Debug mode, the address and data values are discarded. If the Read Protect Option Bit is enabled, then only writes to the Flash Control Registers are allowed and all other register write data values are discarded.

```
DBG <-- 08H
DBG <-- {4'h0, Register Address[11:8]}
DBG <-- Register Address[7:0]
DBG <-- Size[7:0]
DBG <-- 1-256 data bytes
```

- **Read Register (09H)**—The Read Register command reads data from the Register File. Data can be read 1-256 bytes at a time (256 bytes can be read by setting size to

RPEN—Read Protect Option Bit Enabled

0 = The Read Protect Option Bit is disabled (1).

0 = The Read Protect Option Bit is enabled (0), disabling many OCD commands.

Reserved

These bits are always 0.

OCD Watchpoint Control Register

The OCD Watchpoint Control register is used to configure the debug Watchpoint.

Table 96. OCD Watchpoint Control/Address (WPTCTL)

BITS	7	6	5	4	3	2	1	0
FIELD	WPW	WPR	WPDM	Reserved	WPTADDR[11:8]			
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

WPW—Watchpoint Break on Write

This bit cannot be set if the Read Protect Option Bit is enabled.

0 = Watchpoint Break on Register File write is disabled.

1 = Watchpoint Break on Register File write is enabled.

WPR—Watchpoint Break on Read

This bit cannot be set if the Read Protect Option Bit is enabled.

0 = Watchpoint Break on Register File read is disabled.

1 = Watchpoint Break on Register File write is enabled.

WPDM—Watchpoint Data Match

If this bit is set, then the Watchpoint only generates a Debug Break if the data being read or written matches the specified Watchpoint data. Either the WPR and/or WPW bits must also be set for this bit to affect operation. This bit cannot be set if the Read Protect Option Bit is enabled.

0 = Watchpoint Break on read and/or write does not require a data match.

1 = Watchpoint Break on read and/or write requires a data match.

Reserved

This bit is reserved and must be 0.

RADDR[11:8]—Register address

These bits specify the upper 4 bits of the Register File address to match when generating a Watchpoint Debug Break. The full 12-bit Register File address is given by {WPTCTL3:0, WPTADDR[7:0]}.

Figure 104 illustrates the 44-pin LQFP (low profile quad flat package) available for the Z8F1601, Z8F2401, Z8F3201, Z8F4801, and Z8F6401 devices.

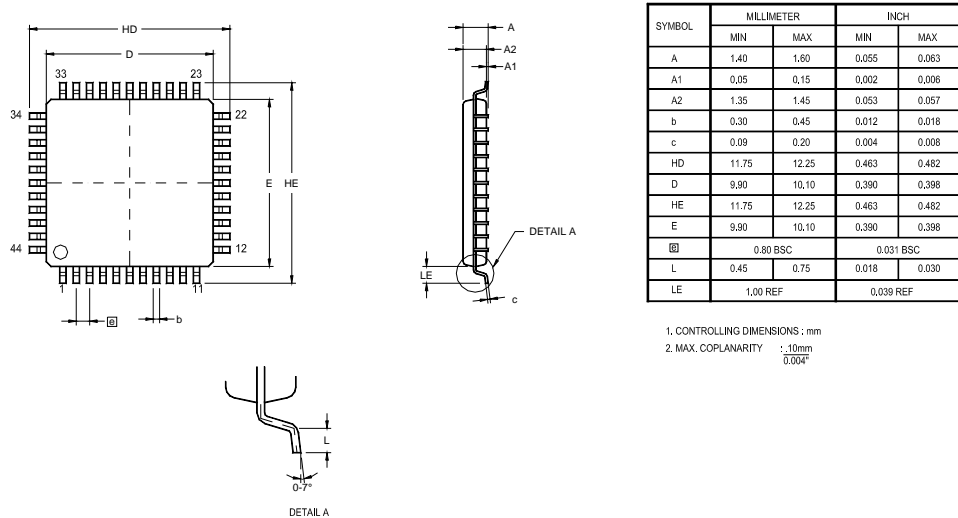


Figure 104. 44-Lead Low-Profile Quad Flat Package (LQFP)

Figure 105 illustrates the 44-pin PLCC (plastic lead chip carrier) package available for the Z8F1601, Z8F2401, Z8F3201, Z8F4801, and Z8F6401 devices.

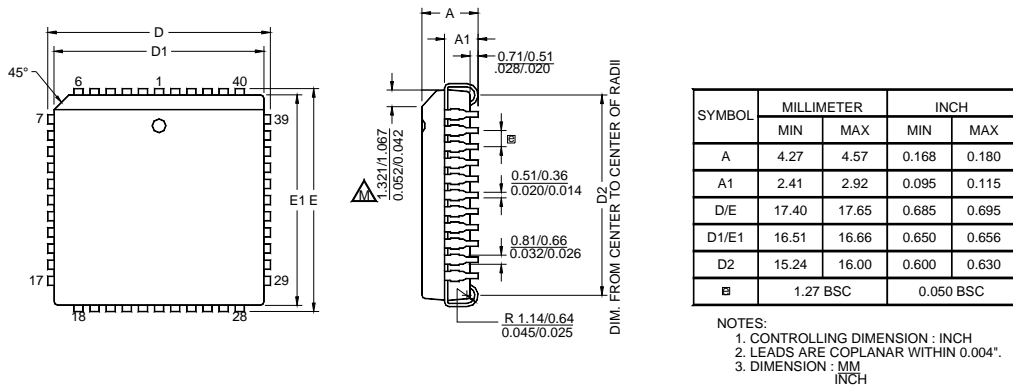


Figure 105. 44-Lead Plastic Lead Chip Carrier Package (PLCC)



Customer Feedback Form

The Z8 Encore!™ Product Specification

If you experience any problems while operating this product, or if you note any inaccuracies while reading this Product Specification, please copy and complete this form, then mail or fax it to ZiLOG (see *Return Information*, below). We also welcome your suggestions!

Customer Information

Name	Country
Company	Phone
Address	Fax
City/State/Zip	E-Mail

Product Information

Part #, Serial #, Board Fab #, or Rev. #
Software Version
Document Number
Host Computer Description/Type

Return Information

ZiLOG
532 Race Street
San Jose, CA 95126
Fax: (408) 558-8536
Email: tools@zillog.com



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