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Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	46
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	68-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f6402vs020sc00tr

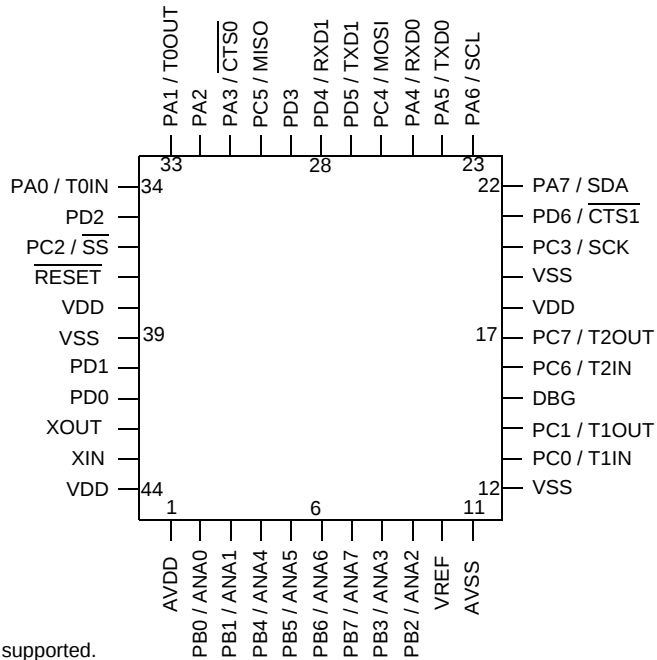


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Note: Timer 3 is not supported.

Figure 58. Z8Fxx01 in 44-Pin Low-Profile Quad Flat Package (LQFP)



Table 6. Register File Address Map (Continued)

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page #
FCE	Interrupt Port Select	IRQPS	00	55
FCF	Interrupt Control	IRQCTL	00	56
GPIO Port A				
FD0	Port A Address	PAADDR	00	37
FD1	Port A Control	PACTL	00	38
FD2	Port A Input Data	PAIN	XX	42
FD3	Port A Output Data	PAOUT	00	43
GPIO Port B				
FD4	Port B Address	PBADDR	00	37
FD5	Port B Control	PBCTL	00	38
FD6	Port B Input Data	PBIN	XX	42
FD7	Port B Output Data	PBOUT	00	43
GPIO Port C				
FD8	Port C Address	PCADDR	00	37
FD9	Port C Control	PCCTL	00	38
FDA	Port C Input Data	PCIN	XX	42
FDB	Port C Output Data	PCOUT	00	43
GPIO Port D				
FDC	Port D Address	PDADDR	00	37
FDD	Port D Control	PDCTL	00	38
FDE	Port D Input Data	PDIN	XX	42
FDF	Port D Output Data	PDOUT	00	43
GPIO Port E				
FE0	Port E Address	PEADDR	00	37
FE1	Port E Control	PECTL	00	38
FE2	Port E Input Data	PEIN	XX	42
FE3	Port E Output Data	PEOUT	00	43
GPIO Port F				
FE4	Port F Address	PFADDR	00	37
FE5	Port F Control	PFCTL	00	38
FE6	Port F Input Data	PFIN	XX	42
FE7	Port F Output Data	PFOUT	00	43
GPIO Port G				
FE8	Port G Address	PGADDR	00	37
FE9	Port G Control	PGCTL	00	38
FEA	Port G Input Data	PGIN	XX	42
FEB	Port G Output Data	PGOUT	00	43
GPIO Port H				
FEC	Port H Address	PHADDR	00	37
XX=Undefined				

Table 33. IRQ2 Enable High Bit Register (IRQ2ENH)

BITS	7	6	5	4	3	2	1	0
FIELD	T3ENH	U1RENH	U1TENH	DMAENH	C3ENH	C2ENH	C1ENH	C0ENH
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	FC7H							

T3ENH—Timer 3 Interrupt Request Enable High Bit
U1RENH—UART 1 Receive Interrupt Request Enable High Bit
U1TENH—UART 1 Transmit Interrupt Request Enable High Bit
DMAENH—DMA Interrupt Request Enable High Bit
C3ENH—Port C3 Interrupt Request Enable High Bit
C2ENH—Port C2 Interrupt Request Enable High Bit
C1ENH—Port C1 Interrupt Request Enable High Bit
C0ENH—Port C0 Interrupt Request Enable High Bit

Table 34. IRQ2 Enable Low Bit Register (IRQ2ENL)

BITS	7	6	5	4	3	2	1	0
FIELD	T3ENL	U1RENL	U1TENL	DMAENL	C3ENL	C2ENL	C1ENL	C0ENL
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	FC8H							

T3ENL—Timer 3 Interrupt Request Enable Low Bit
U1RENL—UART 1 Receive Interrupt Request Enable Low Bit
U1TENL—UART 1 Transmit Interrupt Request Enable Low Bit
DMAENL—DMA Interrupt Request Enable Low Bit
C3ENL—Port C3 Interrupt Request Enable Low Bit
C2ENL—Port C2 Interrupt Request Enable Low Bit
C1ENL—Port C1 Interrupt Request Enable Low Bit
C0ENL—Port C0 Interrupt Request Enable Low Bit

Interrupt Edge Select Register

The Interrupt Edge Select (IRQES) register (Table 35) determines whether an interrupt is generated for the rising edge or falling edge on the selected GPIO Port input pin. The



If the Timer reaches FFFFH, the timer rolls over to 0000H and continue counting.

The steps for configuring a timer for Compare mode and initiating the count are as follows:

1. Write to the Timer Control register to:
 - Disable the timer
 - Configure the timer for Compare mode.
 - Set the prescale value.
 - Set the initial logic level (High or Low) for the Timer Output alternate function, if desired.
2. Write to the Timer High and Low Byte registers to set the starting count value.
3. Write to the Timer Reload High and Low Byte registers to set the Compare value.
4. If desired, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
5. If using the Timer Output function, configure the associated GPIO port pin for the Timer Output alternate function.
6. Write to the Timer Control register to enable the timer and initiate counting.

In Compare mode, the system clock always provides the timer input. The Compare time is given by the following equation:

$$\text{Compare Mode Time (s)} = \frac{(\text{Compare Value} - \text{Start Value}) \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

Gated Mode

In Gated mode, the timer counts only when the Timer Input signal is in its active state (asserted), as determined by the TPOL bit in the Timer Control register. When the Timer Input signal is asserted, counting begins. A timer interrupt is generated when the Timer Input signal is deasserted or a timer reload occurs. To determine if a Timer Input signal deassertion generated the interrupt, read the associated GPIO input value and compare to the value stored in the TPOL bit.

The timer counts up to the 16-bit Reload value stored in the Timer Reload High and Low Byte registers. The timer input is the system clock. When reaching the Reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes (assuming the Timer Input signal is still asserted). Also, if the Timer Output alternate function is enabled, the Timer Output pin changes state (from Low to High or from High to Low) at timer reset.

The steps for configuring a timer for Gated mode and initiating the count are as follows:

1. Write to the Timer Control register to:
 - Disable the timer

information on approximate time-out delays for the minimum and maximum WDT reload values.

Table 45. Watch-Dog Timer Approximate Time-Out Delays

WDT Reload Value (Hex)	WDT Reload Value (Decimal)	Approximate Time-Out Delay (with 50kHz typical WDT oscillator frequency)	
		Typical	Description
000004	4	80μs	Minimum time-out delay
FFFFFF	16,777,215	335.5s	Maximum time-out delay

Watch-Dog Timer Refresh

When first enabled, the Watch-Dog Timer is loaded with the value in the Watch-Dog Timer Reload registers. The Watch-Dog Timer then counts down to 000000H unless a WDT instruction is executed by the eZ8 CPU. Execution of the WDT instruction causes the downcounter to be reloaded with the WDT Reload value stored in the Watch-Dog Timer Reload registers. Counting resumes following the reload operation.\

When the Z8F640x family device is operating in Debug Mode (via the On-Chip Debugger), the Watch-Dog Timer is continuously refreshed to prevent spurious Watch-Dog Timer time-outs.

Watch-Dog Timer Time-Out Response

The Watch-Dog Timer times out when the counter reaches 000000H. A time-out of the Watch-Dog Timer generates either an interrupt or a Short Reset. The WDT_RES Option Bit determines the time-out response of the Watch-Dog Timer. Refer to the **Option Bits** chapter for information regarding programming of the WDT_RES Option Bit.

WDT Interrupt in Normal Operation

If configured to generate an interrupt when a time-out occurs, the Watch-Dog Timer issues an interrupt request to the interrupt controller and sets the WDT status bit in the Watch-Dog Timer Control register. If interrupts are enabled, the eZ8 CPU responds to the interrupt request by fetching the Watch-Dog Timer interrupt vector and executing code from the vector address. After time-out and interrupt generation, the Watch-Dog Timer counter rolls over to its maximum value of FFFFFH and continues counting. The Watch-Dog Timer counter is not automatically returned to its Reload Value.

WDT Interrupt in Stop Mode

If configured to generate an interrupt when a time-out occurs and the Z8F640x family device is in STOP mode, the Watch-Dog Timer automatically initiates a STOP Mode Recovery and generates an interrupt request. Both the WDT status bit and the STOP bit in the Watch-Dog Timer Control register are set to 1 following WDT time-out in STOP



mode. Refer to the **Reset and Stop Mode Recovery** chapter for more information on STOP Mode Recovery.

If interrupts are enabled, following completion of the Stop Mode Recovery the eZ8 CPU responds to the interrupt request by fetching the Watch-Dog Timer interrupt vector and executing code from the vector address.

WDT Reset in Normal Operation

If configured to generate a Reset when a time-out occurs, the Watch-Dog Timer forces the Z8F640x family device into the Short Reset state. The WDT status bit in the Watch-Dog Timer Control register is set to 1. Refer to the **Reset and Stop Mode Recovery** chapter for more information on Short Reset.

WDT Reset in Stop Mode

If configured to generate a Reset when a time-out occurs and the Z8F640x family device is in STOP mode, the Watch-Dog Timer initiates a Stop Mode Recovery. Both the WDT status bit and the STOP bit in the Watch-Dog Timer Control register are set to 1 following WDT time-out in STOP mode. Refer to the **Reset and Stop Mode Recovery** chapter for more information.

Watch-Dog Timer Reload Unlock Sequence

Writing the unlock sequence to the Watch-Dog Timer Control register (WDTCTL) unlocks the three Watch-Dog Timer Reload Byte registers (WDTU, WDTL, and WDTL) to allow changes to the time-out period. These write operations to the WDTCTL register address produce no effect on the bits in the WDTCTL register. The locking mechanism prevents spurious writes to the Reload registers. The follow sequence is required to unlock the Watch-Dog Timer Reload Byte registers (WDTU, WDTL, and WDTL) for write access.

1. Write 55H to the Watch-Dog Timer Control register (WDTCTL)
2. Write AAH to the Watch-Dog Timer Control register (WDTCTL)
3. Write the Watch-Dog Timer Reload Upper Byte register (WDTU)
4. Write the Watch-Dog Timer Reload High Byte register (WDTL)
5. Write the Watch-Dog Timer Reload Low Byte register (WDTL)

All three Watch-Dog Timer Reload registers must be written in the order just listed. There must be no other register writes between each of these operations. If a register write occurs, the lock state machine resets and no further writes can occur, unless the sequence is restarted. The value in the Watch-Dog Timer Reload registers is loaded into the counter when the Watch-Dog Timer is first enabled and every time a WDT instruction is executed.

3. Enable the Baud Rate Generator timer function and associated interrupt by setting the BIRQ bit in the UARTx Control 1 register to 1.

UART Control Register Definitions

The UART control registers support both the UARTs and the associated Infrared Encoder/Decoders. For more information on the infrared operation, refer to the **Infrared Encoder/Decoder** chapter on page 95.

UARTx Transmit Data Register

Data bytes written to the UARTx Transmit Data register (Table 50) are shifted out on the TXDx pin. The Write-only UARTx Transmit Data register shares a Register File address with the Read-only UARTx Receive Data register.

Table 50. UARTx Transmit Data Register (UxTXD)

BITS	7	6	5	4	3	2	1	0
FIELD	TXD							
RESET	X	X	X	X	X	X	X	X
R/W	W	W	W	W	W	W	W	W
ADDR	F40H and F48H							

TXD—Transmit Data

UART transmitter data byte to be shifted out through the TXDx pin.



Table 58. UART Baud Rates (Continued)

10.0 MHz System Clock				5.5296 MHz System Clock			
Desired Rate	BRG Divisor	Actual Rate	Error	Desired Rate	BRG Divisor	Actual Rate	Error
(kHz)	(Decimal)	(kHz)	(%)	(kHz)	(Decimal)	(kHz)	(%)
1250.0	N/A	N/A	N/A	1250.0	N/A	N/A	N/A
625.0	1	625.0	0.00	625.0	N/A	N/A	N/A
250.0	3	208.33	-16.67	250.0	1	345.6	38.24
115.2	5	125.0	8.51	115.2	3	115.2	0.00
57.6	11	56.8	-1.36	57.6	6	57.6	0.00
38.4	16	39.1	1.73	38.4	9	38.4	0.00
19.2	33	18.9	0.16	19.2	18	19.2	0.00
9.60	65	9.62	0.16	9.60	36	9.60	0.00
4.80	130	4.81	0.16	4.80	72	4.80	0.00
2.40	260	2.40	-0.03	2.40	144	2.40	0.00
1.20	521	1.20	-0.03	1.20	288	1.20	0.00
0.60	1042	0.60	-0.03	0.60	576	0.60	0.00
0.30	2083	0.30	0.02	0.30	1152	0.30	0.00

3.579545 MHz System Clock				1.8432 MHz System Clock			
Desired Rate	BRG Divisor	Actual Rate	Error	Desired Rate	BRG Divisor	Actual Rate	Error
(kHz)	(Decimal)	(kHz)	(%)	(kHz)	(Decimal)	(kHz)	(%)
1250.0	N/A	N/A	N/A	1250.0	N/A	N/A	N/A
625.0	N/A	N/A	N/A	625.0	N/A	N/A	N/A
250.0	1	223.72	-10.51	250.0	N/A	N/A	N/A
115.2	2	111.9	-2.90	115.2	1	115.2	0.00
57.6	4	55.9	-2.90	57.6	2	57.6	0.00
38.4	6	37.3	-2.90	38.4	3	38.4	0.00
19.2	12	18.6	-2.90	19.2	6	19.2	0.00
9.60	23	9.73	1.32	9.60	12	9.60	0.00
4.80	47	4.76	-0.83	4.80	24	4.80	0.00
2.40	93	2.41	0.23	2.40	48	2.40	0.00
1.20	186	1.20	0.23	1.20	96	1.20	0.00
0.60	373	0.60	-0.04	0.60	192	0.60	0.00
0.30	746	0.30	-0.04	0.30	384	0.30	0.00

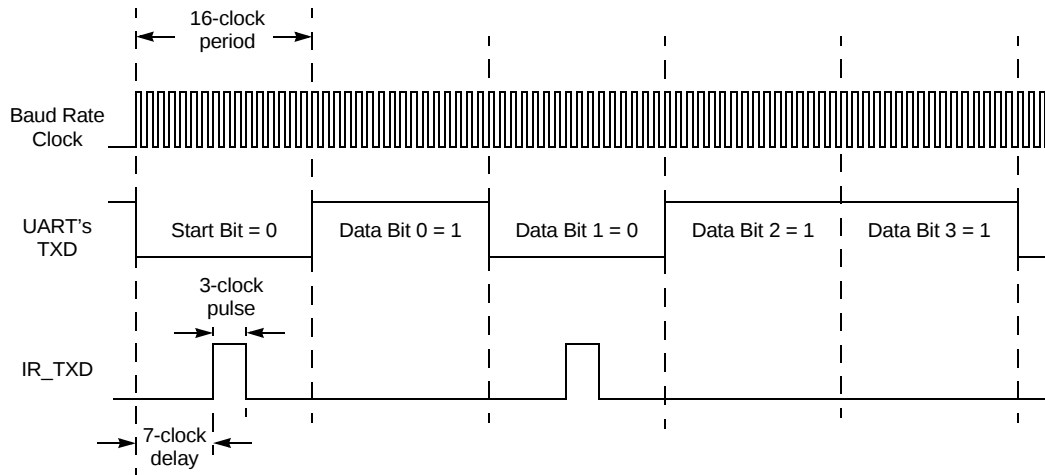


Figure 72. Infrared Data Transmission

Receiving IrDA Data

Data received from the infrared transceiver via the IR_RXD signal through the RXD pin is decoded by the Infrared Endec and passed to the UART. The UART's baud rate clock is used by the Infrared Endec to generate the demodulated signal (RXD) that drives the UART. Each UART/Infrared data bit is 16-clocks wide. Figure 73 illustrates data reception. When the Infrared Endec is enabled, the UART's RXD signal is internal to the Z8F640x family device while the IR_RXD signal is received through the RXD pin.

2. The I²C Controller waits for the slave to send an Acknowledge (by pulling the SDA signal Low). If the slave pulls the SDA signal High (Not-Acknowledge), the I²C Controller sends a Stop signal.
3. If the slave needs to service an interrupt, it pulls the SCL signal Low, which halts I²C operation.
4. If there is no other data in the I²C Data register or the STOP bit in the I²C Control register is set by software, then the Stop signal is sent.

Figure 79 illustrates the data transfer format for a 7-bit addressed slave. Shaded regions indicate data transferred from the I²C Controller to slaves and unshaded regions indicate data transferred from the slaves to the I²C Controller.



Figure 79. 7-Bit Addressed Slave Data Transfer Format

The data transfer format for a transmit operation on a 7-bit addressed slave is as follows:

1. Software asserts the IEN bit in the I²C Control register.
2. Software asserts the TXI bit of the I²C Control register to enable Transmit interrupts.
3. The I²C interrupt asserts, because the I²C Data register is empty
4. Software responds to the TDRE bit by writing a 7-bit slave address followed by a 0 (write) to the I²C Data register.
5. Software asserts the START bit of the I²C Control register.
6. The I²C Controller sends the START condition to the I²C slave.
7. The I²C Controller loads the I²C Shift register with the contents of the I²C Data register.
8. After one bit of address has been shifted out by the SDA signal, the Transmit interrupt is asserted.
9. Software responds by writing the contents of the data into the I²C Data register.
10. The I²C Controller shifts the rest of the address and write bit out by the SDA signal.
11. The I²C slave sends an acknowledge (by pulling the SDA signal low) during the next high period of SCL. The I²C Controller sets the ACK bit in the I²C Status register.
12. The I²C Controller loads the contents of the I²C Shift register with the contents of the I²C Data register.
13. The I²C Controller shifts the data out of via the SDA signal. After the first bit is sent, the Transmit interrupt is asserted.



Direct Memory Access Controller

Overview

The Z8F640x family device's Direct Memory Access (DMA) Controller provides three independent Direct Memory Access channels. Two of the channels (DMA0 and DMA1) transfer data between the on-chip peripherals and the Register File. The third channel (DMA_ADC) controls the Analog-to-Digital Converter (ADC) operation and transfers the Single-Shot mode ADC output data to the Register File.

Operation

DMA0 and DMA1 Operation

DMA0 and DMA1, referred to collectively as DMAx, transfer data either from the on-chip peripheral control registers to the Register File, or from the Register File to the on-chip peripheral control registers. The sequence of operations in a DMAx data transfer is:

1. DMAx trigger source requests a DMA data transfer.
2. DMAx requests control of the system bus (address and data) from the eZ8 CPU.
3. After the eZ8 CPU acknowledges the bus request, DMAx transfers either a single byte or a two-byte word (depending upon configuration) and then returns system bus control back to the eZ8 CPU.
4. If Current Address equals End Address:
 - DMAx reloads the original Start Address
 - If configured to generate an interrupt, DMAx sends an interrupt request to the Interrupt Controller
 - If configured for single-pass operation, DMAx resets the DEN bit in the DMAx Control register to 0 and the DMA is disabled.

If Current Address does not equal End Address, the Current Address increments by 1 (single-byte transfer) or 2 (two-byte word transfer).

When the DMA is configured for two-byte word transfers, the DMAx I/O Address register must contain an even numbered address.

Table 72. DMAx I/O Address Register (DMAxIO)

BITS	7	6	5	4	3	2	1	0
FIELD	DMA_IO							
RESET	X	X	X	X	X	X	X	X
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	FB1H, FB9H							

DMA_IO—DMA on-chip peripheral control register address

This byte sets the low byte of the on-chip peripheral control register address on Register File Page FH (addresses F00H to FFFH).

DMAx Address High Nibble Register

The DMAx Address High register specifies the upper four bits of address for the Start/Current and End Addresses of DMAx.

Table 73. DMAx Address High Nibble Register (DMAxH)

BITS	7	6	5	4	3	2	1	0
FIELD	DMA_END_H				DMA_START_H			
RESET	X	X	X	X	X	X	X	X
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADDR	FB2H, FHAH							

DMA_END_H—DMAx End Address High Nibble

These bits, used with the DMAx End Address Low register, form a 12-bit End Address. The full 12-bit address is given by {DMA_END_H[3:0], DMA_END[7:0]}.

DMA_START_H—DMAx Start/Current Address High Nibble

These bits, used with the DMAx Start/Current Address Low register, form a 12-bit Start/Current Address. The full 12-bit address is given by {DMA_START_H[3:0], DMA_START[7:0]}.

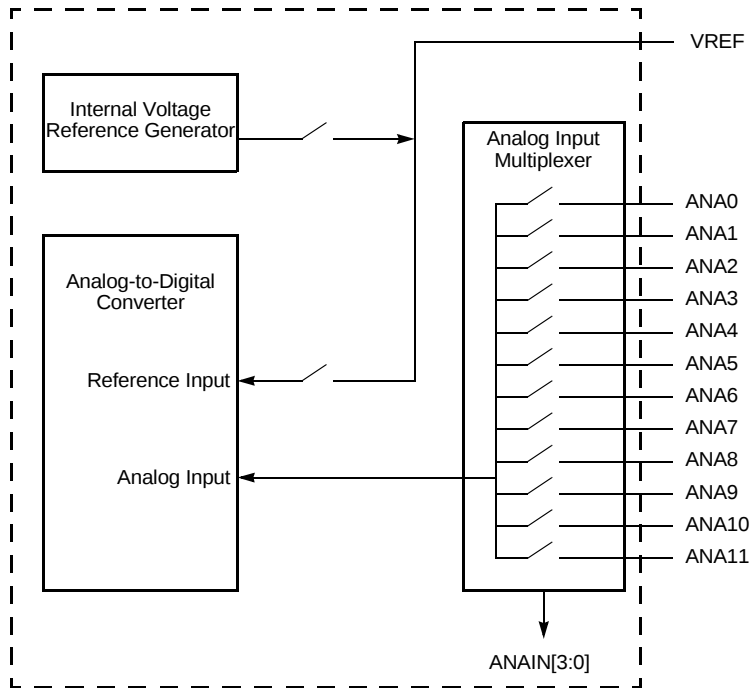


Figure 83. Analog-to-Digital Converter Block Diagram

Operation

Automatic Power-Down

If the ADC is idle (no conversions in progress) for 160 consecutive system clock cycles, portions of the ADC are automatically powered-down. From this power-down state, the ADC requires 40 system clock cycles to power-up. The ADC powers up when a conversion is requested using the ADC Control register.

Single-Shot Conversion

When configured for single-shot conversion, the ADC performs a single analog-to-digital conversion on the selected analog input channel. After completion of the conversion, the ADC shuts down. The steps for setting up the ADC and initiating a single-shot conversion are as follows:

ADC Data High Byte Register

The ADC Data High Byte register contains the upper eight bits of the 10-bit ADC output. During a conversion, this value is invalid. Access to the ADC Data High Byte register is read-only. The full 10-bit ADC result is given by {ADCD_H[7:0], ADCD_L[7:6]}.

Table 81. ADC Data High Byte Register (ADCD_H)

BITS	7	6	5	4	3	2	1	0
FIELD	ADCD_H							
RESET	X							
R/W	R							
ADDR	F72H							

ADCD_H—ADC Data High Byte

This byte contains the upper eight bits of the 10-bit ADC output. These bits are not valid during a conversion. These bits are undefined after a Reset.

ADC Data Low Bits Register

The ADC Data Low Bits register contains the lower two bits of the conversion value. During a conversion this value is invalid. Access to the ADC Data Low Bits register is read-only. The full 10-bit ADC result is given by {ADCD_H[7:0], ADCD_L[7:6]}.

Table 82. ADC Data Low Bits Register (ADCD_L)

BITS	7	6	5	4	3	2	1	0
FIELD	ADCD_L		Reserved					
RESET	X		X					
R/W	R		R					
ADDR	F73H							

ADCD_L—ADC Data Low Bits

These are the least significant two bits of the 10-bit ADC output. During a conversion, this value is invalid. These bits are undefined after a Reset.

Reserved

These bits are reserved and are always undefined.



Table 126. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode		Opcode(s) (Hex)	Flags						Fetch Cycles	Instr. Cycles
		dst	src		C	Z	S	V	D	H		
LD dst, rc	dst ← src	r	IM	0C-FC	-	-	-	-	-	-	2	2
		r	X(r)	C7							3	3
		X(r)	r	D7							3	4
		r	Ir	E3							2	3
		R	R	E4							3	2
		R	IR	E5							3	3
		R	IM	E6							3	3
		IR	IM	E7							3	3
		Ir	r	F3							2	3
		IR	R	F5							3	3
LDC dst, src	dst ← src	r	Irr	C2	-	-	-	-	-	-	2	5
		Ir	Irr	C5							2	9
		Irr	r	D2							2	5
LDCI dst, src	dst ← src	Ir	Irr	C3	-	-	-	-	-	-	2	9
	r ← r + 1 rr ← rr + 1	Irr	Ir	D3							2	9
LDE dst, src	dst ← src	r	Irr	82	-	-	-	-	-	-	2	5
		Irr	r	92							2	5
LDEI dst, src	dst ← src	Ir	Irr	83	-	-	-	-	-	-	2	9
	r ← r + 1 rr ← rr + 1	Irr	Ir	93							2	9
Flags Notation:		* = Value is a function of the result of the operation.			0 = Reset to 0 - = Unaffected X = Undefined							

Table 126. eZ8 CPU Instruction Summary (Continued)

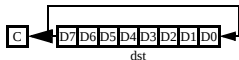
Assembly Mnemonic	Symbolic Operation	Address Mode		Opcode(s) (Hex)	Flags						Fetch Cycles	Instr. Cycles
		dst	src		C	Z	S	V	D	H		
POP dst	dst ← @SP	R		50	-	-	-	-	-	-	2	2
	SP ← SP + 1	IR		51							2	3
POPX dst	dst ← @SP	ER		D8	-	-	-	-	-	-	3	2
	SP ← SP + 1											
PUSH src	SP ← SP − 1	R		70	-	-	-	-	-	-	2	2
	@SP ← src	IR		71							2	3
PUSHX src	SP ← SP − 1	ER		C8	-	-	-	-	-	-	3	2
	@SP ← src											
RCF	C ← 0			CF	0	-	-	-	-	-	1	2
RET	PC ← @SP			AF	-	-	-	-	-	-	1	4
RL dst		R		90	*	*	*	*	-	-	2	2
		IR		91							2	3
RLC dst		R		10	*	*	*	*	-	-	2	2
		IR		11							2	3
RR dst		R		E0	*	*	*	*	-	-	2	2
		IR		E1							2	3
RRC dst		R		C0	*	*	*	*	-	-	2	2
		IR		C1							2	3
Flags Notation:												
* = Value is a function of the result of the operation.					0 = Reset to 0							
- = Unaffected					1 = Set to 1							
X = Undefined												



Table 128. Ordering Information (Continued)

Part	Flash KB (Bytes)	RAM KB (Bytes)	Max. Speed (MHz)	Temp (°C)	Voltage (V)	Package	Part Number
Z8 Encore!® with 64KB Flash, Standard Temperature							
Z8 Encore!®	64 (65,536)	4 (4096)	20	0 to +70	3.0 - 3.6	PDIP-40	Z8F6401PM020SC
Z8 Encore!®	64 (65,536)	4 (4096)	20	0 to +70	3.0 - 3.6	LQFP-44	Z8F6401AN020SC
Z8 Encore!®	64 (65,536)	4 (4096)	20	0 to +70	3.0 - 3.6	PLCC-44	Z8F6401VN020SC
Z8 Encore!®	64 (65,536)	4 (4096)	20	0 to +70	3.0 - 3.6	LQFP-64	Z8F6402AR020SC
Z8 Encore!®	64 (65,536)	4 (4096)	20	0 to +70	3.0 - 3.6	PLCC-68	Z8F6402VS020SC
Z8 Encore!®	64 (65,536)	4 (4096)	20	0 to +70	3.0 - 3.6	QFP-80	Z8F6403FT020SC
Z8 Encore!® with 16KB Flash, Extended Temperature							
Z8 Encore!®	16 (16,384)	2 (2048)	20	-40 to +105	3.0 - 3.6	PDIP-40	Z8F1601PM020EC
Z8 Encore!®	16 (16,384)	2 (2048)	20	-40 to +105	3.0 - 3.6	LQFP-44	Z8F1601AN020EC
Z8 Encore!®	16 (16,384)	2 (2048)	20	-40 to +105	3.0 - 3.6	PLCC-44	Z8F1601VN020EC
Z8 Encore!®	16 (16,384)	2 (2048)	20	-40 to +105	3.0 - 3.6	LQFP-64	Z8F1602AR020EC
Z8 Encore!®	16 (16,384)	2 (2048)	20	-40 to +105	3.0 - 3.6	PLCC-68	Z8F1602VS020EC
Z8 Encore!® with 24KB Flash, Extended Temperature							
Z8 Encore!®	24 (24,576)	2 (2048)	20	-40 to +105	3.0 - 3.6	PDIP-40	Z8F2401PM020EC
Z8 Encore!®	24 (24,576)	2 (2048)	20	-40 to +105	3.0 - 3.6	LQFP-44	Z8F2401AN020EC
Z8 Encore!®	24 (24,576)	2 (2048)	20	-40 to +105	3.0 - 3.6	PLCC-44	Z8F2401VN020EC
Z8 Encore!®	24 (24,576)	2 (2048)	20	-40 to +105	3.0 - 3.6	LQFP-64	Z8F2402AR020EC
Z8 Encore!®	24 (24,576)	2 (2048)	20	-40 to +105	3.0 - 3.6	PLCC-68	Z8F2402VS020EC
Z8 Encore!® with 32KB Flash, Extended Temperature							
Z8 Encore!®	32 (32,768)	2 (2048)	20	-40 to +105	3.0 - 3.6	PDIP-40	Z8F3201PM020EC
Z8 Encore!®	32 (32,768)	2 (2048)	20	-40 to +105	3.0 - 3.6	LQFP-44	Z8F3201AN020EC
Z8 Encore!®	32 (32,768)	2 (2048)	20	-40 to +105	3.0 - 3.6	PLCC-44	Z8F3201VN020EC
Z8 Encore!®	32 (32,768)	2 (2048)	20	-40 to +105	3.0 - 3.6	LQFP-64	Z8F3202AR020EC
Z8 Encore!®	32 (32,768)	2 (2048)	20	-40 to +105	3.0 - 3.6	PLCC-68	Z8F3202VS020EC



Customer Feedback Form

The Z8 Encore!™ Product Specification

If you experience any problems while operating this product, or if you note any inaccuracies while reading this Product Specification, please copy and complete this form, then mail or fax it to ZiLOG (see *Return Information*, below). We also welcome your suggestions!

Customer Information

Name	Country
Company	Phone
Address	Fax
City/State/Zip	E-Mail

Product Information

Part #, Serial #, Board Fab #, or Rev. #
Software Version
Document Number
Host Computer Description/Type

Return Information

ZiLOG
532 Race Street
San Jose, CA 95126
Fax: (408) 558-8536
Email: tools@zillog.com