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Details

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Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	30 MIPs
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	30
Program Memory Size	24KB (8K x 24)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 13x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic30f3014-30i-p

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Pin Diagrams (Continued)





CORE REGISTER MAP⁽¹⁾ (CONTINUED) **TABLE 3-3:**

	•. •						,											
SFR Name	Address (Home)	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
CORCON	0044	—		_	US	EDT	DL2	DL1	DL0	SATA	SATB	SATDW	ACCSAT	IPL3	PSV	RND	IF	0000 0000 0010 0000
MODCON	0046	XMODEN	YMODEN	—	—		BWN	1<3:0>			YW	M<3:0>			XWM<	:3:0>		0000 0000 0000 0000
XMODSRT	0048		XS<15:1> 0 ע									uuuu uuuu uuuu uuu0						
XMODEND	004A							XI	E<15:1>								1	uuuu uuuu uuul
YMODSRT	004C							YS	S<15:1>								0	uuuu uuuu uuuu uuu0
YMODEND	004E			YE<15:1> 1 u								uuuu uuuu uuul						
XBREV	0050	BREN	XB<14:0> υ								uuuu uuuu uuuu uuuu							
DISICNT	0052	_	_	— DISICNT<13:0> 0								0000 0000 0000 0000						

Legend:

u = uninitialized bit; — = unimplemented bit, read as '0'
 Refer to the "dsPIC30F Family Reference Manual" (DS70046) for descriptions of register bit fields.

4.1.3 MOVE AND ACCUMULATOR INSTRUCTIONS

Move instructions and the DSP accumulator class of instructions provide a greater degree of addressing flexibility than other instructions. In addition to the addressing modes supported by most MCU instructions, move and accumulator instructions also support Register Indirect with Register Offset Addressing mode, also referred to as Register Indexed mode.

Note: For the MOV instructions, the addressing mode specified in the instruction can differ for the source and destination EA. However, the 4-bit Wb (register offset) field is shared between both source and destination (but typically only used by one).

In summary, the following addressing modes are supported by move and accumulator instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-Modified
- Register Indirect Pre-Modified
- Register Indirect with Register Offset (Indexed)
- Register Indirect with Literal Offset
- 8-bit Literal
- 16-bit Literal

Note: Not all instructions support all the addressing modes given above. Individual instructions may support different subsets of these addressing modes.

4.1.4 MAC INSTRUCTIONS

The dual source operand DSP instructions (CLR, ED, EDAC, MAC, MPY, MPY.N, MOVSAC and MSC), also referred to as MAC instructions, utilize a simplified set of addressing modes to allow the user to effectively manipulate the Data Pointers through register indirect tables.

The two source operand prefetch registers must be a member of the set {W8, W9, W10, W11}. For data reads, W8 and W9 is always directed to the X RAGU, and W10 and W11 are always directed to the Y AGU. The Effective Addresses generated (before and after modification) must, therefore, be valid addresses within X data space for W8 and W9 and Y data space for W10 and W11.

Note: Register Indirect with Register Offset addressing is only available for W9 (in X space) and W11 (in Y space). In summary, the following addressing modes are supported by the ${\tt MAC}$ class of instructions:

- Register Indirect
- Register Indirect Post-Modified by 2
- Register Indirect Post-Modified by 4
- Register Indirect Post-Modified by 6
- Register Indirect with Register Offset (Indexed)

4.1.5 OTHER INSTRUCTIONS

Besides the various addressing modes outlined above, some instructions use literal constants of various sizes. For example, BRA (branch) instructions use 16-bit signed literals to specify the branch destination directly, whereas the DISI instruction uses a 14-bit unsigned literal field. In some instructions, such as ADD Acc, the source of an operand or result is implied by the opcode itself. Certain operations, such as NOP, do not have any operands.

4.2 Modulo Addressing

Modulo Addressing is a method of providing an automated means to support circular data buffers using hardware. The objective is to remove the need for software to perform data address boundary checks when executing tightly looped code, as is typical in many DSP algorithms.

Modulo Addressing can operate in either data or program space (since the data pointer mechanism is essentially the same for both). One circular buffer can be supported in each of the X (which also provides the pointers into program space) and Y data spaces. Modulo Addressing can operate on any W register pointer. However, it is not advisable to use W14 or W15 for Modulo Addressing since these two registers are used as the Stack Frame Pointer and Stack Pointer, respectively.

In general, any particular circular buffer can only be configured to operate in one direction, as there are certain restrictions on the buffer start address (for incrementing buffers), or end address (for decrementing buffers) based upon the direction of the buffer.

The only exception to the usage restrictions is for buffers that have a power-of-2 length. As these buffers satisfy the start and end address criteria, they may operate in a Bidirectional mode (i.e., address boundary checks are performed on both the lower and upper address boundaries).

11.0 TIMER4/5 MODULE

Note: This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the *dsPIC30F Family Reference Manual* (DS70046).

This section describes the second 32-bit general purpose timer module (Timer4/5) and associated operational modes. Figure 11-1 depicts the simplified block diagram of the 32-bit Timer4/5 module. Figure 11-2 and Figure 11-3 show Timer4/5 configured as two independent 16-bit timers, Timer4 and Timer5, respectively.

The Timer4/5 module is similar in operation to the Timer2/3 module. However, there are some differences:

- The Timer4/5 module does not support the ADC event trigger feature
- Timer4/5 can not be utilized by other peripheral modules, such as input capture and output compare

The operating modes of the Timer4/5 module are determined by setting the appropriate bit(s) in the 16-bit T4CON and T5CON SFRs.

For 32-bit timer/counter operation, Timer4 is the lsw and Timer5 is the msw of the 32-bit timer.

Note: For 32-bit timer operation, T5CON control bits are ignored. Only T4CON control bits are used for setup and control. Timer4 clock and gate inputs are utilized for the 32-bit timer module but an interrupt is generated with the Timer5 Interrupt Flag (T5IF) and the interrupt is enabled with the Timer5 interrupt enable bit (T5IE).



TABLE 13-1: dsPIC30F3014 OUTPUT COMPARE REGISTER MAP⁽¹⁾

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
OC1RS	DC1RS 0180 Output Compare 1 Secondary Register												0000 0000 0000 0000					
OC1R	0182	Output Compare 1 Main Register										0000 0000 0000 0000						
OC1CON	0184	_	—	OCSIDL	_	_	—	_	_	-	_	_	OCFLT	OCTSEL		OCM<2:0>		0000 0000 0000 0000
OC2RS	0186							Outpu	ut Compar	e 2 Secon	dary Regi	ster						0000 0000 0000 0000
OC2R	0188							Οι	utput Com	oare 2 Mai	in Registe	r						0000 0000 0000 0000
OC2CON	018A		—	OCSIDL	_	_	—	_	—	—	_	_	OCFLT	OCTSE		OCM<2:0>		0000 0000 0000 0000
Logondi		molomor	tod bit ro	ad an '0'														

Legend: = unimplemented bit, read as '0

Note 1: Refer to the "dsPIC30F Family Reference Manual" (DS70046) for descriptions of register bit fields.

TABLE 13-2: dsPIC30F4013 OUTPUT COMPARE REGISTER MAP⁽¹⁾

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
OC1RS	0180							Outpu	ut Compar	e 1 Secon	dary Regi	ster						0000 0000 0000 0000
OC1R	0182		Output Compare 1 Main Register											0000 0000 0000 0000				
OC1CON	0184	_	—	OCSIDL	_	_	—	—	_	_	_	_	OCFLT	OCTSEL		OCM<2:0>	•	0000 0000 0000 0000
OC2RS	0186							Outpu	ut Compar	e 2 Secon	dary Regi	ster						0000 0000 0000 0000
OC2R	0188							Ou	Itput Com	pare 2 Ma	in Registe	r						0000 0000 0000 0000
OC2CON	018A	_	—	OCSIDL	_	_	—	—	_	_	_	_	OCFLT	OCTSE		OCM<2:0>	•	0000 0000 0000 0000
OC3RS	018C							Outpu	ut Compar	e 3 Secon	dary Regi	ster						0000 0000 0000 0000
OC3R	018E							Ou	Itput Com	pare 3 Ma	in Registe	r						0000 0000 0000 0000
OC3CON	0190	_	—	OCSIDL	_	_	—	—	_	_	_	_	OCFLT	OCTSEL		OCM<2:0>	•	0000 0000 0000 0000
OC4RS	0192		Output Compare 4 Secondary Register									0000 0000 0000 0000						
OC4R	0194		Output Compare 4 Main Register									0000 0000 0000 0000						
OC4CON	0196	_	_	OCSIDL	_	_	_	_	_	_	_	_	OCFLT	OCTSEL		OCM<2:0>	•	0000 0000 0000 0000

Legend: --- = unimplemented bit, read as '0'

Refer to the "dsPIC30F Family Reference Manual" (DS70046) for descriptions of register bit fields. Note 1:

14.2 I²C Module Addresses

The I2CADD register contains the Slave mode addresses. The register is a 10-bit register.

If the A10M bit (I2CCON<10>) is '0', the address is interpreted by the module as a 7-bit address. When an address is received, it is compared to the 7 LSbs of the I2CADD register.

If the A10M bit is '1', the address is assumed to be a 10-bit address. When an address is received, it is compared with the binary value, '11110 A9 A8' (where A9 and A8 are two Most Significant bits of I2CADD). If that value matches, the next address is compared with the Least Significant 8 bits of I2CADD, as specified in the 10-bit addressing protocol.

TABLE 14-1: 7-BIT I²C[™] SLAVE ADDRESSES SUPPORTED BY dsPIC30F

0x00	General Call Address or Start Byte
0x01-0x03	Reserved
0x04-0x07	HS mode Master Codes
0x08-0x77	Valid 7-Bit Addresses
0x78-0x7b	Valid 10-Bit Addresses (lower 7 bits)
0x7c-0x7f	Reserved

14.3 I²C 7-Bit Slave Mode Operation

Once enabled (I2CEN = 1), the slave module waits for a Start bit to occur (i.e., the I²C module is 'Idle'). Following the detection of a Start bit, 8 bits are shifted into I2CRSR, and the address is compared against I2CADD. In 7-bit mode (A10M = 0), bits I2CADD<6:0> are compared against I2CRSR<7:1> and I2CRSR<0> is the R_W bit. All incoming bits are sampled on the rising edge of SCL.

If an address match occurs, an Acknowledgement is sent and the Slave Event Interrupt Flag (SI2CIF) is set on the falling edge of the ninth (ACK) bit. The address match does not affect the contents of the I2CRCV buffer or the RBF bit.

14.3.1 SLAVE TRANSMISSION

If the R_W bit received is a '1', the serial port goes into Transmit mode. It sends an ACK on the ninth bit and then holds SCL to '0' until the CPU responds by writing to I2CTRN. SCL is released by setting the SCLREL bit, and 8 bits of data are shifted out. Data bits are shifted out on the falling edge of SCL, such that SDA is valid during SCL high. The interrupt pulse is sent on the falling edge of the ninth clock pulse, regardless of the status of the ACK received from the master.

14.3.2 SLAVE RECEPTION

If the R_W bit received is a '0' during an address match, then Receive mode is initiated. Incoming bits are sampled on the rising edge of SCL. After 8 bits are received, if I2CRCV is not full or I2COV is not set, I2CRSR is transferred to I2CRCV. ACK is sent on the ninth clock.

If the RBF flag is set, indicating that I2CRCV is still holding data from a previous operation (RBF = 1), then ACK is not sent; however, the interrupt pulse is generated. In the case of an overflow, the contents of the I2CRSR are not loaded into the I2CRCV.

Note:	The I2CRCV is loaded if the I2COV bit = 1
	and the RBF flag = 0. In this case, a read
	of the I2CRCV was performed but the
	user did not clear the state of the I2COV
	bit before the next receive occurred. The
	acknowledgement is not sent ($\overline{ACK} = 1$)
	and the I2CRCV is updated.

14.4 I²C 10-Bit Slave Mode Operation

In 10-bit mode, the basic receive and transmit operations are the same as in the 7-bit mode. However, the criteria for address match is more complex.

The I^2C specification dictates that a slave must be addressed for a write operation with two address bytes following a Start bit.

The A10M bit is a control bit that signifies that the address in I2CADD is a 10-bit address rather than a 7-bit address. The address detection protocol for the first byte of a message address is identical for 7-bit and 10-bit messages, but the bits being compared are different.

I2CADD holds the entire 10-bit address. Upon receiving an address following a Start bit, I2CRSR <7:3> is compared against a literal '11110' (the default 10-bit address) and I2CRSR<2:1> are compared against I2CADD<9:8>. If a match occurs and if $R_W = 0$, the interrupt pulse is sent. The ADD10 bit is cleared to indicate a partial address match. If a match fails or $R_W = 1$, the ADD10 bit is cleared and the module returns to the Idle state.

The low byte of the address is then received and compared with I2CADD<7:0>. If an address match occurs, the interrupt pulse is generated and the ADD10 bit is set, indicating a complete 10-bit address match. If an address match did not occur, the ADD10 bit is cleared and the module returns to the Idle state.

14.4.1 10-BIT MODE SLAVE TRANSMISSION

Once a slave is addressed in this fashion with the full 10-bit address (we refer to this state as "PRIOR_ADDR_MATCH"), the master can begin sending data bytes for a slave reception operation.

TABLE 14-2: dsPIC30F3014/4013 I²C REGISTER MAP⁽¹⁾

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
I2CRCV	0200	_	_	_	—	—	_	_	_				Receive R	legister				0000 0000 0000 0000
I2CTRN	0202	_	_	_	—		_	_	_				Transmit F	Register				0000 0000 1111 1111
I2CBRG	0204	_	_	_	—		_	_				Baud F	Rate Genei	rator				0000 0000 0000 0000
I2CCON	0206	I2CEN	_	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	0001 0000 0000 0000
I2CSTAT	0208	ACKSTAT	TRSTAT	_	—		BCL	GCSTAT	ADD10	IWCOL	I2COV	D_A	Р	S	R_W	RBF	TBF	0000 0000 0000 0000
I2CADD	020A	_	_	_	_	_						Address F	Register					0000 0000 0000 0000

 Legend:
 — = unimplemented bit, read as '0'

 Note
 1:
 Refer to the "dsPIC30F Family Reference Manual" (DS70046) for descriptions of register bit fields.

16.3.4 TRANSMIT INTERRUPT

The transmit interrupt flag (U1TXIF or U2TXIF) is located in the corresponding interrupt flag register.

The transmitter generates an edge to set the UxTXIF bit. The condition for generating the interrupt depends on the UTXISEL control bit:

- a) If UTXISEL = 0, an interrupt is generated when a word is transferred from the transmit buffer to the Transmit Shift register (UxTSR). This means that the transmit buffer has at least one empty word.
- b) If UTXISEL = 1, an interrupt is generated when a word is transferred from the transmit buffer to the Transmit Shift register (UxTSR) and the transmit buffer is empty.

Switching between the two Interrupt modes during operation is possible and sometimes offers more flexibility.

16.3.5 TRANSMIT BREAK

Setting the UTXBRK bit (UxSTA<11>) causes the UxTX line to be driven to logic '0'. The UTXBRK bit overrides all transmission activity. Therefore, the user should generally wait for the transmitter to be Idle before setting UTXBRK.

To send a Break character, the UTXBRK bit must be set by software and must remain set for a minimum of 13 baud clock cycles. The UTXBRK bit is then cleared by software to generate Stop bits. The user must wait for a duration of at least one or two baud clock cycles in order to ensure a valid Stop bit(s) before reloading the UxTXB, or starting other transmitter activity. Transmission of a Break character does not generate a transmit interrupt.

16.4 Receiving Data

16.4.1 RECEIVING IN 8-BIT OR 9-BIT DATA MODE

The following steps must be performed while receiving 8-bit or 9-bit data:

- 1. Set up the UART (see Section 16.3.1 "Transmitting in 8-Bit Data Mode").
- 2. Enable the UART (see Section 16.3.1 "Transmitting in 8-Bit Data Mode").
- 3. A receive interrupt is generated when one or more data words have been received, depending on the receive interrupt settings specified by the URXISEL bits (UxSTA<7:6>).
- 4. Read the OERR bit to determine if an overrun error has occurred. The OERR bit must be reset in software.
- Read the received data from UxRXREG. The act of reading UxRXREG moves the next word to the top of the receive FIFO, and the PERR and FERR values are updated.

16.4.2 RECEIVE BUFFER (UXRXB)

The receive buffer is 4 words deep. Including the Receive Shift register (UxRSR), the user effectively has a 5-word deep FIFO buffer.

URXDA (UxSTA<0>) = 1 indicates that the receive buffer has data available. URXDA = 0 means that the buffer is empty. If a user attempts to read an empty buffer, the old values in the buffer are read and no data shift occurs within the FIFO.

The FIFO is reset during any device Reset. It is not affected when the device enters or wakes up from a power-saving mode.

16.4.3 RECEIVE INTERRUPT

The receive interrupt flag (U1RXIF or U2RXIF) can be read from the corresponding interrupt flag register. The interrupt flag is set by an edge generated by the receiver. The condition for setting the receive interrupt flag depends on the settings specified by the URXISEL<1:0> (UxSTA<7:6>) control bits.

- a) If URXISEL<1:0> = 00 or 01, an interrupt is generated every time a data word is transferred from the Receive Shift register (UxRSR) to the receive buffer. There may be one or more characters in the receive buffer.
- b) If URXISEL<1:0> = 10, an interrupt is generated when a word is transferred from the Receive Shift register (UxRSR) to the receive buffer, which as a result of the transfer, contains 3 characters.
- c) If URXISEL<1:0> = 11, an interrupt is set when a word is transferred from the Receive Shift register (UxRSR) to the receive buffer, which as a result of the transfer, contains 4 characters (i.e., becomes full).

Switching between the Interrupt modes during operation is possible, though generally not advisable during normal operation.

16.5 Reception Error Handling

16.5.1 RECEIVE BUFFER OVERRUN ERROR (OERR BIT)

The OERR bit (UxSTA<1>) is set if all of the following conditions occur:

- a) The receive buffer is full.
- b) The Receive Shift register is full, but unable to transfer the character to the receive buffer.
- c) The Stop bit of the character in the UxRSR is detected, indicating that the UxRSR needs to transfer the character to the buffer.

Once OERR is set, no further data is shifted in UxRSR (until the OERR bit is cleared in software or a Reset occurs). The data held in UxRSR and UxRXREG remains valid.

18.3 DCI Module Operation

18.3.1 MODULE ENABLE

The DCI module is enabled or disabled by setting/ clearing the DCIEN control bit in the DCICON1 SFR. Clearing the DCIEN control bit has the effect of resetting the module. In particular, all counters associated with CSCK generation, Frame Sync, and the DCI buffer control unit are reset.

The DCI clocks are shut down when the DCIEN bit is cleared.

When enabled, the DCI controls the data direction for the four I/O pins associated with the module. The port, LAT and TRIS register values for these I/O pins are overridden by the DCI module when the DCIEN bit is set.

It is also possible to override the CSCK pin separately when the bit clock generator is enabled. This permits the bit clock generator to operate without enabling the rest of the DCI module.

18.3.2 WORD-SIZE SELECTION BITS

The WS<3:0> word-size selection bits in the DCICON2 SFR determine the number of bits in each DCI data word. Essentially, the WS<3:0> bits determine the counting period for a 4-bit counter clocked from the CSCK signal.

Any data length, up to 16 bits, may be selected. The value loaded into the WS<3:0> bits is one less the desired word length. For example, a 16-bit data word size is selected when WS<3:0> = 1111.

Note:	These WS<3:0> control bits are used only
	in the Multichannel and I ² S modes. These
	bits have no effect in AC-Link mode since
	the data slot sizes are fixed by the protocol.

18.3.3 FRAME SYNC GENERATOR

The Frame Sync generator (COFSG) is a 4-bit counter that sets the frame length in data words. The Frame Sync generator is incremented each time the word-size counter is reset (refer to **Section 18.3.2** "**Word-Size Selection Bits**"). The period for the Frame Synchronization generator is set by writing the COFSG<3:0> control bits in the DCICON2 SFR. The COFSG period in clock cycles is determined by the following formula:

EQUATION 18-1: COFSG PERIOD

Frame Length = Word Length • (FSG Value + 1)

Frame lengths, up to 16 data words, may be selected. The frame length in CSCK periods can vary up to a maximum of 256 depending on the word size that is selected.

Note:	The COFSG control bits have no effect in
	AC-Link mode since the frame length is
	set to 256 CSCK periods by the protocol.

18.3.4 FRAME SYNC MODE CONTROL BITS

The type of Frame Sync signal is selected using the Frame Synchronization mode control bits (COFSM<1:0>) in the DCICON1 SFR. The following operating modes can be selected:

- Multichannel mode
- I²S mode
- AC-Link mode (16-bit)
- AC-Link mode (20-bit)

The operation of the COFSM control bits depends on whether the DCI module generates the Frame Sync signal as a master device, or receives the Frame Sync signal as a slave device.

The master device in a DSP/Codec pair is the device that generates the Frame Sync signal. The Frame Sync signal initiates data transfers on the CSDI and CSDO pins and usually has the same frequency as the data sample rate (COFS).

The DCI module is a Frame Sync master if the COFSD control bit is cleared and is a Frame Sync slave if the COFSD control bit is set.

18.3.5 MASTER FRAME SYNC OPERATION

When the DCI module is operating as a Frame Sync master device (COFSD = 0), the COFSM mode bits determine the type of Frame Sync pulse that is generated by the Frame Sync generator logic.

A new COFS signal is generated when the Frame Sync generator resets to '0'.

In the Multichannel mode, the Frame Sync pulse is driven high for the CSCK period to initiate a data transfer. The number of CSCK cycles between successive Frame Sync pulses depends on the word size and Frame Sync generator control bits. A timing diagram for the Frame Sync signal in Multichannel mode is shown in Figure 18-2.

In the AC-Link mode of operation, the Frame Sync signal has a fixed period and duty cycle. The AC-Link Frame Sync signal is high for 16 CSCK cycles and is low for 240 CSCK cycles. A timing diagram with the timing details at the start of an AC-Link frame is shown in Figure 18-3.

In the I^2S mode, a Frame Sync signal having a 50% duty cycle is generated. The period of the I^2S Frame Sync signal in CSCK cycles is determined by the word

20.2.7 FAIL-SAFE CLOCK MONITOR

The Fail-Safe Clock Monitor (FSCM) allows the device to continue to operate even in the event of an oscillator failure. The FSCM function is enabled by appropriately programming the FCKSM Configuration bits (clock switch and monitor selection bits) in the FOSC Device Configuration register. If the FSCM function is enabled, the LPRC internal oscillator runs at all times (except during Sleep mode) and is not subject to control by the SWDTEN bit.

In the event of an oscillator failure, the FSCM generates a clock failure trap event and switches the system clock over to the FRC oscillator. The user then has the option to either attempt to restart the oscillator or execute a controlled shutdown. The user may decide to treat the trap as a warm Reset by simply loading the Reset address into the oscillator fail trap vector. In this event, the CF (Clock Fail) status bit (OSCCON<3>) is also set whenever a clock failure is recognized.

In the event of a clock failure, the WDT is unaffected and continues to run on the LPRC clock.

If the oscillator has a very slow start-up time coming out of POR, BOR or Sleep, it is possible that the PWRT timer will expire before the oscillator has started. In such cases, the FSCM is activated and the FSCM initiates a clock failure trap, and the COSC<2:0> bits are loaded with FRC oscillator selection. This effectively shuts off the original oscillator that was trying to start.

The user may detect this situation and restart the oscillator in the clock fail trap ISR.

Upon a clock failure detection, the FSCM module initiates a clock switch to the FRC oscillator as follows:

- 1. The COSC bits (OSCCON<14:12>) are loaded with the FRC oscillator selection value.
- 2. CF bit is set (OSCCON<3>).
- 3. OSWEN control bit (OSCCON<0>) is cleared.

For the purpose of clock switching, the clock sources are sectioned into four groups:

- Primary
- Secondary
- Internal FRC
- Internal LPRC

The user can switch between these functional groups but cannot switch between options within a group. If the primary group is selected, then the choice within the group is always determined by the FPR<4:0> Configuration bits.

The OSCCON register holds the control and status bits related to clock switching.

• COSC<2:0>: Read-only status bits always reflect the current oscillator group in effect.

- NOSC<2:0>: Control bits which are written to indicate the new oscillator group of choice.
 - On POR and BOR, COSC<2:0> and NOSC<2:0> are both loaded with the Configuration bit values, FOS<2:0>.
- LOCK: The LOCK status bit indicates a PLL lock.
- CF: Read-only status bit indicating if a clock fail detect has occurred.
- OSWEN: Control bit changes from a '0' to a '1' when a clock transition sequence is initiated. Clearing the OSWEN control bit aborts a clock transition in progress (used for hang-up situations).

If Configuration bits, FCKSM<1:0> = 1x, then the clock switching and Fail-Safe Clock Monitor functions are disabled. This is the default Configuration bit setting.

If clock switching is disabled, then the FOS<2:0> and FPR<4:0> bits directly control the oscillator selection and the COSC<2:0> bits do not control the clock selection. However, these bits reflect the clock source selection.

Note: The application should not attempt to switch to a clock of frequency lower than 100 kHz when the Fail-Safe Clock Monitor is enabled. If such clock switching is performed, the device may generate an oscillator fail trap and switch to the Fast RC oscillator.

20.2.8 PROTECTION AGAINST ACCIDENTAL WRITES TO OSCCON

A write to the OSCCON register is intentionally made difficult because it controls clock switching and clock scaling.

To write to the OSCCON low byte, the following code sequence must be executed without any other instructions in between:

Byte Write 0x46 to OSCCON low Byte Write 0x57 to OSCCON low

Byte write is allowed for one instruction cycle. Write the desired value or use bit manipulation instruction.

To write to the OSCCON high byte, the following instructions must be executed without any other instructions in between:

Byte Write 0x78 to OSCCON high Byte Write 0x9A to OSCCON high

Byte write is allowed for one instruction cycle. Write the desired value or use bit manipulation instruction.

Field	Description
Wb	Base W register ∈ {W0W15}
Wd	Destination W register ∈ { Wd, [Wd], [Wd++], [Wd], [++Wd], [Wd] }
Wdo	Destination W register ∈ { Wnd, [Wnd], [Wnd++], [Wnd], [++Wnd], [Wnd], [Wnd+Wb] }
Wm,Wn	Dividend, Divisor Working register pair (direct addressing)
Wm*Wm	Multiplicand and Multiplier working register pair for Square instructions \in {W4*W4,W5*W5,W6*W6,W7*W7}
Wm*Wn	Multiplicand and Multiplier working register pair for DSP instructions ∈ {W4*W5,W4*W6,W4*W7,W5*W6,W5*W7,W6*W7}
Wn	One of 16 working registers ∈ {W0W15}
Wnd	One of 16 destination working registers ∈ {W0W15}
Wns	One of 16 source working registers ∈ {W0W15}
WREG	W0 (working register used in file register instructions)
Ws	Source W register ∈ { Ws, [Ws], [Ws++], [Ws], [++Ws], [Ws] }
Wso	Source W register ∈ { Wns, [Wns], [Wns++], [Wns], [++Wns], [Wns], [Wns+Wb] }
Wx	X data space prefetch address register for DSP instructions ∈ {[W8]+=6, [W8]+=4, [W8]+=2, [W8], [W8]-=6, [W8]-=4, [W8]-=2, [W9]+=6, [W9]+=4, [W9]+=2, [W9], [W9]-=6, [W9]-=4, [W9]-=2, [W9+W12],none}
Wxd	X data space prefetch destination register for DSP instructions \in {W4W7}
Wy	Y data space prefetch address register for DSP instructions ∈ {[W10]+=6, [W10]+=4, [W10]+=2, [W10], [W10]-=6, [W10]-=4, [W10]-=2, [W11]+=6, [W11]+=4, [W11]+=2, [W11], [W11]-=6, [W11]-=4, [W11]-=2, [W11+W12], none}
Wyd	Y data space prefetch destination register for DSP instructions \in {W4W7}

TABLE 21-1: SYMBOLS USED IN OPCODE DESCRIPTIONS (CONTINUED)

TABLE 21-2: INSTRUCTION SET OVERVIEW

Base Instr #	Assembly Mnemoni c		Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
1	ADD	ADD	Acc	Add Accumulators	1	1	OA,OB,SA,SB
		ADD	f	f = f + WREG	1	1	C,DC,N,OV,Z
		ADD	f,WREG	WREG = f + WREG	1	1	C,DC,N,OV,Z
		ADD	#lit10,Wn	Wd = lit10 + Wd	1	1	C,DC,N,OV,Z
		ADD	Wb,Ws,Wd	Wd = Wb + Ws	1	1	C,DC,N,OV,Z
		ADD	Wb,#lit5,Wd	Wd = Wb + lit5	1	1	C,DC,N,OV,Z
		ADD	Wso,#Slit4,Acc	16-bit Signed Add to Accumulator	1	1	OA,OB,SA,SB
2	ADDC	ADDC	f	f = f + WREG + (C)	1	1	C,DC,N,OV,Z
		ADDC	f,WREG	WREG = f + WREG + (C)	1	1	C,DC,N,OV,Z
		ADDC	#lit10,Wn	Wd = lit10 + Wd + (C)	1	1	C,DC,N,OV,Z
		ADDC	Wb,Ws,Wd	Wd = Wb + Ws + (C)	1	1	C,DC,N,OV,Z
		ADDC	Wb,#lit5,Wd	Wd = Wb + lit5 + (C)	1	1	C,DC,N,OV,Z
3	AND	AND	f	f = f .AND. WREG	1	1	N,Z
		AND	f,WREG	WREG = f .AND. WREG	1	1	N,Z
		AND	#lit10,Wn	Wd = lit10 .AND. Wd	1	1	N,Z
		AND	Wb,Ws,Wd	Wd = Wb .AND. Ws	1	1	N,Z
		AND	Wb,#lit5,Wd	Wd = Wb .AND. lit5	1	1	N,Z
4	ASR	ASR	f	f = Arithmetic Right Shift f	1	1	C,N,OV,Z
		ASR	f,WREG	WREG = Arithmetic Right Shift f	1	1	C,N,OV,Z
		ASR	Ws,Wd	Wd = Arithmetic Right Shift Ws	1	1	C,N,OV,Z
		ASR	Wb,Wns,Wnd	Wnd = Arithmetic Right Shift Wb by Wns	1	1	N,Z
		ASR	Wb,#lit5,Wnd	Wnd = Arithmetic Right Shift Wb by lit5	1	1	N,Z
5	BCLR	BCLR	f,#bit4	Bit Clear f	1	1	None
		BCLR	Ws,#bit4	Bit Clear Ws	1	1	None
6	BRA	BRA	C,Expr	Branch if Carry	1	1 (2)	None
		BRA	GE, Expr	Branch if Greater than or Equal	1	1 (2)	None
		BRA	GEU,Expr	Branch if Unsigned Greater than or Equal	1	1 (2)	None
		BRA	GT,Expr	Branch if Greater than	1	1 (2)	None
		BRA	GTU, Expr	Branch if Unsigned Greater than	1	1 (2)	None
		BRA	LE,Expr	Branch if Less than or Equal	1	1 (2)	None
		BRA	LEU,Expr	Branch if Unsigned Less than or Equal	1	1 (2)	None
		BRA	LT,Expr	Branch if Less than	1	1 (2)	None
		BRA	LTU,Expr	Branch if Unsigned Less than	1	1 (2)	None
		BRA	N,Expr	Branch if Negative	1	1 (2)	None
		BRA	NC, Expr	Branch if Not Carry	1	1 (2)	None
		BRA	NN, Expr	Branch if Not Negative	1	1 (2)	None
		BRA	NOV, Expr	Branch if Not Overflow	1	1 (2)	None
		BRA	NZ,Expr	Branch if Not Zero	1	1 (2)	None
		BRA	OA,Expr	Branch if Accumulator A Overflow	1	1 (2)	None
		BRA	OB,Expr	Branch if Accumulator B Overflow	1	1 (2)	None
		BRA	OV,Expr	Branch if Overflow	1	1 (2)	None
		BRA	SA,Expr	Branch if Accumulator A Saturated	1	1 (2)	None
		BRA	SB,Expr	Branch if Accumulator B Saturated	1	1 (2)	None
		BRA	Expr	Branch Unconditionally	1	2	None
		BRA	Z,Expr	Branch if Zero	1	1 (2)	None
		BRA	Wn	Computed Branch	1	2	None
7	BSET	BSET	f,#bit4	Bit Set f	1	1	None
		BSET	Ws,#bit4	Bit Set Ws	1	1	None
8	BSW	BSW.C	Ws,Wb	Write C bit to Ws <wb></wb>	1	1	None
		BSW.Z	Ws,Wb	Write Z bit to Ws <wb></wb>	1	1	None

TABLE 23-20: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER AND BROWN-OUT RESET TIMING REQUIREMENTS

AC CHA	RACTER	ISTICS	$\begin{tabular}{lllllllllllllllllllllllllllllllllll$								
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Тур ⁽²⁾	Мах	Units	Conditions				
SY10	TmcL	MCLR Pulse Width (low)	2	—	_	μS	-40°C to +85°C				
SY11	TPWRT	Power-up Timer Period	2 10 43	4 16 64	8 32 128	ms	-40°C to +85°C, VDD = 5V User programmable				
SY12	TPOR	Power-on Reset Delay	3	10	30	μS	-40°C to +85°C				
SY13	Tioz	I/O High-Impedance from MCLR Low or Watchdog Timer Reset		0.8	1.0	μS					
SY20	Twdt1 Twdt2 Twdt3	Watchdog Timer Time-out Period (no prescaler)	1.1 1.2 1.3	2.0 2.0 2.0	6.6 5.0 4.0	ms ms ms	VDD = 2.5V VDD = 3.3V, ±10% VDD = 5V, ±10%				
SY25	TBOR	Brown-out Reset Pulse Width ⁽³⁾	100	—		μS	$VDD \le VBOR (D034)$				
SY30	Tost	Oscillator Start-up Timer Period		1024 Tosc		_	Tosc = OSC1 period				
SY35	TFSCM	Fail-Safe Clock Monitor Delay	_	500	900	μS	-40°C to +85°C				

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ" column is at 5V, 25°C unless otherwise stated.

3: Refer to Figure 23-2 and Table 23-11 for BOR.

FIGURE 23-7: BAND GAP START-UP TIME CHARACTERISTICS



TABLE 23-21: BAND GAP START-UP TIME REQUIREMENTS

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 2.5V to 5.5V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^\circ C \leq TA \leq +85^\circ C \mbox{ for Industrial} \\ & -40^\circ C \leq TA \leq +125^\circ C \mbox{ for Extended} \end{array}$					
Param No.	Symbol	Characteristic ⁽¹⁾	Min	Typ ⁽²⁾	Max	Units	Conditions	
SY40	Tbgap	Band Gap Start-up Time		40	65	μS	Defined as the time between the instant that the band gap is enabled and the moment that the band gap reference voltage is stable (RCON<13> status bit)	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ" column is at 5V, 25°C unless otherwise stated.





44-Lead Plastic Quad Flat, No Lead Package (ML) – 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS					
Dimension	MIN	NOM	MAX			
Contact Pitch	E		0.65 BSC			
Optional Center Pad Width	W2			6.80		
Optional Center Pad Length	T2			6.80		
Contact Pad Spacing	C1		8.00			
Contact Pad Spacing	C2		8.00			
Contact Pad Width (X44)	X1			0.35		
Contact Pad Length (X44)	Y1			0.80		
Distance Between Pads	G	0.25				

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2103A