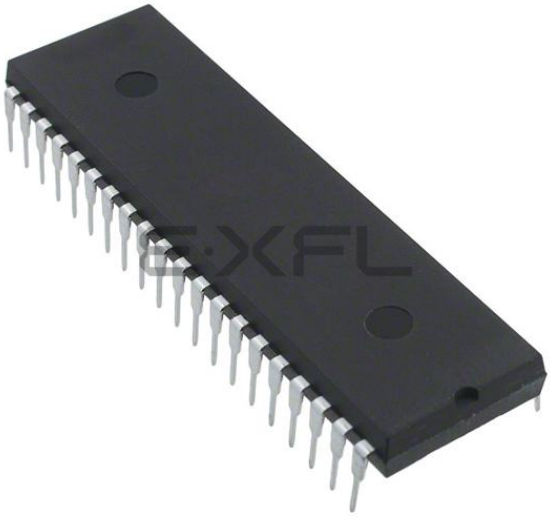

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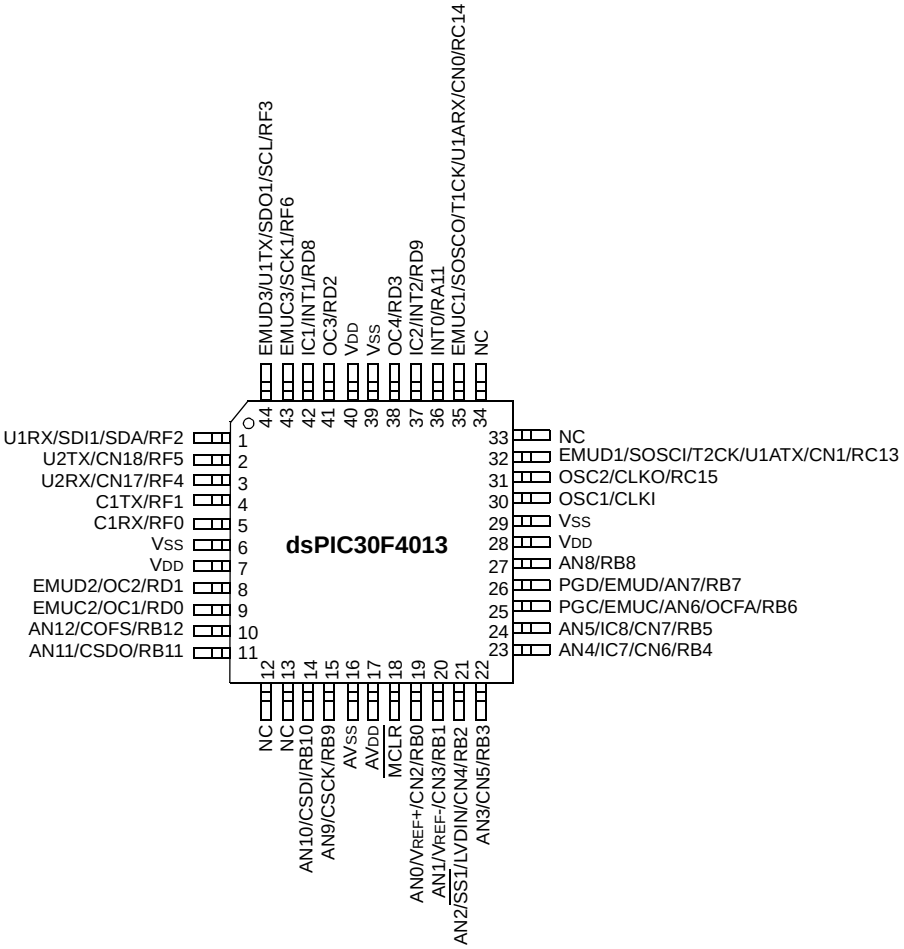
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	20 MIPS
Connectivity	CANbus, I²C, SPI, UART/USART
Peripherals	AC'97, Brown-out Detect/Reset, I²S, POR, PWM, WDT
Number of I/O	30
Program Memory Size	48KB (16K x 24)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 13x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic30f4013-20e-p

Pin Diagrams (Continued)

44-Pin TQFP



2.3 Divide Support

The dsPIC DSC devices feature a 16/16-bit signed fractional divide operation, as well as 32/16-bit and 16/16-bit signed and unsigned integer divide operations, in the form of single instruction iterative divides. The following instructions and data sizes are supported:

1. DIVF – 16/16 signed fractional divide
2. DIV.sd – 32/16 signed divide
3. DIV.ud – 32/16 unsigned divide
4. DIV.s – 16/16 signed divide
5. DIV.u – 16/16 unsigned divide

The 16/16 divides are similar to the 32/16 (same number of iterations), but the dividend is either zero-extended or sign-extended during the first iteration.

The divide instructions must be executed within a REPEAT loop. Any other form of execution (e.g., a series of discrete divide instructions) will not function correctly because the instruction flow depends on RCOUNT. The divide instruction does not automatically set up the RCOUNT value and it must, therefore, be explicitly and correctly specified in the REPEAT instruction, as shown in Table 2-1 (REPEAT will execute the target instruction {operand value+1} times). The REPEAT loop count must be setup for 18 iterations of the DIV/DIVF instruction. Thus, a complete divide operation requires 19 cycles.

Note:	The divide flow is interruptible. However, the user needs to save the context as appropriate.

TABLE 2-1: DIVIDE INSTRUCTIONS

Instruction	Function
DIVF	Signed fractional divide: Wm/Wn → W0; Rem → W1
DIV.sd	Signed divide: (Wm+1:Wm)/Wn → W0; Rem → W1
DIV.s	Signed divide: Wm/Wn → W0; Rem → W1
DIV.ud	Unsigned divide: (Wm+1:Wm)/Wn → W0; Rem → W1
DIV.u	Unsigned divide: Wm/Wn → W0; Rem → W1

5.4 RTSP Operation

The dsPIC30F Flash program memory is organized into rows and panels. Each row consists of 32 instructions or 96 bytes. Each panel consists of 128 rows or 4K x 24 instructions. RTSP allows the user to erase one row (32 instructions) at a time and to program four instructions at one time. RTSP may be used to program multiple program memory panels, but the Table Pointer must be changed at each panel boundary.

Each panel of program memory contains write latches that hold 32 instructions of programming data. Prior to the actual programming operation, the write data must be loaded into the panel write latches. The data to be programmed into the panel is loaded in sequential order into the write latches; instruction 0, instruction 1, etc. The instruction words loaded must always be from a 32 address boundary.

The basic sequence for RTSP programming is to set up a Table Pointer, then do a series of TBLWT instructions to load the write latches. Programming is performed by setting the special bits in the NVMCON register. 32 TBLWTL and four TBLWTH instructions are required to load the 32 instructions. If multiple panel programming is required, the Table Pointer needs to be changed and the next set of multiple write latches written.

All of the table write operations are single-word writes (2 instruction cycles), because only the table latches are written. A programming cycle is required for programming each row.

The Flash program memory is readable, writable and erasable during normal operation over the entire VDD range.

5.5 Control Registers

The four SFRs used to read and write the program Flash memory are:

- NVMCON
- NVMADR
- NVMADRU
- NVMKEY

5.5.1 NVMCON REGISTER

The NVMCON register controls which blocks are to be erased, which memory type is to be programmed and the start of the programming cycle.

5.5.2 NVMADR REGISTER

The NVMADR register is used to hold the lower two bytes of the Effective Address. The NVMADR register captures the EA<15:0> of the last table instruction that has been executed and selects the row to write.

5.5.3 NVMADRU REGISTER

The NVMADRU register is used to hold the upper byte of the Effective Address. The NVMADRU register captures the EA<23:16> of the last table instruction that has been executed.

5.5.4 NVMKEY REGISTER

NVMKEY is a write-only register that is used for write protection. To start a programming or erase sequence, the user must consecutively write 0x55 and 0xAA to the NVMKEY register. Refer to **Section 5.6 “Programming Operations”** for further details.

Note:	The user can also directly write to the NVMADR and NVMADRU registers to specify a program memory address for erasing or programming.

TABLE 9-1: dsPIC30F3014/4013 TIMER1 REGISTER MAP(1)

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
TMR1	0100	Timer1 Register																uuuu uuuu uuuu uuuu
PR1	0102	Period Register 1																1111 1111 1111 1111
T1CON	0104	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	—	TSYNC	TCS	—	0000 0000 0000 0000

Legend: u = uninitialized bit; — = unimplemented bit, read as '0'

Note 1: Refer to the *"dsPIC30F Family Reference Manual*" (DS70046) for descriptions of register bit fields.

10.0 TIMER2/3 MODULE

Note:	This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the "*dsPIC30F Family Reference Manual*" (DS70046).

This section describes the 32-bit general purpose timer module (Timer2/3) and associated operational modes. Figure 10-1 depicts the simplified block diagram of the 32-bit Timer2/3 module. Figure 10-2 and Figure 10-3 show Timer2/3 configured as two independent 16-bit timers, Timer2 and Timer3, respectively.

The Timer2/3 module is a 32-bit timer (which can be configured as two 16-bit timers) with selectable operating modes. These timers are utilized by other peripheral modules, such as:

- Input Capture
- Output Compare/Simple PWM

The following sections provide a detailed description, including setup and control registers, along with associated block diagrams for the operational modes of the timers.

The 32-bit timer has the following modes:

- Two independent 16-bit timers (Timer2 and Timer3) with all 16-bit operating modes (except Asynchronous Counter mode)
- Single 32-bit timer operation
- Single 32-bit synchronous counter

Further, the following operational characteristics are supported:

- ADC event trigger
- Timer gate operation
- Selectable prescaler settings
- Timer operation during Idle and Sleep modes
- Interrupt on a 32-bit Period register match

These operating modes are determined by setting the appropriate bit(s) in the 16-bit T2CON and T3CON SFRs.

For 32-bit timer/counter operation, Timer2 is the lsw and Timer3 is the msw of the 32-bit timer.

Note:	For 32-bit timer operation, T3CON control bits are ignored. Only T2CON control bits are used for setup and control. Timer2 clock and gate inputs are utilized for the 32-bit timer module, but an interrupt is generated with the Timer3 Interrupt Flag (T3IF) and the interrupt is enabled with the Timer3 interrupt enable bit (T3IE).

16-Bit Timer Mode: In the 16-bit mode, Timer2 and Timer3 can be configured as two independent 16-bit timers. Each timer can be set up in either 16-bit Timer mode or 16-bit Synchronous Counter mode. See **Section 9.0 "Timer1 Module"** for details on these two operating modes.

The only functional difference between Timer2 and Timer3 is that Timer2 provides synchronization of the clock prescaler output. This is useful for high-frequency external clock inputs.

32-Bit Timer Mode: In the 32-Bit Timer mode, the timer increments on every instruction cycle, up to a match value preloaded into the combined 32-bit Period register, PR3/PR2, then resets to '0' and continues to count.

For synchronous 32-bit reads of the Timer2/Timer3 pair, reading the lsw (TMR2 register) causes the msw to be read and latched into a 16-bit holding register, termed TMR3HLD.

For synchronous 32-bit writes, the holding register (TMR3HLD) must first be written to. When followed by a write to the TMR2 register, the contents of TMR3HLD is transferred and latched into the MSB of the 32-bit timer (TMR3).

32-Bit Synchronous Counter Mode: In the 32-Bit Synchronous Counter mode, the timer increments on the rising edge of the applied external clock signal which is synchronized with the internal phase clocks. The timer counts up to a match value preloaded in the combined 32-bit Period register, PR3/PR2, then resets to '0' and continues.

When the timer is configured for the Synchronous Counter mode of operation and the CPU goes into the Idle mode, the timer stops incrementing unless the TSIDL (T2CON<13>) bit = 0. If TSIDL = 1, the timer module logic resumes the incrementing sequence upon termination of the CPU Idle mode.

TABLE 10-1: dsPIC30F3014/4013 TIMER2/3 REGISTER MAP(1)

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
TMR2	0106	Timer2 Register																uuuu uuuu uuuu uuuu
TMR3HLD	0108	Timer3 Holding Register (for 32-bit timer operations only)																uuuu uuuu uuuu uuuu
TMR3	010A	Timer3 Register																uuuu uuuu uuuu uuuu
PR2	010C	Period Register 2																1111 1111 1111 1111
PR3	010E	Period Register 3																1111 1111 1111 1111
T2CON	0110	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	T32	—	TCS	—	0000 0000 0000 0000
T3CON	0112	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	—	—	TCS	—	0000 0000 0000 0000

Legend: u = uninitialized bit; — = unimplemented bit, read as '0'

Note 1: Refer to the *"dsPIC30F Family Reference Manual*" (DS70046) for descriptions of register bit fields.

12.0 INPUT CAPTURE MODULE

Note: This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the "*dsPIC30F Family Reference Manual*" (DS70046).

This section describes the input capture module and associated operational modes. The features provided by this module are useful in applications requiring frequency (period) and pulse measurement. Figure 12-1 depicts a block diagram of the input capture module. Input capture is useful for such modes as:

- Frequency/Period/Pulse Measurements
- Additional Sources of External Interrupts

The key operational features of the input capture module are:

- Simple Capture Event mode
- Timer2 and Timer3 mode selection
- Interrupt on input capture event

These operating modes are determined by setting the appropriate bits in the ICxCON register (where x = 1,2,...,N). The dsPIC DSC devices contain up to 8 capture channels (i.e., the maximum value of N is 8). The dsPIC30F3014 device contains 2 capture channels while the dsPIC30F4013 device contains 4 capture channels.

12.1 Simple Capture Event Mode

The simple capture events in the dsPIC30F product family are:

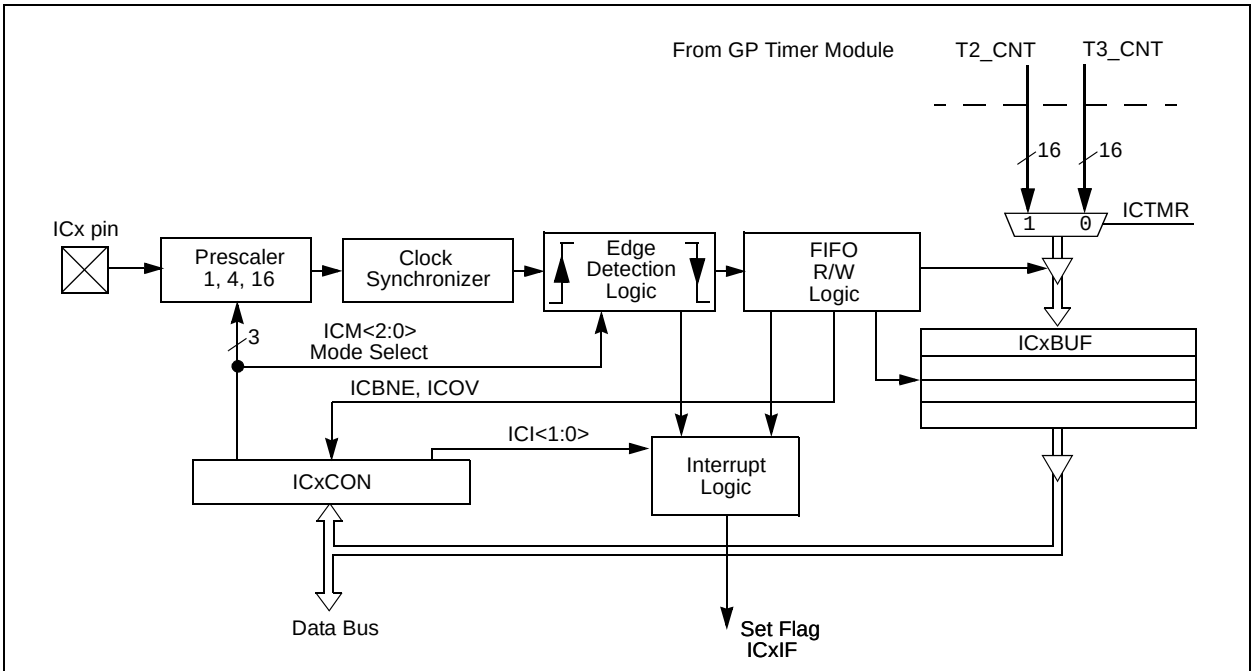
- Capture every falling edge
- Capture every rising edge
- Capture every 4th rising edge
- Capture every 16th rising edge
- Capture every rising and falling edge

These simple Input Capture modes are configured by setting the appropriate bits, ICM<2:0> (ICxCON<2:0>).

12.1.1 CAPTURE PRESCALER

There are four input capture prescaler settings specified by bits, ICM<2:0> (ICxCON<2:0>). Whenever the capture channel is turned off, the prescaler counter is cleared. In addition, any Reset clears the prescaler counter.

FIGURE 12-1: INPUT CAPTURE MODE BLOCK DIAGRAM



Note: Where 'x' is shown, reference is made to the registers or bits associated to the respective input capture channels, 1 through N.

NOTES:

14.7 Interrupts

The I²C module generates two interrupt flags, MI2CIF (I²C Master Interrupt Flag) and SI2CIF (I²C Slave Interrupt Flag). The MI2CIF interrupt flag is activated on completion of a master message event. The SI2CIF interrupt flag is activated on detection of a message directed to the slave.

14.8 Slope Control

The I²C standard requires slope control on the SDA and SCL signals for Fast mode (400 kHz). The control bit, DISSLW, enables the user to disable slew rate control if desired. It is necessary to disable the slew rate control for 1 MHz mode.

14.9 IPMI Support

The control bit, IPMIEN, enables the module to support Intelligent Peripheral Management Interface (IPMI). When this bit is set, the module accepts and acts upon all addresses.

14.10 General Call Address Support

The general call address can address all devices. When this address is used, all devices should, in theory, respond with an Acknowledgement.

The general call address is one of eight addresses reserved for specific purposes by the I²C protocol. It consists of all '0's with R_W = 0.

The general call address is recognized when the General Call Enable (GCEN) bit is set (I2CCON<7> = 1). Following a Start bit detection, 8 bits are shifted into I2CRSR and the address is compared with I2CADD, and is also compared with the general call address which is fixed in hardware.

If a general call address match occurs, the I2CRSR is transferred to the I2CRCV after the eighth clock, the RBF flag is set and on the falling edge of the ninth bit ($\overline{ACK}$ bit), the Master Event Interrupt Flag (MI2CIF) is set.

When the interrupt is serviced, the source for the interrupt can be checked by reading the contents of the I2CRCV to determine if the address was device-specific or a general call address.

14.11 I²C Master Support

As a master device, six operations are supported:

- Assert a Start condition on SDA and SCL.
- Assert a Restart condition on SDA and SCL.
- Write to the I2CTRN register initiating transmission of data/address.
- Generate a Stop condition on SDA and SCL.
- Configure the I²C port to receive data.
- Generate an $\overline{ACK}$ condition at the end of a received byte of data.

14.12 I²C Master Operation

The master device generates all of the serial clock pulses and the Start and Stop conditions. A transfer is ended with a Stop condition or with a Repeated Start condition. Since the Repeated Start condition is also the beginning of the next serial transfer, the I²C bus is not released.

In Master Transmitter mode, serial data is output through SDA, while SCL outputs the serial clock. The first byte transmitted contains the slave address of the receiving device (7 bits) and the data direction bit. In this case, the data direction bit (R_W) is logic '0'. Serial data is transmitted 8 bits at a time. After each byte is transmitted, an $\overline{ACK}$ bit is received. Start and Stop conditions are output to indicate the beginning and the end of a serial transfer.

In Master Receive mode, the first byte transmitted contains the slave address of the transmitting device (7 bits) and the data direction bit. In this case, the data direction bit (R_W) is logic '1'. Thus, the first byte transmitted is a 7-bit slave address, followed by a '1' to indicate the receive bit. Serial data is received via SDA while SCL outputs the serial clock. Serial data is received 8 bits at a time. After each byte is received, an $\overline{ACK}$ bit is transmitted. Start and Stop conditions indicate the beginning and end of transmission.

14.12.1 I²C MASTER TRANSMISSION

Transmission of a data byte, a 7-bit address or the second half of a 10-bit address, is accomplished by simply writing a value to I2CTRN register. The user should only write to I2CTRN when the module is in a Wait state. This action sets the Buffer Full Flag (TBF) and allow the Baud Rate Generator to begin counting and start the next transmission. Each bit of address/data is shifted out onto the SDA pin after the falling edge of SCL is asserted. The Transmit Status Flag, TRSTAT (I2CSTAT<14>), indicates that a master transmit is in progress.

16.3.4 TRANSMIT INTERRUPT

The transmit interrupt flag (U1TXIF or U2TXIF) is located in the corresponding interrupt flag register.

The transmitter generates an edge to set the UxTXIF bit. The condition for generating the interrupt depends on the UTXISEL control bit:

a) If UTXISEL = 0, an interrupt is generated when a word is transferred from the transmit buffer to the Transmit Shift register (UxTSR). This means that the transmit buffer has at least one empty word.

b) If UTXISEL = 1, an interrupt is generated when a word is transferred from the transmit buffer to the Transmit Shift register (UxTSR) and the transmit buffer is empty.

Switching between the two Interrupt modes during operation is possible and sometimes offers more flexibility.

16.3.5 TRANSMIT BREAK

Setting the UTXBRK bit (UxSTA<11>) causes the UxTX line to be driven to logic '0'. The UTXBRK bit overrides all transmission activity. Therefore, the user should generally wait for the transmitter to be Idle before setting UTXBRK.

To send a Break character, the UTXBRK bit must be set by software and must remain set for a minimum of 13 baud clock cycles. The UTXBRK bit is then cleared by software to generate Stop bits. The user must wait for a duration of at least one or two baud clock cycles in order to ensure a valid Stop bit(s) before reloading the UxTXB, or starting other transmitter activity. Transmission of a Break character does not generate a transmit interrupt.

16.4 Receiving Data

16.4.1 RECEIVING IN 8-BIT OR 9-BIT DATA MODE

The following steps must be performed while receiving 8-bit or 9-bit data:

1. Set up the UART (see **Section 16.3.1 "Transmitting in 8-Bit Data Mode"**).
2. Enable the UART (see **Section 16.3.1 "Transmitting in 8-Bit Data Mode"**).
3. A receive interrupt is generated when one or more data words have been received, depending on the receive interrupt settings specified by the URXISEL bits (UxSTA<7:6>).
4. Read the OERR bit to determine if an overrun error has occurred. The OERR bit must be reset in software.
5. Read the received data from UxRXREG. The act of reading UxRXREG moves the next word to the top of the receive FIFO, and the PERR and FERR values are updated.

16.4.2 RECEIVE BUFFER (UxRXB)

The receive buffer is 4 words deep. Including the Receive Shift register (UxRSR), the user effectively has a 5-word deep FIFO buffer.

URXDA (UxSTA<0>) = 1 indicates that the receive buffer has data available. URXDA = 0 means that the buffer is empty. If a user attempts to read an empty buffer, the old values in the buffer are read and no data shift occurs within the FIFO.

The FIFO is reset during any device Reset. It is not affected when the device enters or wakes up from a power-saving mode.

16.4.3 RECEIVE INTERRUPT

The receive interrupt flag (U1RXIF or U2RXIF) can be read from the corresponding interrupt flag register. The interrupt flag is set by an edge generated by the receiver. The condition for setting the receive interrupt flag depends on the settings specified by the URXISEL<1:0> (UxSTA<7:6>) control bits.

a) If URXISEL<1:0> = 00 or 01, an interrupt is generated every time a data word is transferred from the Receive Shift register (UxRSR) to the receive buffer. There may be one or more characters in the receive buffer.

b) If URXISEL<1:0> = 10, an interrupt is generated when a word is transferred from the Receive Shift register (UxRSR) to the receive buffer, which as a result of the transfer, contains 3 characters.

c) If URXISEL<1:0> = 11, an interrupt is set when a word is transferred from the Receive Shift register (UxRSR) to the receive buffer, which as a result of the transfer, contains 4 characters (i.e., becomes full).

Switching between the Interrupt modes during operation is possible, though generally not advisable during normal operation.

16.5 Reception Error Handling

16.5.1 RECEIVE BUFFER OVERRUN ERROR (OERR BIT)

The OERR bit (UxSTA<1>) is set if all of the following conditions occur:

a) The receive buffer is full.

b) The Receive Shift register is full, but unable to transfer the character to the receive buffer.

c) The Stop bit of the character in the UxRSR is detected, indicating that the UxRSR needs to transfer the character to the buffer.

Once OERR is set, no further data is shifted in UxRSR (until the OERR bit is cleared in software or a Reset occurs). The data held in UxRSR and UxRXREG remains valid.

TABLE 16-1: dsPIC30F3014/4013 UART1 REGISTER MAP(1)

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
U1MODE	020C	UARTEN	—	USIDL	—	—	ALTIO	—	—	WAKE	LPBACK	ABAUD	—	—	PDSEL1	PDSEL0	STSEL	0000 0000 0000 0000
U1STA	020E	UTXISEL	—	—	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0000 0001 0001 0000
U1TXREG	0210	—	—	—	—	—	—	—	UTX8	Transmit Register								0000 000u uuuu uuuu
U1RXREG	0212	—	—	—	—	—	—	—	URX8	Receive Register								0000 0000 0000 0000
U1BRG	0214	Baud Rate Generator Prescaler																0000 0000 0000 0000

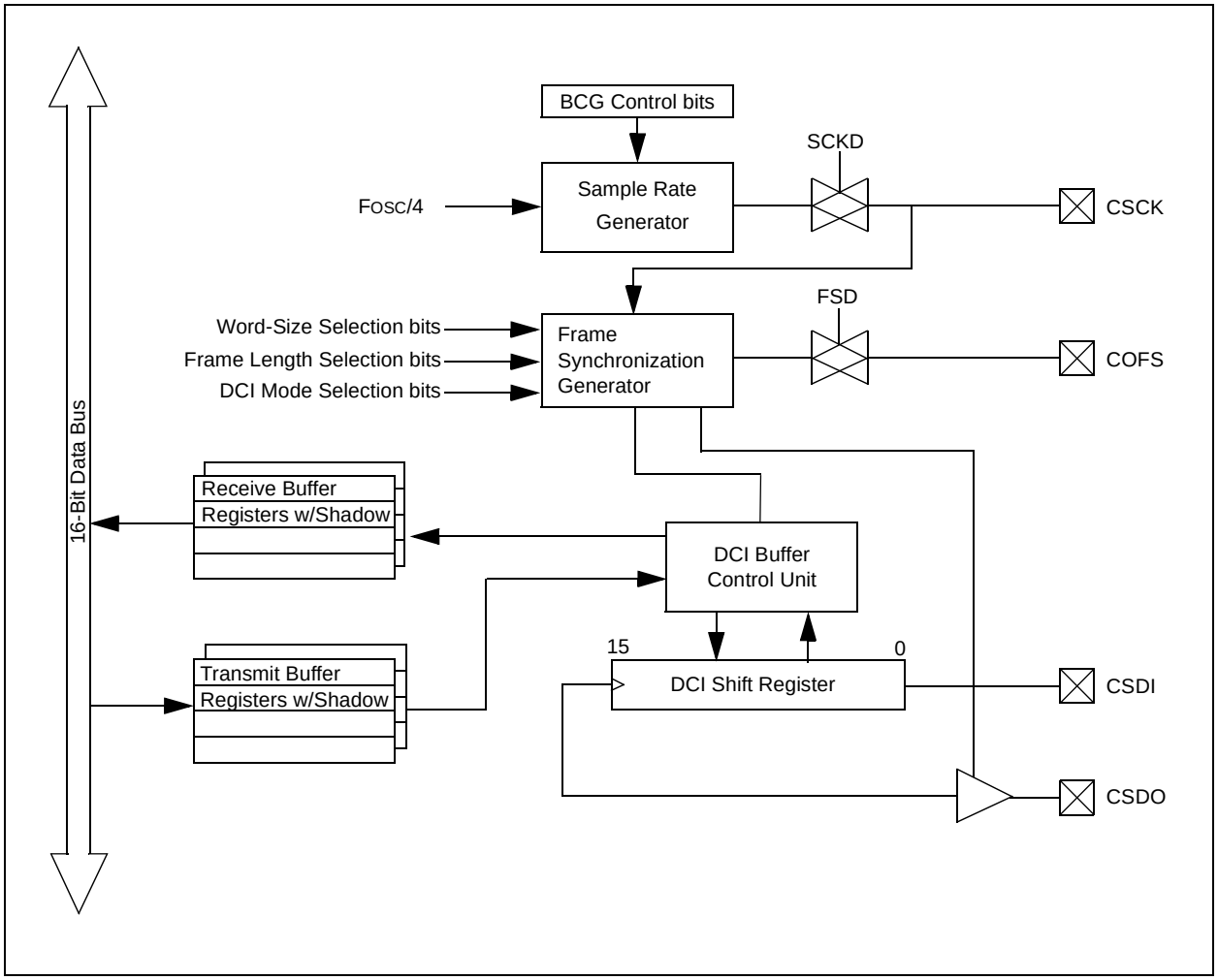
Legend: u = uninitialized bit; — = unimplemented bit, read as '0'
Note 1: Refer to the *"dsPIC30F Family Reference Manual*" (DS70046) for descriptions of register bit fields.

TABLE 16-2: dsPIC30F3014/4013 UART2 REGISTER MAP(1)

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
U2MODE	0216	UARTEN	—	USIDL	—	—	—	—	—	WAKE	LPBACK	ABAUD	—	—	PDSEL1	PDSEL0	STSEL	0000 0000 0000 0000
U2STA	0218	UTXISEL	—	—	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0000 0001 0001 0000
U2TXREG	021A	—	—	—	—	—	—	—	UTX8	Transmit Register								0000 000u uuuu uuuu
U2RXREG	021C	—	—	—	—	—	—	—	URX8	Receive Register								0000 0000 0000 0000
U2BRG	021E	Baud Rate Generator Prescaler																0000 0000 0000 0000

Legend: u = uninitialized bit; — = unimplemented bit, read as '0'
Note 1: Refer to the *"dsPIC30F Family Reference Manual*" (DS70046) for descriptions of register bit fields.

FIGURE 18-1: DCI MODULE BLOCK DIAGRAM



19.4 Programming the Start of Conversion Trigger

The conversion trigger terminates acquisition and starts the requested conversions.

The SSRC<2:0> bits select the source of the conversion trigger. The SSRC bits provide for up to 4 alternate sources of conversion trigger.

When SSRC<2:0> = 000, the conversion trigger is under software control. Clearing the SAMP bit causes the conversion trigger.

When SSRC<2:0> = 111 (Auto-Convert mode), the conversion trigger is under A/D clock control. The SAMC bits select the number of A/D clocks between the start of acquisition and the start of conversion. This provides the fastest conversion rates on multiple channels. The SAMC bits must always be at least one clock cycle.

Other trigger sources can come from timer modules or external interrupts.

19.5 Aborting a Conversion

Clearing the ADON bit during a conversion aborts the current conversion and stops the sampling sequencing until the next sampling trigger. The ADCBUF is not updated with the partially completed A/D conversion sample. That is, the ADCBUF will continue to contain the value of the last completed conversion (or the last value written to the ADCBUF register).

If clearing of the ADON bit coincides with an auto-start, the clearing has a higher priority and a new conversion does not start.

19.6 Selecting the ADC Conversion Clock

The ADC conversion requires 14 TAD. The source of the ADC conversion clock is software selected, using a 6-bit counter. There are 64 possible options for TAD.

EQUATION 19-1: ADC CONVERSION CLOCK

$$T_{AD} = T_{CY} * (0.5*(ADCS<5:0> + 1))$$

The internal RC oscillator is selected by setting the ADRC bit.

For correct ADC conversions, the ADC conversion clock (TAD) must be selected to ensure a minimum TAD time of 334 nsec (for VDD = 5V). Refer to **Section 23.0 "Electrical Characteristics"** for minimum TAD under other operating conditions.

Example 19-1 shows a sample calculation for the ADCS<5:0> bits, assuming a device operating speed of 30 MIPS.

EXAMPLE 19-1: ADC CONVERSION CLOCK AND SAMPLING RATE CALCULATION

Minimum T_{AD} = 334 nsec

T_{CY} = 33.33 nsec (30 MIPS)

$$ADCS<5:0> = 2\ \frac{T_{AD}}{T_{CY}} - 1$$

$$= 2 \bullet \frac{334\ nsec}{33.33\ nsec} - 1$$

$$= 19$$

Therefore,

Set ADCS<5:0> = 19

$$\text{Actual } T_{AD} = \frac{T_{CY}}{2}(ADCS<5:0> + 1)$$

$$= \frac{33.33\ nsec}{2}(19 + 1)$$

$$= 334\ nsec$$

If SSRC<2:0> = 111 and SAMC<4:0> = 00001

Since,

Sampling Time = Acquisition Time + Conversion Time

= 1 TAD + 14 TAD

= 15 x 334 nsec

Therefore,

$$\text{Sampling Rate} = \frac{1}{(15 \times 334\ nsec)}$$

= ~200 kHz

20.3 Oscillator Control Registers

The oscillators are controlled with two SFRs, OSCCON and OSCTUN and one Configuration register, FOSC.

Note:	The description of the OSCCON and OSCTUN SFRs, as well as the FOSC Configuration register provided in this section are applicable only to the dsPIC30F3014 and dsPIC30F4013 devices in the dsPIC30F product family.

REGISTER 20-1: OSCCON: OSCILLATOR CONTROL REGISTER

U-0	R-y	R-y	R-y	U-0	R/W-y	R/W-y	R/W-y
—	COSC<2:0>			—	NOSC<2:0>		
bit 15							bit 8

R/W-0	R/W-0	R-0	U-0	R/W-0	U-0	R/W-0	R/W-0
POST<1:0>		LOCK	—	CF	—	LPOSCEN	OSWEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **COSC<2:0>:** Current Oscillator Group Selection bits (read-only)
111 = PLL oscillator; PLL source selected by FPR<4:0> bits
011 = External oscillator; OSC1/OSC2 pins; external oscillator configuration selected by FPR<4:0> bits
010 = LPRC internal low-power RC
001 = FRC internal fast RC
000 = LP crystal oscillator; SOSCI/SOSCO pins
Set to FOS<2:0> values on POR or BOR. Loaded with NOSC<2:0> at the completion of a successful clock switch. Set to FRC value when FSCM detects a failure and switches clock to FRC.

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **NOSC<2:0>:** New Oscillator Group Selection bits
111 = PLL Oscillator; PLL source selected by FPR<4:0> bits
011 = External oscillator; OSC1/OSC2 pins; external oscillator configuration selected by FPR<4:0> bits
010 = LPRC internal low-power RC
001 = FRC internal fast RC
000 = LP crystal oscillator; SOSCI/SOSCO pins
Set to FOS<2:0> values on POR or BOR.

bit 7-6 **POST<1:0>:** Oscillator Postscaler Selection bits
11 = Oscillator postscaler divides clock by 64
10 = Oscillator postscaler divides clock by 16
01 = Oscillator postscaler divides clock by 4
00 = Oscillator postscaler does not alter clock

20.5 Watchdog Timer (WDT)

20.5.1 WATCHDOG TIMER OPERATION

The primary function of the Watchdog Timer (WDT) is to reset the processor in the event of a software malfunction. The WDT is a free-running timer that runs off an on-chip RC oscillator, requiring no external component. Therefore, the WDT timer continues to operate even if the main processor clock (e.g., the crystal oscillator) fails.

20.5.2 ENABLING AND DISABLING THE WDT

The Watchdog Timer can be “Enabled” or “Disabled” only through a Configuration bit (FWDTEN) in the Configuration register, FWDT.

Setting FWDTEN = 1 enables the Watchdog Timer. The enabling is done when programming the device. By default, after chip erase, FWDTEN bit = 1. Any device programmer capable of programming dsPIC30F devices allows programming of this and other Configuration bits.

If enabled, the WDT increments until it overflows or “times out”. A WDT time-out forces a device Reset (except during Sleep). To prevent a WDT time-out, the user must clear the Watchdog Timer using a CLRWDT instruction.

If a WDT times out during Sleep, the device wakes up. The WDTO bit in the RCON register is cleared to indicate a wake-up resulting from a WDT time-out.

Setting FWDTEN = 0 allows user software to enable/disable the Watchdog Timer via the SWDTEN (RCON<5>) control bit.

20.6 Low-Voltage Detect

The Low-Voltage Detect (LVD) module is used to detect when the V_{DD} of the device drops below a threshold value, V_{LVD}, which is determined by the LVDL<3:0> bits (RCON<11:8>) and is thus user programmable. The internal voltage reference circuitry requires a nominal amount of time to stabilize, and the BGST bit (RCON<13>) indicates when the voltage reference has stabilized.

In some devices, the LVD threshold voltage may be applied externally on the LVDIN pin.

The LVD module is enabled by setting the LVDEN bit (RCON<12>).

20.7 Power-Saving Modes

There are two power-saving states that can be entered through the execution of a special instruction, PWRSAV; these are Sleep and Idle.

The format of the PWRSAV instruction is as follows:

PWRSAV <parameter>, where ‘parameter’ defines Idle or Sleep mode.

20.7.1 SLEEP MODE

In Sleep mode, the clock to the CPU and peripherals is shut down. If an on-chip oscillator is being used, it is shut down.

The Fail-Safe Clock Monitor is not functional during Sleep since there is no clock to monitor. However, the LPRC clock remains active if WDT is operational during Sleep.

The brown-out protection circuit and the Low-Voltage Detect (LVD) circuit, if enabled, remains functional during Sleep.

The processor wakes up from Sleep if at least one of the following conditions has occurred:

- any interrupt that is individually enabled and meets the required priority level
- any Reset (POR, BOR and $\overline{\text{MCLR}}$)
- WDT time-out

On waking up from Sleep mode, the processor restarts the same clock that was active prior to entry into Sleep mode. When clock switching is enabled, bits, COSC<2:0>, determine the oscillator source to be used on wake-up. If clock switch is disabled, then there is only one system clock.

Note:	If a POR or BOR occurred, the selection of the oscillator is based on the FOS<2:0> and FPR<4:0> Configuration bits.

If the clock source is an oscillator, the clock to the device is held off until OST times out (indicating a stable oscillator). If PLL is used, the system clock is held off until LOCK = 1 (indicating that the PLL is stable). In either case, T_{POR}, T_{LOCK} and T_{PWRT} delays are applied.

If EC, FRC, LPRC or ERC oscillators are used, then a delay of T_{POR} (~ 10 μs) is applied. This is the smallest delay possible on wake-up from Sleep.

Moreover, if the LP oscillator was active during Sleep and LP is the oscillator used on wake-up, then the start-up delay is equal to T_{POR}. PWRT delay and OST timer delay are not applied. In order to have the smallest possible start-up delay when waking up from Sleep, one of these faster wake-up options should be selected before entering Sleep.

TABLE 20-7: SYSTEM INTEGRATION REGISTER MAP(1)

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
RCON	0740	TRAPR	IOPUWR	BGST	LVDEN	LVDL<3:0>				EXTR	SWR	SWDTEN	WDTO	SLEEP	IDLE	BOR	POR	(Note 2)
OSCCON	0742	—	COSC<2:0>			—	NOSC<2:0>			POST<1:0>		LOCK	—	CF	—	LPOSCEN	OSWEN	(Note 3)
OSCTUN	0744	—	—	—	—	—	—	—	—	—	—	—	—	TUN3	TUN2	TUN1	TUN0	0000 0000 0000 0000
PMD1	0770	T5MD(4)	T4MD(4)	T3MD	T2MD	T1MD	—	—	DCIMD(4)	I2CMD	U2MD	U1MD	—	SPI1MD	—	C1MD	ADCMD	0000 0000 0000 0000
PMD2	0772	IC8MD(4)	IC7MD(4)	—	—	—	—	IC2MD	IC1MD	—	—	—	—	OC4MD(4)	OC3MD(4)	OC2MD	OC1MD	0000 0000 0000 0000

Legend: — = unimplemented bit, read as '0'

Note 1: Refer to the *"dsPIC30F Family Reference Manual"* (DS70046) for descriptions of register bit fields.

2: Reset state depends on type of Reset.

3: Reset state depends on Configuration bits.

4: These bits are not available in dsPIC30F3014 devices.

TABLE 20-8: DEVICE CONFIGURATION REGISTER MAP(1)

Name	Address	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FOSC	F80000	FCKSM<1:0>		—	—	—	FOS<2:0>			—	—	—	FPR<4:0>				
FWDT	F80002	FWDTEN	—	—	—	—	—	—	—	—	—	FWPSA<1:0>		FWPSB<3:0>			
FBORPOR	F80004	MCLREN	—	—	—	—	PWMPIN(2)	HPOL(2)	LPOL(2)	BOREN	—	BORV<1:0>		—	—	FPWRT<1:0>	
FBS	F80006	—	—	Reserved(3)		—	—	—	Reserved(3)	—	—	—	—	Reserved(3)			
FSS	F80008	—	—	Reserved(3)		—	—	Reserved(3)		—	—	—	—	Reserved(3)			
FGS	F8000A	—	—	—	—	—	—	—	—	—	—	—	—	—	Reserved(4)	GCP	GWRP
FICD	F8000C	BKBUG	COE	—	—	—	—	—	—	—	—	—	—	—	—	ICS<1:0>	

Legend: — = unimplemented bit, read as '0'

Note 1: Refer to the *"dsPIC30F Family Reference Manual"* (DS70046) for descriptions of register bit fields.

2: These bits are reserved (read as '1' and must be programmed as '1').

3: Reserved bits read as '1' and must be programmed as '1'.

4: The FGS<2> bit is a read-only copy of the GCP bit (FGS<1>).

23.1 DC Characteristics

TABLE 23-1: OPERATING MIPS vs. VOLTAGE

VDD Range	Temp Range	Max MIPS	
		dsPIC30FXXX-30I	dsPIC30FXXX-20E
4.5-5.5V	-40°C to 85°C	30	—
4.5-5.5V	-40°C to 125°C	—	20
3.0-3.6V	-40°C to 85°C	15	—
3.0-3.6V	-40°C to 125°C	—	10
2.5-3.0V	-40°C to 85°C	10	—

TABLE 23-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min	Typ	Max	Unit
dsPIC30F3014-30I dsPIC30F4013-30I					
Operating Junction Temperature Range	T_J	-40	—	+125	°C
Operating Ambient Temperature Range	T_A	-40	—	+85	°C
dsPIC30F3014-20E dsPIC30F4013-20E					
Operating Junction Temperature Range	T_J	-40	—	+150	°C
Operating Ambient Temperature Range	T_A	-40	—	+125	°C
Power Dissipation: Internal chip power dissipation: $P_{INT} = V_{DD} \times (I_{DD} - \sum I_{OH})$ I/O Pin power dissipation: $P_{I/O} = \sum (\{V_{DD} - V_{OH}\} \times I_{OH}) + \sum (V_{OL} \times I_{OL})$	P_D	$P_{INT} + P_{I/O}$			W
Maximum Allowed Power Dissipation	P_{DMAX}	$(T_J - T_A)/\theta_{JA}$			W

TABLE 23-3: THERMAL PACKAGING CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit	Notes
Package Thermal Resistance, 40-pin DIP (P)	θ_{JA}	—	47	°C/W	1
Package Thermal Resistance, 44-pin TQFP (10x10x1mm)	θ_{JA}	—	39.3	°C/W	1
Package Thermal Resistance, 44-pin QFN	θ_{JA}	—	27.8	°C/W	1

Note 1: Junction to ambient thermal resistance, Theta-ja (θ_{JA}) numbers are achieved by package simulations.

TABLE 23-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Operating Voltage(2)							
DC10	VDD	**Supply Voltage**	2.5	—	5.5	V	Industrial temperature
DC11	VDD	**Supply Voltage**	3.0	—	5.5	V	Extended temperature
DC12	VDR	**RAM Data Retention Voltage(3)**	1.75	—	—	V	
DC16	VPOR	**VDD Start Voltage** to Ensure Internal Power-on Reset Signal	—	—	VSS	V	
DC17	SVDD	**VDD Rise Rate** to Ensure Internal Power-on Reset Signal	0.05	—	—	V/ms	0-5V in 0.1 sec 0-3V in 60 ms

Note 1: Data in "Typ" column is at 5V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: These parameters are characterized but not tested in manufacturing.

3: This is the limit to which VDD can be lowered without losing RAM data.

TABLE 23-30: SPI MASTER MODE (CKE = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min**	**Typ(2)**	**Max**	**Units**	**Conditions**
SP10	TscL	SCKx Output Low Time(3)	TCY/2	—	—	ns	
SP11	TscH	SCKx Output High Time(3)	TCY/2	—	—	ns	
SP20	TscF	SCKx Output Fall Time(4	—	—	—	ns	See parameter DO32
SP21	TscR	SCKx Output Rise Time(4)	—	—	—	ns	See parameter DO31
SP30	TdoF	SDOx Data Output Fall Time(4)	—	—	—	ns	See parameter DO32
SP31	TdoR	SDOx Data Output Rise Time(4)	—	—	—	ns	See parameter DO31
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	30	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	20	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	20	—	—	ns	

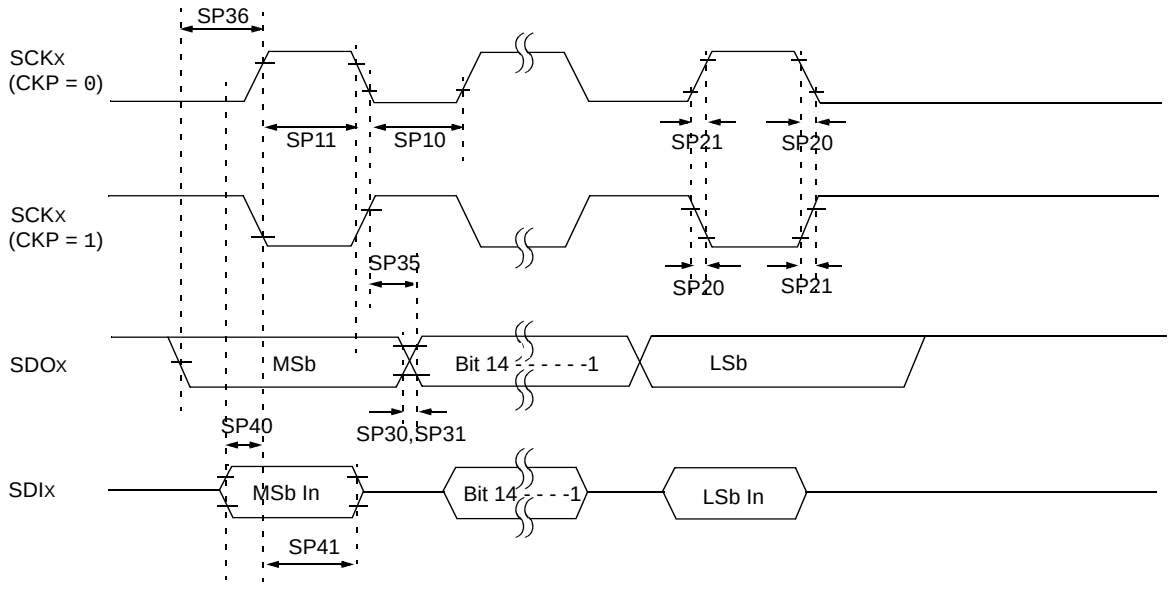
Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ" column is at 5V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 100 ns. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPI pins.

FIGURE 23-15: SPI MODULE MASTER MODE (CKE =1) TIMING CHARACTERISTICS

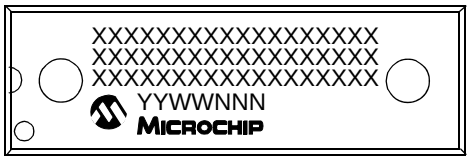


Note: Refer to Figure 23-3 for load conditions.

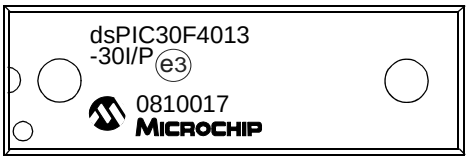
24.0 PACKAGING INFORMATION

24.1 Package Marking Information

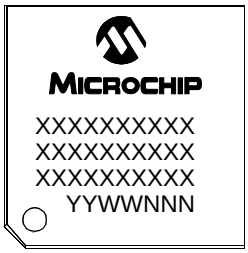
40-Lead PDIP



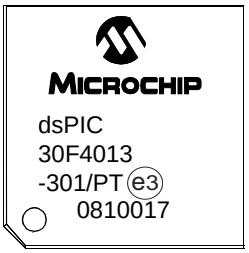
Example



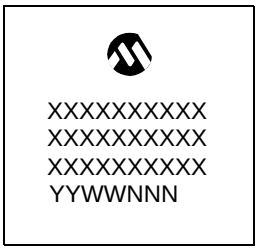
44-Lead TQFP



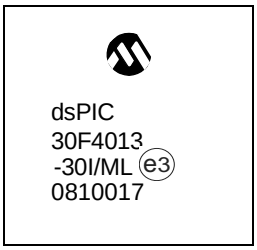
Example



44-Lead QFN



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.