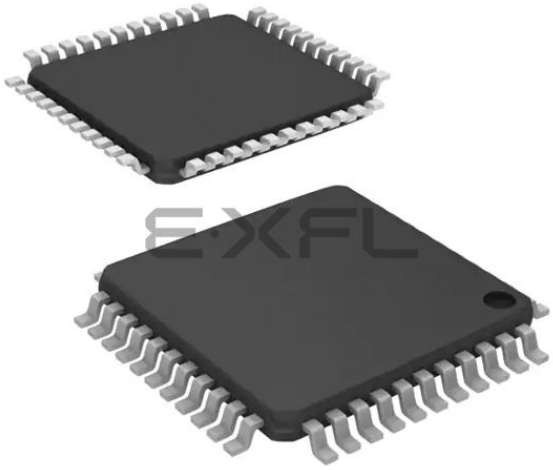

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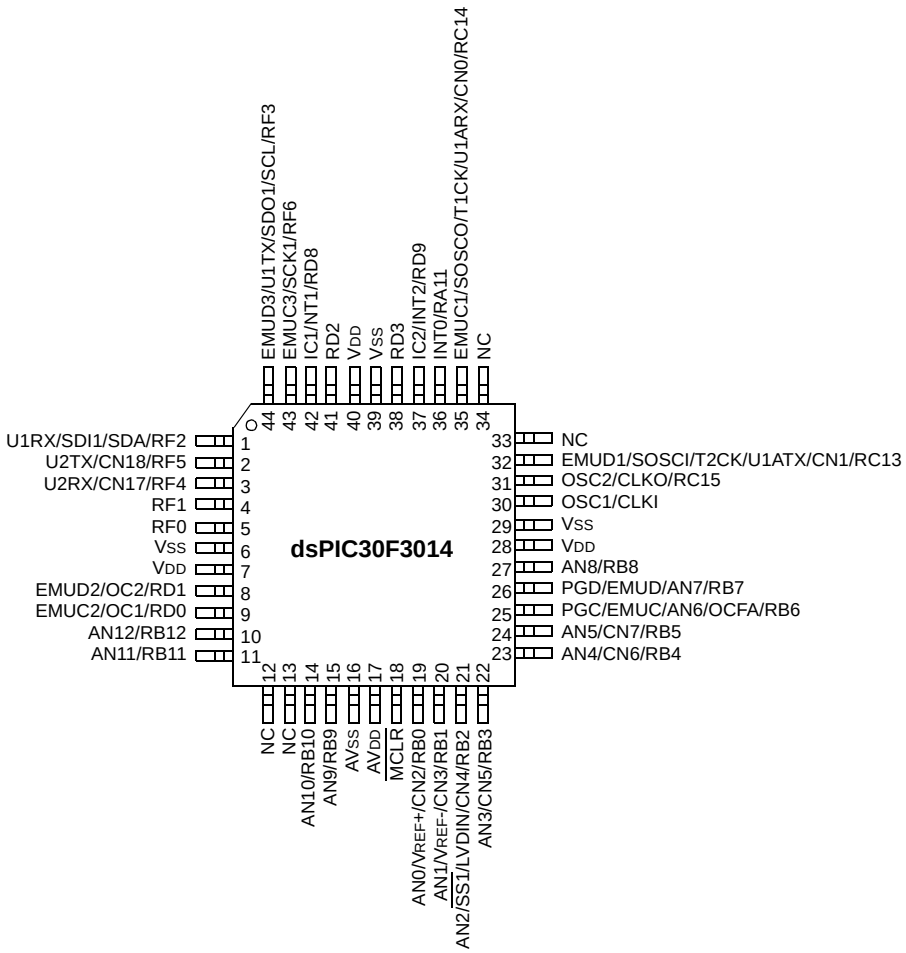
Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	30 MIPs
Connectivity	CANbus, I²C, SPI, UART/USART
Peripherals	AC'97, Brown-out Detect/Reset, I²S, POR, PWM, WDT
Number of I/O	30
Program Memory Size	48KB (16K x 24)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 13x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic30f4013t-30i-pt

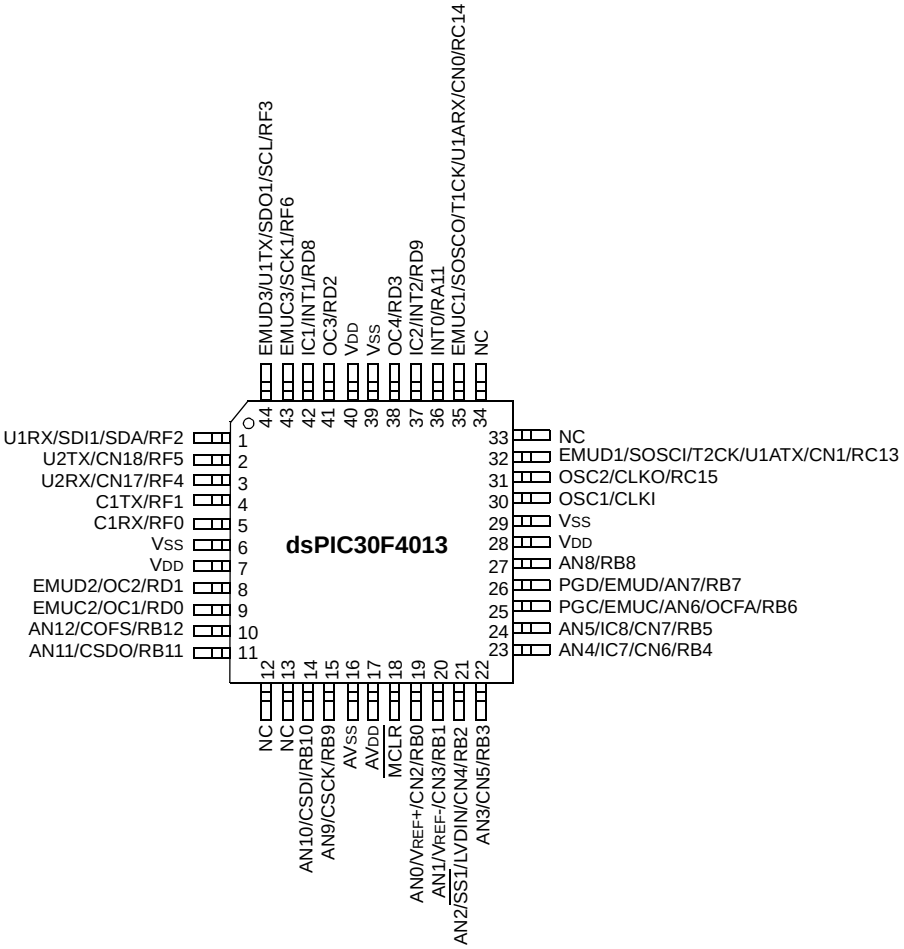
Pin Diagrams (Continued)

44-Pin TQFP



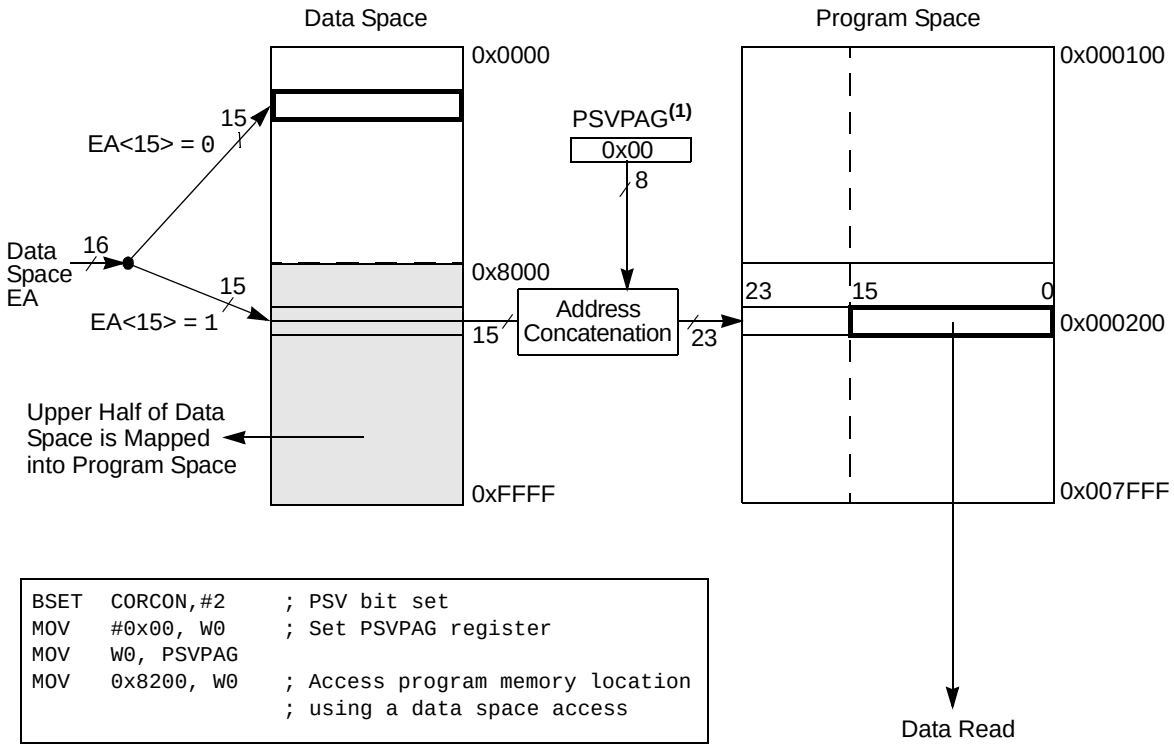
Pin Diagrams (Continued)

44-Pin TQFP



NOTES:

FIGURE 3-6: DATA SPACE WINDOW INTO PROGRAM SPACE OPERATION




```
BSET   CORCON,#2     ; PSV bit set
MOV    #0x00, W0     ; Set PSVPAG register
MOV    W0, PSVPAG
MOV    0x8200, W0    ; Access program memory location
                     ; using a data space access
```

Note: PSVPAG is an 8-bit register, containing bits<22:15> of the program space address (i.e., it defines the page in program space to which the upper half of data space is being mapped).
The memory map shown here is for a dsPIC30F4013 device.

NOTES:

5.4 RTSP Operation

The dsPIC30F Flash program memory is organized into rows and panels. Each row consists of 32 instructions or 96 bytes. Each panel consists of 128 rows or 4K x 24 instructions. RTSP allows the user to erase one row (32 instructions) at a time and to program four instructions at one time. RTSP may be used to program multiple program memory panels, but the Table Pointer must be changed at each panel boundary.

Each panel of program memory contains write latches that hold 32 instructions of programming data. Prior to the actual programming operation, the write data must be loaded into the panel write latches. The data to be programmed into the panel is loaded in sequential order into the write latches; instruction 0, instruction 1, etc. The instruction words loaded must always be from a 32 address boundary.

The basic sequence for RTSP programming is to set up a Table Pointer, then do a series of TBLWT instructions to load the write latches. Programming is performed by setting the special bits in the NVMCON register. 32 TBLWTL and four TBLWTH instructions are required to load the 32 instructions. If multiple panel programming is required, the Table Pointer needs to be changed and the next set of multiple write latches written.

All of the table write operations are single-word writes (2 instruction cycles), because only the table latches are written. A programming cycle is required for programming each row.

The Flash program memory is readable, writable and erasable during normal operation over the entire VDD range.

5.5 Control Registers

The four SFRs used to read and write the program Flash memory are:

- NVMCON
- NVMADR
- NVMADRU
- NVMKEY

5.5.1 NVMCON REGISTER

The NVMCON register controls which blocks are to be erased, which memory type is to be programmed and the start of the programming cycle.

5.5.2 NVMADR REGISTER

The NVMADR register is used to hold the lower two bytes of the Effective Address. The NVMADR register captures the EA<15:0> of the last table instruction that has been executed and selects the row to write.

5.5.3 NVMADRU REGISTER

The NVMADRU register is used to hold the upper byte of the Effective Address. The NVMADRU register captures the EA<23:16> of the last table instruction that has been executed.

5.5.4 NVMKEY REGISTER

NVMKEY is a write-only register that is used for write protection. To start a programming or erase sequence, the user must consecutively write 0x55 and 0xAA to the NVMKEY register. Refer to **Section 5.6 “Programming Operations”** for further details.

Note:	The user can also directly write to the NVMADR and NVMADRU registers to specify a program memory address for erasing or programming.

TABLE 5-1: NVM REGISTER MAP(1)

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
NVMCON	0760	WR	WREN	WRERR	—	—	—	—	TWRI	—	PROGOP<6:0>							0000 0000 0000 0000
NVMADR	0762	NVMADR<15:0>																uuuu uuuu uuuu uuuu
NVMADRU	0764	—	—	—	—	—	—	—	—	NVMADR<23:16>								0000 0000 uuuu uuuu
NVMKEY	0766	—	—	—	—	—	—	—	—	KEY<7:0>								0000 0000 0000 0000

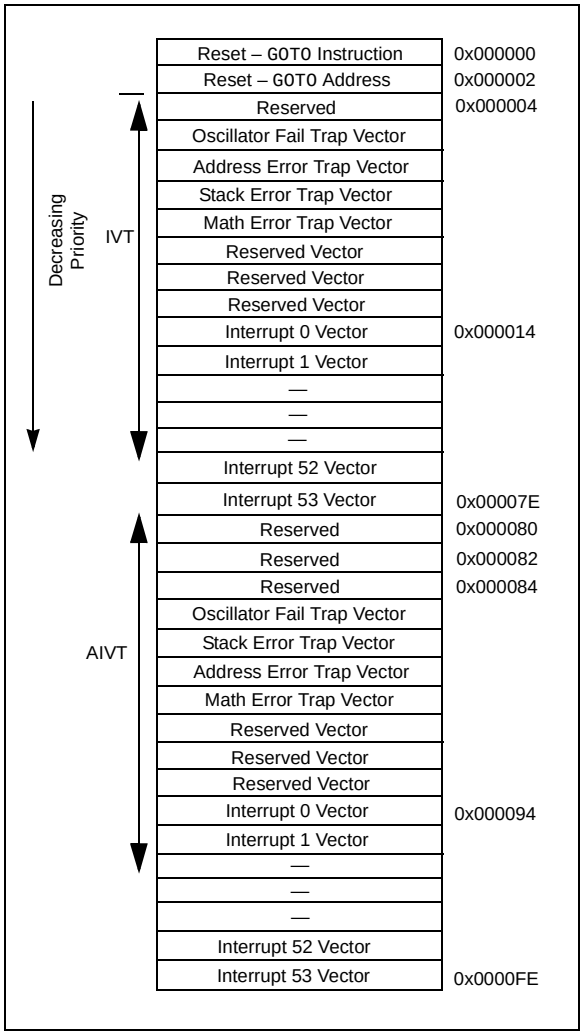
Legend: u = uninitialized bit; — = unimplemented bit, read as '0'

Note 1: Refer to the *"dsPIC30F Family Reference Manual*" (DS70046) for descriptions of register bit fields.

Each hard trap that occurs must be Acknowledged before code execution of any type may continue. If a lower priority hard trap occurs while a higher priority trap is pending, Acknowledged, or is being processed, a hard trap conflict occurs.

The device is automatically Reset in a hard trap conflict condition. The TRAPR status bit (RCON<15>) is set when the Reset occurs so that the condition may be detected in software.

FIGURE 8-1: TRAP VECTORS



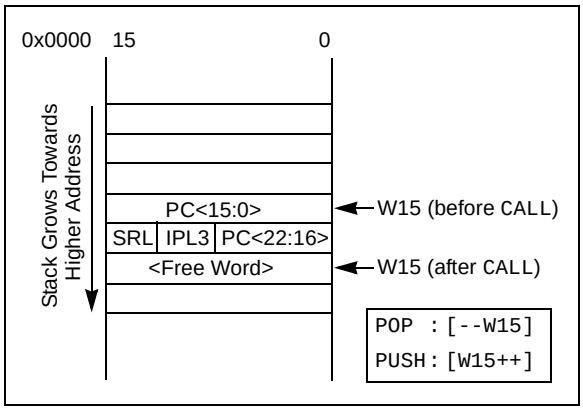
8.4 Interrupt Sequence

All interrupt event flags are sampled in the beginning of each instruction cycle by the IFSx registers. A pending Interrupt Request (IRQ) is indicated by the flag bit being equal to a '1' in an IFSx register. The IRQ causes an interrupt to occur if the corresponding bit in the Interrupt Enable (IECx) register is set. For the remainder of the instruction cycle, the priorities of all pending interrupt requests are evaluated.

If there is a pending IRQ with a priority level greater than the current processor priority level in the IPL bits, the processor is interrupted.

The processor then stacks the current program counter and the low byte of the processor STATUS register (SRL), as shown in Figure 8-2. The low byte of the STATUS register contains the processor priority level at the time prior to the beginning of the interrupt cycle. The processor then loads the priority level for this interrupt into the STATUS register. This action disables all lower priority interrupts until the completion of the Interrupt Service Routine.

FIGURE 8-2: INTERRUPT STACK FRAME

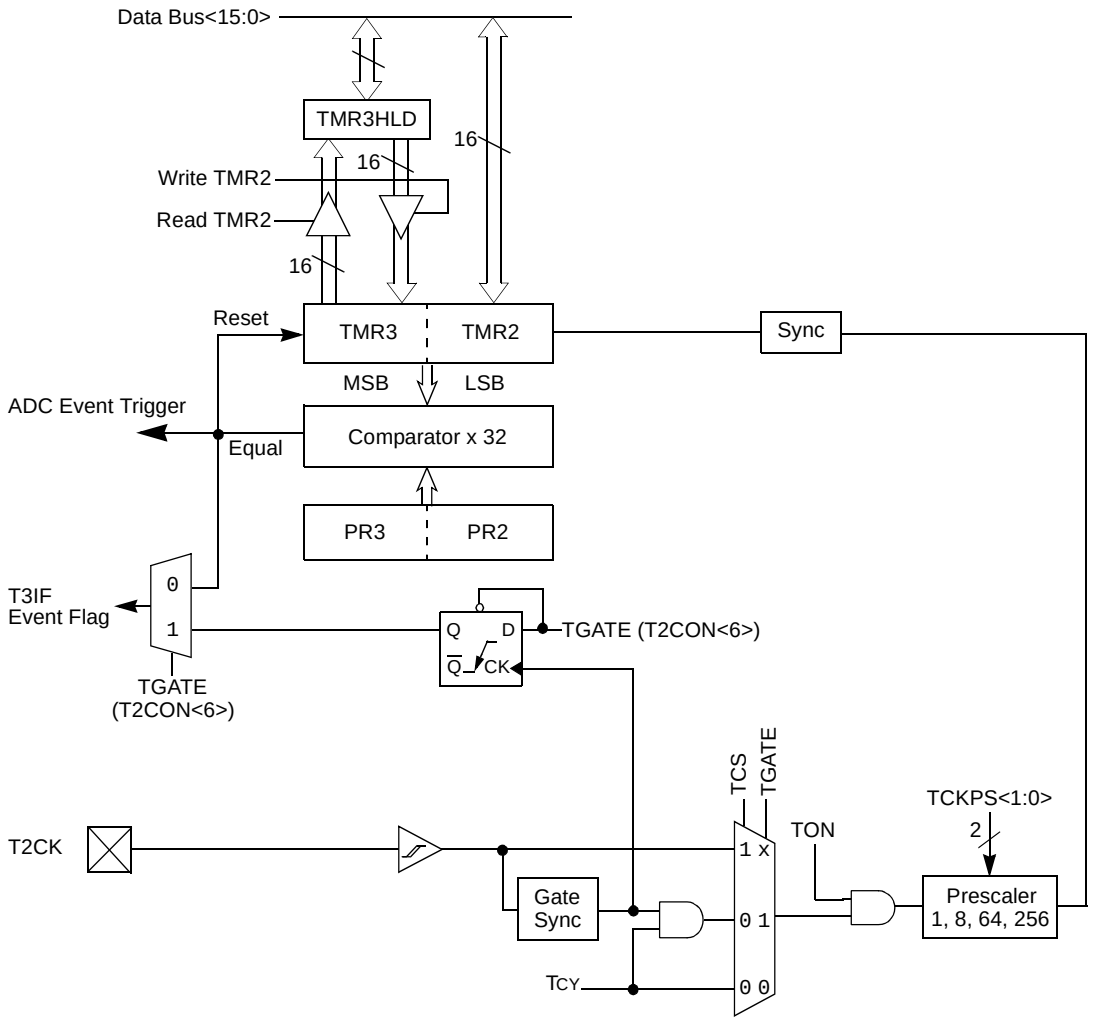


Note 1: The user can always lower the priority level by writing a new value into SR. The Interrupt Service Routine must clear the interrupt flag bits in the IFSx register before lowering the processor interrupt priority, in order to avoid recursive interrupts.

2: The IPL3 bit (CORCON<3>) is always clear when interrupts are being processed. It is set only during execution of traps.

The RETFIE (return from interrupt) instruction unstacks the program counter and STATUS registers to return the processor to its state prior to the interrupt sequence.

FIGURE 10-1: 32-BIT TIMER2/3 BLOCK DIAGRAM



Note: Timer Configuration bit, T32 (T2CON<3>), must be set to '1' for a 32-bit timer/counter operation. All control bits are respective to the T2CON register.

13.0 OUTPUT COMPARE MODULE

Note: This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the "*dsPIC30F Family Reference Manual*" (DS70046).

This section describes the output compare module and associated operational modes. The features provided by this module are useful in applications requiring operational modes, such as:

- Generation of Variable Width Output Pulses
- Power Factor Correction

Figure 13-1 depicts a block diagram of the output compare module.

The key operational features of the output compare module include:

- Timer2 and Timer3 Selection mode
- Simple Output Compare Match mode
- Dual Output Compare Match mode
- Simple PWM mode
- Output Compare During Sleep and Idle modes
- Interrupt on Output Compare/PWM Event

These operating modes are determined by setting the appropriate bits in the 16-bit OCxCON SFR (where x = 1,2,3,...,N). The dsPIC DSC devices contain up to 8 compare channels (i.e., the maximum value of N is 8). The dsPIC30F3014 device contains 2 compare channels while the dsPIC30F4013 device contains 4 compare channels.

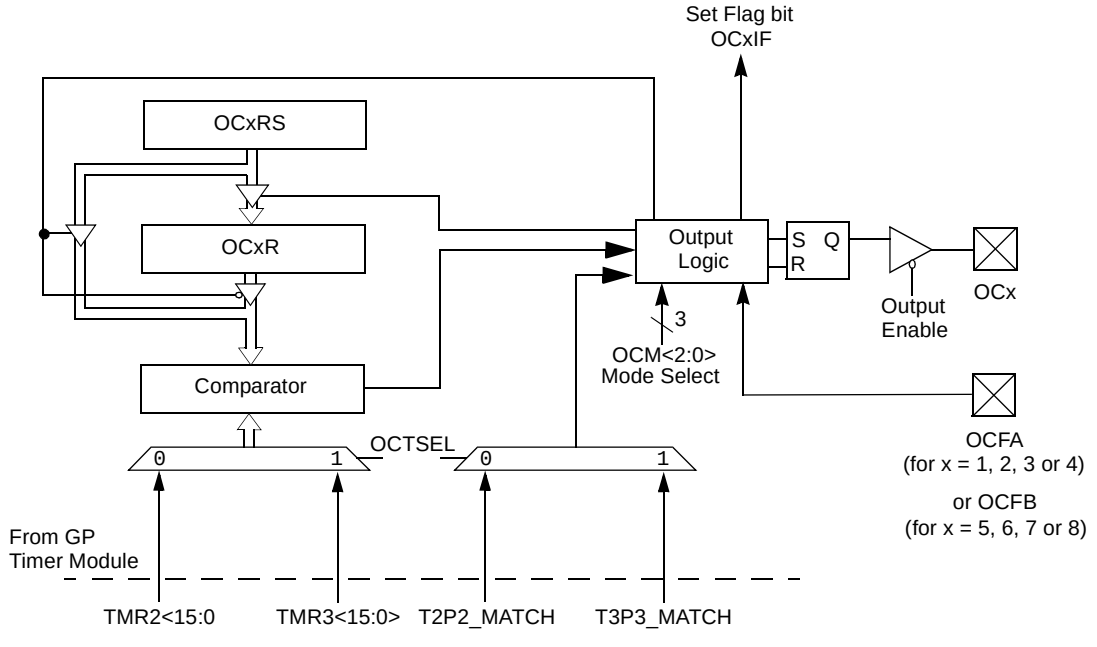
OCxRS and OCxR in Figure 13-1 represent the Dual Compare registers. In the Dual Compare mode, the OCxR register is used for the first compare and OCxRS is used for the second compare.

13.1 Timer2 and Timer3 Selection Mode

Each output compare channel can select between one of two 16-bit timers: Timer2 or Timer3.

The selection of the timers is controlled by the OCTSEL bit (OCxCON<3>). Timer2 is the default timer resource for the output compare module.

FIGURE 13-1: OUTPUT COMPARE MODE BLOCK DIAGRAM



Note: Where 'x' is shown, reference is made to the registers associated with the respective output compare channels, 1 through N.

TABLE 14-2: dsPIC30F3014/4013 I²C REGISTER MAP(1)

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
I2CRCV	0200	—	—	—	—	—	—	—	—	Receive Register								0000 0000 0000 0000
I2CTRN	0202	—	—	—	—	—	—	—	—	Transmit Register								0000 0000 1111 1111
I2CBRG	0204	—	—	—	—	—	—	—	Baud Rate Generator									0000 0000 0000 0000
I2CCON	0206	I2CEN	—	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	0001 0000 0000 0000
I2CSTAT	0208	ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF	0000 0000 0000 0000
I2CADD	020A	—	—	—	—	—	—	Address Register										0000 0000 0000 0000

Legend: — = unimplemented bit, read as '0'

Note 1: Refer to the *"dsPIC30F Family Reference Manual*" (DS70046) for descriptions of register bit fields.

18.3 DCI Module Operation

18.3.1 MODULE ENABLE

The DCI module is enabled or disabled by setting/clearing the DCIEN control bit in the DCICON1 SFR. Clearing the DCIEN control bit has the effect of resetting the module. In particular, all counters associated with CSCK generation, Frame Sync, and the DCI buffer control unit are reset.

The DCI clocks are shut down when the DCIEN bit is cleared.

When enabled, the DCI controls the data direction for the four I/O pins associated with the module. The port, LAT and TRIS register values for these I/O pins are overridden by the DCI module when the DCIEN bit is set.

It is also possible to override the CSCK pin separately when the bit clock generator is enabled. This permits the bit clock generator to operate without enabling the rest of the DCI module.

18.3.2 WORD-SIZE SELECTION BITS

The WS<3:0> word-size selection bits in the DCICON2 SFR determine the number of bits in each DCI data word. Essentially, the WS<3:0> bits determine the counting period for a 4-bit counter clocked from the CSCK signal.

Any data length, up to 16 bits, may be selected. The value loaded into the WS<3:0> bits is one less the desired word length. For example, a 16-bit data word size is selected when WS<3:0> = 1111.

Note:	These WS<3:0> control bits are used only in the Multichannel and I^2S modes. These bits have no effect in AC-Link mode since the data slot sizes are fixed by the protocol.

18.3.3 FRAME SYNC GENERATOR

The Frame Sync generator (COFSG) is a 4-bit counter that sets the frame length in data words. The Frame Sync generator is incremented each time the word-size counter is reset (refer to **Section 18.3.2 "Word-Size Selection Bits"**). The period for the Frame Synchronization generator is set by writing the COFSG<3:0> control bits in the DCICON2 SFR. The COFSG period in clock cycles is determined by the following formula:

EQUATION 18-1: COFSG PERIOD

$$\text{Frame Length} = \text{Word Length} \bullet (\text{FSG Value} + 1)$$

Frame lengths, up to 16 data words, may be selected. The frame length in CSCK periods can vary up to a maximum of 256 depending on the word size that is selected.

Note:	The COFSG control bits have no effect in AC-Link mode since the frame length is set to 256 CSCK periods by the protocol.

18.3.4 FRAME SYNC MODE CONTROL BITS

The type of Frame Sync signal is selected using the Frame Synchronization mode control bits (COFSM<1:0>) in the DCICON1 SFR. The following operating modes can be selected:

- Multichannel mode
- I^2S mode
- AC-Link mode (16-bit)
- AC-Link mode (20-bit)

The operation of the COFSM control bits depends on whether the DCI module generates the Frame Sync signal as a master device, or receives the Frame Sync signal as a slave device.

The master device in a DSP/Codec pair is the device that generates the Frame Sync signal. The Frame Sync signal initiates data transfers on the CSDI and CSDO pins and usually has the same frequency as the data sample rate (COFS).

The DCI module is a Frame Sync master if the COFSD control bit is cleared and is a Frame Sync slave if the COFSD control bit is set.

18.3.5 MASTER FRAME SYNC OPERATION

When the DCI module is operating as a Frame Sync master device (COFSD = 0), the COFSM mode bits determine the type of Frame Sync pulse that is generated by the Frame Sync generator logic.

A new COFS signal is generated when the Frame Sync generator resets to '0'.

In the Multichannel mode, the Frame Sync pulse is driven high for the CSCK period to initiate a data transfer. The number of CSCK cycles between successive Frame Sync pulses depends on the word size and Frame Sync generator control bits. A timing diagram for the Frame Sync signal in Multichannel mode is shown in Figure 18-2.

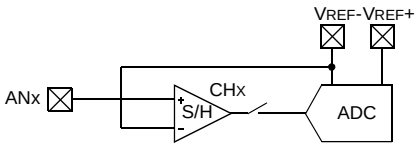
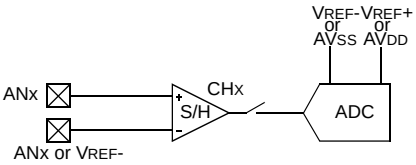
In the AC-Link mode of operation, the Frame Sync signal has a fixed period and duty cycle. The AC-Link Frame Sync signal is high for 16 CSCK cycles and is low for 240 CSCK cycles. A timing diagram with the timing details at the start of an AC-Link frame is shown in Figure 18-3.

In the I^2S mode, a Frame Sync signal having a 50% duty cycle is generated. The period of the I^2S Frame Sync signal in CSCK cycles is determined by the word

19.7 ADC Speeds

The dsPIC30F 12-bit ADC specifications permit a maximum of 200 ksps sampling rate. The table below summarizes the conversion speeds for the dsPIC30F 12-bit ADC and the required operating conditions.

TABLE 19-1: 12-BIT ADC EXTENDED CONVERSION RATES

dsPIC30F 12-Bit ADC Conversion Rates						
Speed	**TAD Minimum**	**Sampling Time Min**	**R_S Max**	**VDD**	**Temperature**	**Channels Configuration**
Up to 200 ksps(1)	334 ns	1 TAD	2.5 kΩ	4.5V to 5.5V	-40°C to +85°C	
Up to 100 ksps	668 ns	1 TAD	2.5 kΩ	3.0V to 5.5V	-40°C to +125°C	

Note 1: External VREF- and VREF+ pins must be used for correct operation. See Figure 19-2 for recommended circuit.

20.2.3 LP OSCILLATOR CONTROL

Enabling the LP oscillator is controlled with two elements:

- The current oscillator group bits, COSC<2:0>.
- The LPOSCEN bit (OSCCON register).

The LP oscillator is on (even during Sleep mode) if LPOSCEN = 1. The LP oscillator is the device clock if:

- COSC<2:0> = 00 (LP selected as main osc.) and
- LPOSCEN = 1

Keeping the LP oscillator on at all times allows for a fast switch to the 32 kHz system clock for lower power operation. Returning to the faster main oscillator still requires a start-up time

20.2.4 PHASE LOCKED LOOP (PLL)

The PLL multiplies the clock which is generated by the primary oscillator. The PLL is selectable to have either gains of x4, x8 and x16. Input and output frequency ranges are summarized in Table 20-3.

TABLE 20-3: PLL FREQUENCY RANGE

FIN	PLL Multiplier	FOUT
4 MHz-10 MHz	x4	16 MHz-40 MHz
4 MHz-10 MHz	x8	32 MHz-80 MHz
4 MHz-7.5 MHz	x16	64 MHz-120 MHz

The PLL features a lock output which is asserted when the PLL enters a phase locked state. Should the loop fall out of lock (e.g., due to noise), the lock signal is rescinded. The state of this signal is reflected in the read-only LOCK bit in the OSCCON register.

20.2.5 FAST RC OSCILLATOR (FRC)

The FRC oscillator is a fast (7.37 MHz ±2% nominal) internal RC oscillator. This oscillator is intended to provide reasonable device operating speeds without the use of an external crystal, ceramic resonator, or RC network. The FRC oscillator can be used with the PLL to obtain higher clock frequencies.

The dsPIC30F operates from the FRC oscillator whenever the current oscillator selection control bits in the OSCCON register (OSCCON<14:12>) are set to '001'.

The four-bit field specified by TUN<3:0> (OSCTUN<3:0>) allows the user to tune the internal fast RC oscillator (nominal 7.37 MHz). The user can tune the FRC oscillator within a range of +10.5% (840 kHz) and -12% (960 kHz) in steps of 1.50% around the factory-calibrated setting (see Table 20-4).

Note: OSCTUN functionality has been provided to help customers compensate for temperature effects on the FRC frequency over a wide range of temperatures. The tuning step size is an approximation and is neither characterized nor tested.

If OSCCON<14:12> are set to '111' and FPR<4:0> are set to '00101', '00110' or '00111', then a PLL multiplier of 4, 8 or 16 (respectively) is applied.

Note: When a 16x PLL is used, the FRC frequency must not be tuned to a frequency greater than 7.5 MHz.

TABLE 20-4: FRC TUNING

TUN<3:0> Bits	FRC Frequency
0111	+10.5%
0110	+9.0%
0101	+7.5%
0100	+6.0%
0011	+4.5%
0010	+3.0%
0001	+1.5%
0000	Center Frequency (oscillator is running at calibrated frequency)
1111	-1.5%
1110	-3.0%
1101	-4.5%
1100	-6.0%
1011	-7.5%
1010	-9.0%
1001	-10.5%
1000	-12.0%

20.2.6 LOW-POWER RC OSCILLATOR (LPRC)

The LPRC oscillator is a component of the Watchdog Timer (WDT) and oscillates at a nominal frequency of 512 kHz. The LPRC oscillator is the clock source for the Power-up Timer (PWRT) circuit, WDT and clock monitor circuits. It may also be used to provide a low-frequency clock source option for applications where power consumption is critical and timing accuracy is not required.

The LPRC oscillator is always enabled at a Power-on Reset because it is the clock source for the PWRT. After the PWRT expires, the LPRC oscillator remains on if one of the following is TRUE:

- The Fail-Safe Clock Monitor is enabled
- The WDT is enabled
- The LPRC oscillator is selected as the system clock via the COSC<2:0> control bits in the OSCCON register

If one of the above conditions is not true, the LPRC shuts off after the PWRT expires.

Note 1: OSC2 pin function is determined by the Primary Oscillator mode selection (FPR<4:0>).

2: OSC1 pin cannot be used as an I/O pin even if the secondary oscillator or an internal clock source is selected at all times.

20.3 Oscillator Control Registers

The oscillators are controlled with two SFRs, OSCCON and OSCTUN and one Configuration register, FOSC.

Note:	The description of the OSCCON and OSCTUN SFRs, as well as the FOSC Configuration register provided in this section are applicable only to the dsPIC30F3014 and dsPIC30F4013 devices in the dsPIC30F product family.

REGISTER 20-1: OSCCON: OSCILLATOR CONTROL REGISTER

U-0	R-y	R-y	R-y	U-0	R/W-y	R/W-y	R/W-y
—	COSC<2:0>			—	NOSC<2:0>		
bit 15							bit 8

R/W-0	R/W-0	R-0	U-0	R/W-0	U-0	R/W-0	R/W-0
POST<1:0>		LOCK	—	CF	—	LPOSCEN	OSWEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-12 **COSC<2:0>:** Current Oscillator Group Selection bits (read-only)
111 = PLL oscillator; PLL source selected by FPR<4:0> bits
011 = External oscillator; OSC1/OSC2 pins; external oscillator configuration selected by FPR<4:0> bits
010 = LPRC internal low-power RC
001 = FRC internal fast RC
000 = LP crystal oscillator; SOSCI/SOSCO pins
Set to FOS<2:0> values on POR or BOR. Loaded with NOSC<2:0> at the completion of a successful clock switch. Set to FRC value when FSCM detects a failure and switches clock to FRC.

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **NOSC<2:0>:** New Oscillator Group Selection bits
111 = PLL Oscillator; PLL source selected by FPR<4:0> bits
011 = External oscillator; OSC1/OSC2 pins; external oscillator configuration selected by FPR<4:0> bits
010 = LPRC internal low-power RC
001 = FRC internal fast RC
000 = LP crystal oscillator; SOSCI/SOSCO pins
Set to FOS<2:0> values on POR or BOR.

bit 7-6 **POST<1:0>:** Oscillator Postscaler Selection bits
11 = Oscillator postscaler divides clock by 64
10 = Oscillator postscaler divides clock by 16
01 = Oscillator postscaler divides clock by 4
00 = Oscillator postscaler does not alter clock

20.4.1.1 POR with Long Crystal Start-up Time (with FSCM Enabled)

The oscillator start-up circuitry is not linked to the POR circuitry. Some crystal circuits (especially low-frequency crystals) have a relatively long start-up time. Therefore, one or more of the following conditions is possible after the POR timer and the PWRT have expired:

- The oscillator circuit has not begun to oscillate.
- The Oscillator Start-up Timer has not expired (if a crystal oscillator is used).
- The PLL has not achieved a LOCK (if PLL is used).

If the FSCM is enabled and one of the above conditions is true, a clock failure trap occurs. The device automatically switches to the FRC oscillator and the user can switch to the desired crystal oscillator in the trap ISR.

20.4.1.2 Operating without FSCM and PWRT

If the FSCM is disabled and the Power-up Timer (PWRT) is also disabled, then the device exits rapidly from Reset on power-up. If the clock source is FRC, LPRC, ERC or EC, it will be active immediately.

If the FSCM is disabled and the system clock has not started, the device will be in a frozen state at the Reset vector until the system clock starts. From the user's perspective, the device appears to be in Reset until a system clock is available.

20.4.2 BOR: PROGRAMMABLE BROWN-OUT RESET

The BOR (Brown-out Reset) module is based on an internal voltage reference circuit. The main purpose of the BOR module is to generate a device Reset when a brown-out condition occurs. Brown-out conditions are generally caused by glitches on the AC mains (i.e., missing portions of the AC cycle waveform due to bad power transmission lines, or voltage sags due to excessive current draw when a large inductive load is turned on).

The BOR module allows selection of one of the following voltage trip points (see Table 23-11):

- 2.6V-2.71V
- 4.1V-4.4V
- 4.58V-4.73V

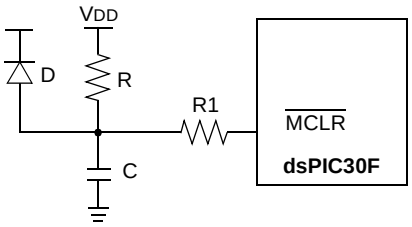
Note:	The BOR voltage trip points indicated here are nominal values provided for design guidance only. Refer to the Electrical Specifications in the specific device data sheet for BOR voltage limit specifications.

A BOR generates a Reset pulse, which resets the device. The BOR selects the clock source based on the device Configuration bit values (FOS<2:0> and FPR<4:0>). Furthermore, if an oscillator mode is selected, the BOR activates the Oscillator Start-up Timer (OST). The system clock is held until OST expires. If the PLL is used, then the clock is held until the LOCK bit (OSCCON<5>) is '1'.

Concurrently, the POR time-out (T_{POR}) and the PWRT time-out (T_{PWRT}) are applied before the internal Reset is released. If T_{PWRT} = 0 and a crystal oscillator is being used, then a nominal delay of T_{FSCM} = 100 μs is applied. The total delay in this case is (T_{POR} + T_{FSCM}).

The BOR status bit (RCON<1>) is set to indicate that a BOR has occurred. The BOR circuit, if enabled, continues to operate while in Sleep or Idle modes and resets the device should V_{DD} fall below the BOR threshold voltage.

FIGURE 20-6: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW V_{DD} POWER-UP)



Note 1: External Power-on Reset circuit is required only if the V_{DD} power-up slope is too slow. The diode D helps discharge the capacitor quickly when V_{DD} powers down.

2: R should be suitably chosen so as to make sure that the voltage drop across R does not violate the device's electrical specifications.

3: R1 should be suitably chosen so as to limit any current flowing into $\overline{MCLR}$ from external capacitor C, in the event of $\overline{MCLR}/V_{PP}$ pin breakdown due to Electrostatic Discharge (ESD), or Electrical Overstress (EOS).

Note:	Dedicated supervisory devices, such as the MCP1XX and MCP8XX, may also be used as an external Power-on Reset circuit.

TABLE 23-5: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Parameter No.	**Typical**	**Max**	**Units**	**Conditions**		
Operating Current (IDD)(1)						
DC31a	2	4	mA	25°C	3.3V	0.128 MIPS LPRC (512 kHz)
DC31b	2	4	mA	85°C		
DC31c	2	4	mA	125°C		
DC31e	4	6	mA	25°C	5V	
DC31f	4	6	mA	85°C		
DC31g	4	6	mA	125°C		
DC30a	6	11	mA	25°C	3.3V	1.8 MIPS FRC (7.37 MHz)
DC30b	6	11	mA	85°C		
DC30c	7	11	mA	125°C		
DC30e	11	16	mA	25°C	5V	
DC30f	11	16	mA	85°C		
DC30g	11	16	mA	125°C		
DC23a	13	20	mA	25°C	3.3V	4 MIPS
DC23b	13	20	mA	85°C		
DC23c	14	20	mA	125°C		
DC23e	22	31	mA	25°C	5V	
DC23f	22	31	mA	85°C		
DC23g	22	31	mA	125°C		
DC24a	27	39	mA	25°C	3.3V	10 MIPS
DC24b	28	39	mA	85°C		
DC24c	28	39	mA	125°C		
DC24e	46	64	mA	25°C	5V	
DC24f	46	64	mA	85°C		
DC24g	46	64	mA	125°C		
DC27d	86	120	mA	25°C	5V	20 MIPS
DC27e	85	120	mA	85°C		
DC27f	85	120	mA	125°C		
DC29a	123	170	mA	25°C	5V	30 MIPS
DC29b	122	170	mA	85°C		

Note 1: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDD measurements are as follows: OSC1 driven with external square wave from rail-to-rail. All I/O pins are configured as inputs and pulled to VDD. $\overline{\text{MCLR}}$ = VDD, WDT, FSCM, LVD and BOR are disabled. CPU, SRAM, program memory and data memory are operational. No peripheral modules are operating.

TABLE 23-31: SPI MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min**	**Typ(2)**	**Max**	**Units**	**Conditions**
SP10	TscL	SCKx Output Low Time(3)	TCY/2	—	—	ns	
SP11	TscH	SCKx Output High Time(3)	TCY/2	—	—	ns	
SP20	TscF	SCKx Output Fall Time(4)	—	—	—	ns	See parameter DO32
SP21	TscR	SCKx Output Rise Time(4)	—	—	—	ns	See parameter DO31
SP30	TdoF	SDOx Data Output Fall Time(4)	—	—	—	ns	See parameter DO32
SP31	TdoR	SDOx Data Output Rise Time(4)	—	—	—	ns	See parameter DO31
SP35	TscH2do, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	—	30	ns	
SP36	TdoV2sc, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	20	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	20	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ" column is at 5V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The minimum clock period for SCKx is 100 ns. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPI pins.

FIGURE 23-16: SPI MODULE SLAVE MODE (CKE = 0) TIMING CHARACTERISTICS

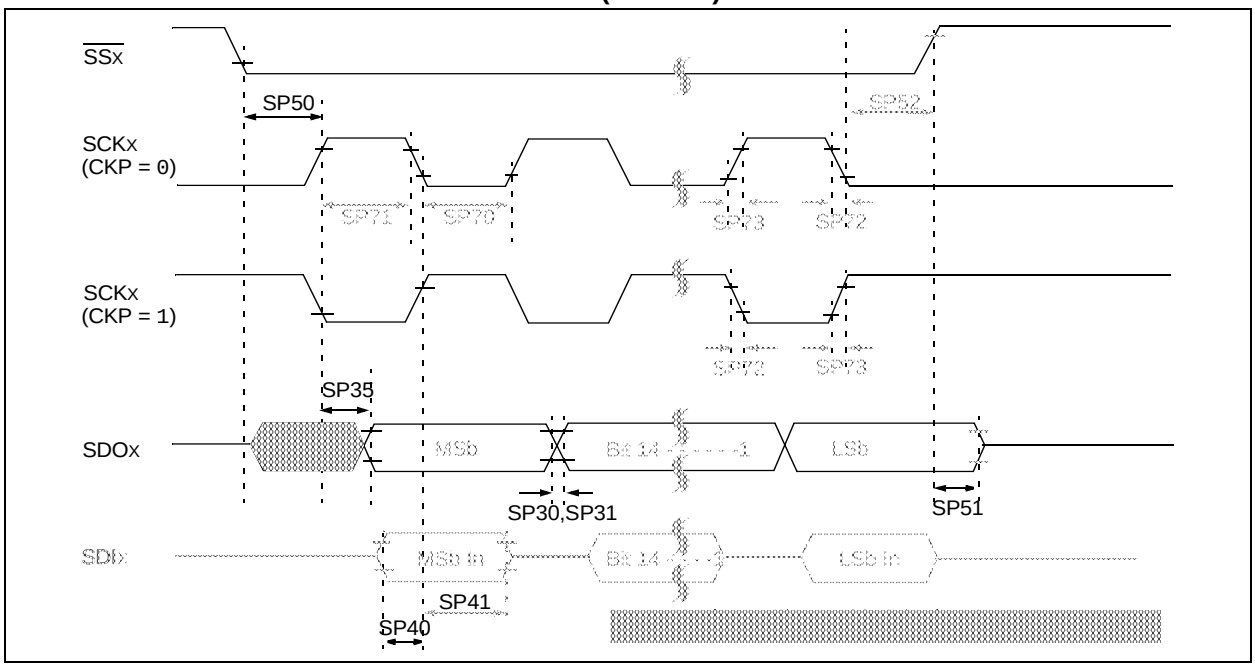
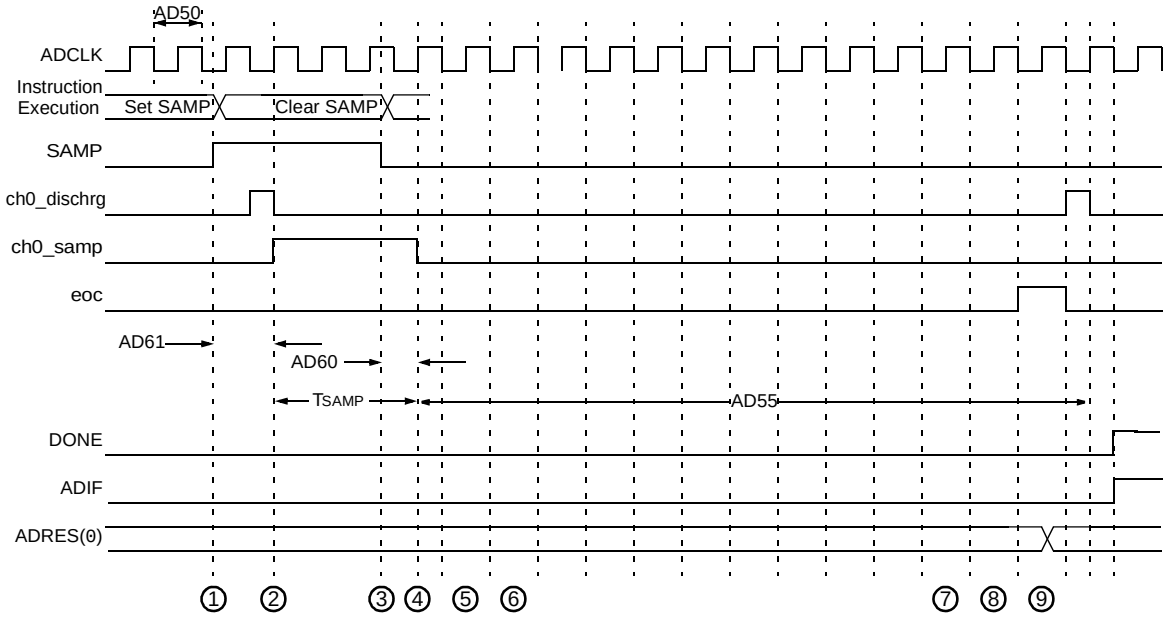


TABLE 23-35: I²C™ BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

AC CHARACTERISTICS			Standard Operating Conditions: 2.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**		**Min**	**Max**	**Units**	**Conditions**
IS10	TLO:SCL	Clock Low Time	100 kHz mode	4.7	—	µs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	1.3	—	µs	Device must operate at a minimum of 10 MHz.
			1 MHz mode(1)	0.5	—	µs	
IS11	THI:SCL	Clock High Time	100 kHz mode	4.0	—	µs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	µs	Device must operate at a minimum of 10 MHz
			1 MHz mode(1)	0.5	—	µs	
IS20	TF:SCL	SDA and SCL Fall Time	100 kHz mode	—	300	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode(1)	—	100	ns	
IS21	TR:SCL	SDA and SCL Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode(1)	—	300	ns	
IS25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	
			400 kHz mode	100	—	ns	
			1 MHz mode(1)	100	—	ns	
IS26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	µs	
			1 MHz mode(1)	0	0.3	µs	
IS30	TSU:STA	Start Condition Setup Time	100 kHz mode	4.7	—	µs	Only relevant for Repeated Start condition
			400 kHz mode	0.6	—	µs	
			1 MHz mode(1)	0.25	—	µs	
IS31	THD:STA	Start Condition Hold Time	100 kHz mode	4.0	—	µs	After this period, the first clock pulse is generated
			400 kHz mode	0.6	—	µs	
			1 MHz mode(1)	0.25	—	µs	
IS33	TSU:STO	Stop Condition Setup Time	100 kHz mode	4.7	—	µs	
			400 kHz mode	0.6	—	µs	
			1 MHz mode(1)	0.6	—	µs	
IS34	THD:STO	Stop Condition Hold Time	100 kHz mode	4000	—	ns	
			400 kHz mode	600	—	ns	
			1 MHz mode(1)	250		ns	
IS40	TAA:SCL	Output Valid From Clock	100 kHz mode	0	3500	ns	
			400 kHz mode	0	1000	ns	
			1 MHz mode(1)	0	350	ns	
IS45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	µs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
			1 MHz mode(1)	0.5	—	µs	
IS50	CB	Bus Capacitive Loading		—	400	pF	

Note 1: Maximum pin capacitance = 10 pF for all I²C pins (for 1 MHz mode only).

FIGURE 23-23: 12-BIT A/D CONVERSION TIMING CHARACTERISTICS (ASAM = 0, SSRC = 000)



1. - Software sets ADCON. SAMP to start sampling.
2. - Sampling starts after discharge period.
   TSAMP is described in **Section 18. "12-bit A/D Converter"** of the *dsPIC30F Family Reference Manual* (DS70046).
3. - Software clears ADCON. SAMP to start conversion.
4. - Sampling ends, conversion sequence starts.
5. - Convert bit 11.
6. - Convert bit 10.
7. - Convert bit 1.
8. - Convert bit 0.
9. - One TAD for end of conversion.