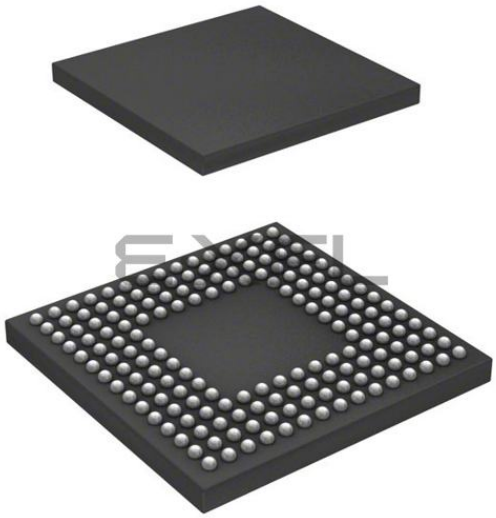

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Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LFBGA
Supplier Device Package	176-LFBGA (13x13)
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7.2.16 Port G

(1) PG7/ExSCLB/$\overline{\text{ExIRQ15}}$

The pin function is switched as shown below according to the combination of the register setting of PTCNT1 and the PG7DDR bit. When the ISS15 bit in ISSR16 is set to 1 and the IRQ15E bit in IER16 of the interrupt controller is set to 1, this pin can be used as the $\overline{\text{ExIRQ15}}$ input pin.

		Setting	
		PTCNT1	I/O Port
Module Name	Pin Function	ExSCLB_OE	PG7DDR
PTCNT1	ExSCLB input/output	1	—
I/O port	PG7 output	0	1
	PG7 input (initial setting)	0	0

Note: The output format for ExSCLB is NMOS output only, and direct bus drive is possible. When this pin is used as the PG7 output pin, the output format is NMOS push-pull.

(2) PG6/ExSDAB/$\overline{\text{ExIRQ14}}$

The pin function is switched as shown below according to the combination of the register setting of PTCNT1 and the PG6DDR bit. When the ISS14 bit in ISSR16 is set to 1 and the IRQ14E bit in IER16 of the interrupt controller is set to 1, this pin can be used as the $\overline{\text{ExIRQ14}}$ input pin.

		Setting	
		PTCNT1	I/O Port
Module Name	Pin Function	ExSDAB_OE	PG6DDR
PTCNT1	ExSDAB input/output	1	—
I/O port	PG6 output	0	1
	PG6 input (initial setting)	0	0

Note: The output format for ExSDAB is NMOS output only, and direct bus drive is possible. When this pin is used as the PG6 output pin, the output format is NMOS push-pull.

Section 8 8-Bit PWM Timer (PWMU)

This LSI has two channels of 8-bit PWM timers, A and B (PWMU_A and PWMU_B). Each PWMU outputs 6 PWM waveforms. Each of the PWM channels of a PWMU can operate independently. A PWMU allows long-period PWM outputs for six channels in 8-bit single-pulse mode and for three channels in 16-bit single-pulse mode. In addition, PWM outputs at a high carrier frequency are available in 8-bit pulse division mode. Connecting a low-pass filter externally to the LSI allows the PWMU to be used as an 8-bit D/A converter.

8.1 Features

- Selectable from four types of counter input clock
  Selection of four internal clock signals (ϕ, ϕ/2, ϕ/4, and ϕ/8)
- Independent operation and variable cycle for each channel
  Cascaded connection of two channels is possible.
  Operation of channel 1 (higher order) and channel 0 (lower order) as a 16-bit single-pulse PWM timer
  Operation of channel 3 (higher order) and channel 2 (lower order) as a 16-bit single-pulse PWM timer
  Operation of channel 5 (higher order) and channel 4 (lower order) as a 16-bit single-pulse PWM timer
- 8-bit single pulse mode
  Operates at a maximum carrier frequency of 78.1 kHz (at 20 MHz operation)
  Pulse output settable with a duty cycle from 0/255 to 255/255
  PWM output enable/disable control, and selection of direct or inverted PWM output
- 16-bit single pulse mode
  Two channels are cascade-connected for operation in this mode.
  Operates at a maximum carrier frequency of 305.1 Hz (at 20 MHz operation)
  Pulse output settable with a duty cycle from 0/65535 to 65535/65535
  PWM output enable/disable control, and selection of direct or inverted PWM output
- 8-bit pulse division mode
  Operable at a maximum carrier frequency of 1.25 MHz (at 20 MHz operation)
  Pulse output settable with a duty cycle from 0/16 to 15/16
  PWM output enable/disable control, and selection of direct or inverted PWM output

8.3.3 PWM Control Register C (PWMCONC)

PWMCONC selects the PWM count mode and operating mode for each channel.

Bit	Bit Name	Initial Value	R/W	Description
7	—	0	R/W	Reserved The initial value should not be changed.
6	CNTMD01	0	R/W	Channels 0 and 1 Counter Select 0: Channels 0 and 1 are in 8-bit counter operation. 1: Channels 0 and 1 are in 16-bit counter operation (Upper: channel 1, lower: channel 0). Note: When the 16-bit counter is selected, specify single pulse mode.
5	PWMSL5	0	R/W	Channel 5 Operating Mode Select 0: Single-pulse mode 1: Pulse division mode (Specify 8-bit counter mode.)
4	PWMSL4	0	R/W	Channel 4 Operating Mode Select 0: Single pulse mode 1: Pulse division mode (Specify 8-bit counter mode.)
3	PWMSL3	0	R/W	Channel 3 Operating Mode Select 0: Single pulse mode 1: Pulse division mode (Specify 8-bit counter mode.)
2	PWMSL2	0	R/W	Channel 2 Operating Mode Select 0: Single pulse mode 1: Pulse division mode (Specify 8-bit counter mode.)
1	PWMSL1	0	R/W	Channel 1 Operating Mode Select 0: Single pulse mode 1: Pulse division mode (Specify 8-bit counter mode.)
0	PWMSL0	0	R/W	Channel 0 Operating Mode Select 0: Single pulse mode 1: Pulse division mode (Specify 8-bit counter mode.)

(b) Examples of waveform output operation

Figure 10.10 shows an example of 0 output/1 output. In this example TCNT has been designated as a free-running counter, and settings have been made so that 1 is output by compare match A, and 0 is output by compare match B. When the set level and the pin level coincide, the pin level does not change.

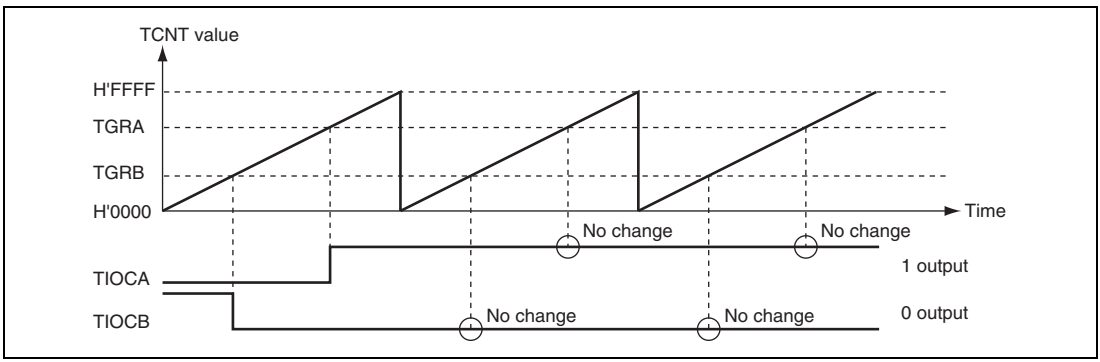

Figure 10.10 Example of 0 Output/1 Output Operation

Figure 10.11 shows an example of toggle output.

In this example TCNT has been designated as a periodic counter (with counter clearing performed by compare match B), and settings have been made so that output is toggled by both compare match A and compare match B.

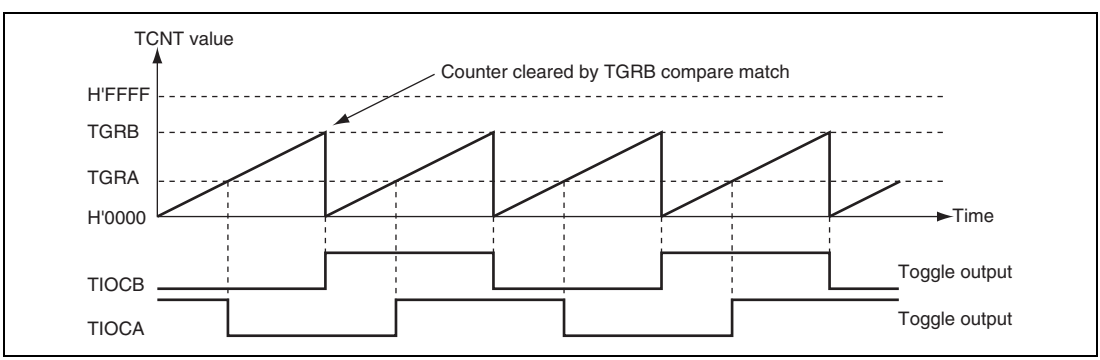

Figure 10.11 Example of Toggle Output Operation

13.5.6 Timing of Overflow Flag (OVF) Setting

The OVF bit in TCSR is set to 1 when the TCNT overflows (changes from H'FF to H'00). Figure 13.10 shows the timing of OVF flag setting.

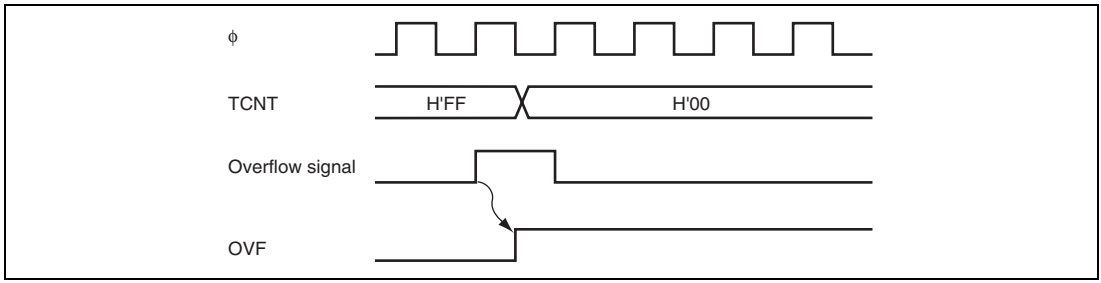

Figure 13.10 Timing of OVF Flag Setting

15.3.5 Serial Mode Register (SMR)

SMR is used to set the SCI's serial transfer format and select the baud rate generator clock source. Some bits in SMR have different functions in normal mode and smart card interface mode. The CPU can always read SMR. The CPU can write to SMR only at the initial settings; do not have the CPU write to SMR in transmission, reception, and simultaneous data transmission and reception.

- Bit Functions in Normal Serial Communication Interface Mode (when SMIF in SCMR = 0)

Bit	Bit Name	Initial Value	R/W	Description
7	C/$\overline{A}$	0	R/W	Communication Mode 0: Asynchronous mode 1: Clocked synchronous mode
6	CHR	0	R/W	Character Length (enabled only in asynchronous mode) 0: Selects 8 bits as the data length. 1: Selects 7 bits as the data length. LSB-first is fixed and the MSB of TDR is not transmitted in transmission. In clocked synchronous mode, a fixed data length of 8 bits is used.
5	PE	0	R/W	Parity Enable (enabled only in asynchronous mode) When this bit is set to 1, the parity bit is added to transmit data before transmission, and the parity bit is checked in reception. For a multiprocessor format, parity bit addition and checking are not performed regardless of the PE bit setting.
4	O/$\overline{E}$	0	R/W	Parity Mode (enabled only when the PE bit is 1 in asynchronous mode) 0: Selects even parity. 1: Selects odd parity.
3	STOP	0	R/W	Stop Bit Length (enabled only in asynchronous mode) Selects the stop bit length in transmission. 0: 1 stop bit 1: 2 stop bits In reception, only the first stop bit is checked. If the second stop bit is 0, it is treated as the start bit of the next transmit frame.

16.4.1 Determination of Signal Type by Low/High-Level Period

The signal type is determined by low/high-level period that is specified in the HHMIN, HHMAX, HLMIN, HLMAX, DT1MIN, DT1MAX, DT0MIN, DT0MAX, RMIN, and RMAX registers. Calculating formula for specified time, setting examples of each maximum/minimum value register during the specified time, and use for each register are described as follows. The symbols in table 16.4 correspond to the ones used in the figure 16.3 to figure 16.5.

$S.E = M (N + 1)/T$

S: Specified time of the NEC format

E: Error from the NEC format

T: Frequency of the reference clock (Hz) set by the CLK1 and CLK0 bits in CCR1 (ϕ, $\phi/2$, $\phi/4$, or ϕsub)

N: Setting value in BRR ($0 \leq N \leq 255$)

M: Value in the maximum/minimum value setting register

Table 17.5 SCIF Output Setting

Bit 3 in HICR5	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**
Bit 7 in SCIFCR	**0**	**0**	**1**	**1**	**0**	**0**	**1**	**1**
Bit 6 in SCIFCR	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**
PB7 and PB5 pins	PORT	PORT	SCIF	PORT	SCIF	PORT	SCIF	PORT
P50 pin	PORT	PORT	SCIF	SCIF	SCIF	SCIF	SCIF	SCIF

Note: P51, PB2 to PB4, and PB6 are input to the SCIF even when the outputs on the PB7, PB5, and P50 pins are set to PORT.

Bit	Bit Name	Initial Value	R/W	Description
5	MST	0	R/W	[MST clearing conditions]
4	TRS	0	R/W	1. When 0 is written by software 2. When lost in bus contention in I²C bus format master mode [MST setting conditions] 1. When 1 is written by software (for MST clearing condition 1) 2. When 1 is written in MST after reading MST = 0 (for MST clearing condition 2) [TRS clearing conditions] 1. When 0 is written by software (except for TRS setting condition 3) 2. When 0 is written in TRS after reading TRS = 1 (for TRS setting condition 3) 3. When lost in bus contention in I²C bus format master mode [TRS setting conditions] 1. When 1 is written by software (except for TRS clearing condition 3) 2. When 1 is written in TRS after reading TRS = 0 (for TRS clearing condition 3) 3. When 1 is received as the R/$\overline{W}$ bit after the first frame address matching in I²C bus format slave mode
3	ACKE	0	R/W	Acknowledge Bit Decision and Selection 0: The value of the acknowledge bit is ignored, and continuous transfer is performed. The value of the received acknowledge bit is not indicated by the ACKB bit in ICSR, which is always 0. 1: If the received acknowledge bit is 1, continuous transfer is halted. Depending on the receiving device, the acknowledge bit may be significant, in indicating completion of processing of the received data, for instance, or may be fixed at 1 and have no significance.

The master mode reception procedure and operations are described below.

1. Clear the TRS bit in ICCR to 0 to switch from transmit mode to receive mode.
   Clear the ACKB bit in ICSR to 0 (acknowledge data setting).
   Clear the IRIC flag to 0 to determine the end of reception.
   Go to step [6] to halt reception operation if the first frame is the last receive data.
2. When ICDR is read (dummy data read), reception is started, the receive clock is output in synchronization with the internal clock, and data is received. (Data from the SDA pin is sequentially transferred to ICDRS in synchronization with the rise of the receive clock pulses.)
3. The master device drives SDA low to return the acknowledge data at the 9th receive clock pulse. The receive data is transferred from ICDRS to ICDRR at the rise of the 9th clock pulse, setting the ICDRF, IRIC, and IRTR flags to 1. If the IEIC bit has been set to 1, an interrupt request is sent to the CPU.
   The master device drives SCL low from the fall of the 9th receive clock pulse to the ICDR data reading.
4. Clear the IRIC flag to determine the next interrupt.
   Go to step [6] to halt reception operation if the next frame is the last receive data.
5. Read ICDR receive data. This clears the ICDRF flag to 0. The master device outputs the receive clock continuously to receive the next data.

Data can be received continuously by repeating steps [3] to [5].

6. Set the ACKB bit to 1 so as to return the acknowledge data for the last reception.
7. Read ICDR receive data. This clears the ICDRF flag to 0. The master device outputs the receive clock to receive data.
8. When one frame of data has been received, the ICDRF, IRIC, and IRTR flags are set to 1 at the rise of the 9th receive clock pulse.
9. Clear the IRIC flag to 0.
10. Read ICDR receive data after setting the TRS bit. This clears the ICDRF flag to 0.
11. Clear the BBSY bit and SCP bit to 0 in ICCR. This changes SDA from low to high when SCL is high, and generates the stop condition.

19.3 Register Descriptions

The PS2 has the following registers for each channel.

Table 19.2 Register Configuration

Channel	Register Name	Abbreviation	R/W	Initial Value	Address	Data Bus Width
Channel 0	Keyboard control register 1_0	KBCR1_0	R/W	H'00	H'FEC0	8
	Keyboard control register 2_0	KBCR2_0	R/W	H'F0	H'FEDB	8
	Keyboard buffer transmit data register_0	KBTR_0	R/W	H'FF	H'FEC1	8
	Keyboard control register H_0	KBCRH_0	R/W	H'70	H'FED8	8
	Keyboard control register L_0	KBCRL_0	R/W	H'70	H'FED9	8
	Keyboard data buffer register_0	KBBR_0	R	H'00	H'FEDA	8
Channel 1	Keyboard control register 1_1	KBCR1_1	R/W	H'00	H'FEC2	8
	Keyboard control register 2_1	KBCR2_1	R/W	H'F0	H'FEDF	8
	Keyboard buffer transmit data register_1	KBTR_1	R/W	H'FF	H'FEC3	8
	Keyboard control register H_1	KBCRH_1	R/W	H'70	H'FEDC	8
	Keyboard control register L_1	KBCRL_1	R/W	H'70	H'FEDD	8
	Keyboard data buffer register_1	KBBR_1	R	H'00	H'FEDE	8
Channel 2	Keyboard control register 1_2	KBCR1_2	R/W	H'00	H'FEC4	8
	Keyboard control register 2_2	KBCR2_2	R/W	H'F0	H'FEE3	8
	Keyboard buffer transmit data register_2	KBTR_2	R/W	H'FF	H'FEC5	8
	Keyboard control register H_2	KBCRH_2	R/W	H'70	H'FEE0	8
	Keyboard control register L_2	KBCRL_2	R/W	H'70	H'FEE1	8
	Keyboard data buffer register_2	KBBR_2	R	H'00	H'FEE2	8
Channel 3	Keyboard control register 1_3	KBCR1_3	R/W	H'00	H'FED2	8
	Keyboard control register 2_3	KBCR2_3	R/W	H'F0	H'FFE3	8
	Keyboard buffer transmit data register_3	KBTR_3	R/W	H'FF	H'FED3	8
	Keyboard control register H_3	KBCRH_3	R/W	H'70	H'FFE0	8
	Keyboard control register L_3	KBCRL_3	R/W	H'70	H'FFE1	8
	Keyboard data buffer register_3	KBBR_3	R	H'00	H'FFE2	8

Bit	Bit Name	Initial Value	R/W		Description
			Slave	Host	
0	IRQ1E1	0	R/W	—	Host IRQ1 Interrupt Enable 1 Enables or disables a host HIRQ1 interrupt request when OBF1 is set by an ODR1 write. 0: HIRQ1 interrupt request by OBF1 and IRQ1E1 is disabled [Clearing conditions] • Writing 0 to IRQ1E1 • LPC hardware reset, LPC software reset • Clearing OBF1 to 0 1: HIRQ1 interrupt request by setting OBF1 to 1 is enabled [Setting condition] Writing 1 after reading IRQ1E1 = 0

20.5.2 SMI, HIRQ1, HIRQ3, HIRQ4, HIRQ5, HIRQ6, HIRQ7, HIRQ8, HIRQ9, HIRQ10, HIRQ11, HIRQ12, HIRQ13, HIRQ14, and HIRQ15

The LPC interface can request 15 kinds of host interrupt by means of SERIRQ. HIRQ1 and HIRQ12 are used on LPC channel 1 and the SCIF, while SMI, HIRQ6, HIRQ9, HIRQ10, and HIRQ11 can be requested from LPC channel 2, 3, 4 or SCIF. HIRQ3, HIRQ4, HIRQ5, HIRQ7, HIRQ8, HIRQ13, HIRQ14, and HIRQ15 are only for the SCIF.

There are two ways of clearing a host interrupt request when the LPC channels are used.

When the IEDIR bit in SIRQCR is cleared to 0, host interrupt sources and LPC channels are all linked to the host interrupt request enable bits. When the OBF flag is cleared to 0 by a read of ODR or TWR15 by the host in the corresponding LPC channel, the corresponding host interrupt enable bit is automatically cleared to 0, and the host interrupt request is cleared.

When the IEDIR bit is set to 1 in SIRQCR, a host interrupt is requested by the only upon the host interrupt enable bits. The host interrupt enable bit is not cleared when OBF is cleared. Therefore, SMIE1, SMIE2, SMIE3A and SMIE3B, SMIE4, IRQ6En, IRQ9En, IRQ10En, and IRQ11En lose their respective functional differences. In order to clear a host interrupt request, it is necessary to clear the host interrupt enable bit. (n = 2 to 4.)

When the SCIF channels are used, clearing the DDCD bit in FMSR of the SCIF clears a host interrupt request.

Table 20.10 summarizes the methods of setting and clearing these bits when the LPC channels are used, and table 20.11 summarizes the methods of setting and clearing these bits when the SCIF channels are used. Figure 20.8 shows the processing flowchart.

Bit	Bit Name	Initial Value	R/W	Description
2	WD	—	R/W	Write Data Address Detect When an address not in the flash memory area is specified as the start address of the storage destination for the program data, an error occurs. 0: Setting of the start address of the storage destination for the program data is normal 1: Setting of the start address of the storage destination for the program data is abnormal
1	WA	—	R/W	Write Address Error Detect When the following items are specified as the start address of the programming destination, an error occurs. • An area other than flash memory • The specified address is not aligned with the 128-byte boundary (lower eight bits of the address are other than H'00 and H'80) 0: Setting of the start address of the programming destination is normal 1: Setting of the start address of the programming destination is abnormal
0	SF	—	R/W	Success/Fail Returns the programming result. 0: Programming has ended normally (no error) 1: Programming has ended abnormally (error occurs)

(3) Flash Program/Erase Frequency Parameter (FPEFEQ: General Register ER0 of CPU)

FPEFEQ sets the operating frequency of the CPU. The operating frequency available in this LSI ranges from 8 MHz to 20 MHz.

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	—	—	Unused These bits should be cleared to 0.
15 to 0	F15 to F0	—	R/W	Frequency Set These bits set the operating frequency of the CPU. The setting value must be calculated as follows: 1. Round off the operating frequency expressed in MHz unit at the third decimal place to make it into two decimal places. 2. Multiply the rounded number by 100 and convert the result into binary and write it to FPEFEQ (general register ER0). For example, when the operating frequency of the CPU is 20.000 MHz, the setting value is as follows: 1. Round 20.000 off at the third decimal place as 20.00. 2. Convert 20.00 × 100 = 2000 into a binary number and set B'0000 0111 1101 0000 (H'07D0) in ER0.

12. The return value in the programming program, the FPFR parameter is determined.
13. Determine whether programming of the necessary data has finished. If more than 128 bytes of data are to be programmed, update the FMPAR and FMPDR parameters in 128-byte units, and repeat steps 11 to 14. Increment the programming destination address by 128 bytes and update the programming data pointer correctly. If an address which has already been programmed is written to again, not only will a programming error occur, but also flash memory will be damaged.
14. After programming finishes, clear FKEY and specify software protection. If this LSI is restarted by a reset immediately after programming has finished, secure the reset input period (period of $\overline{\text{RES}}$ = 0) of at least 100 μs.

(3) Erasing Procedure in User Program Mode

The procedures for download of the on-chip program, initialization, and erasing are shown in figure 24.13.

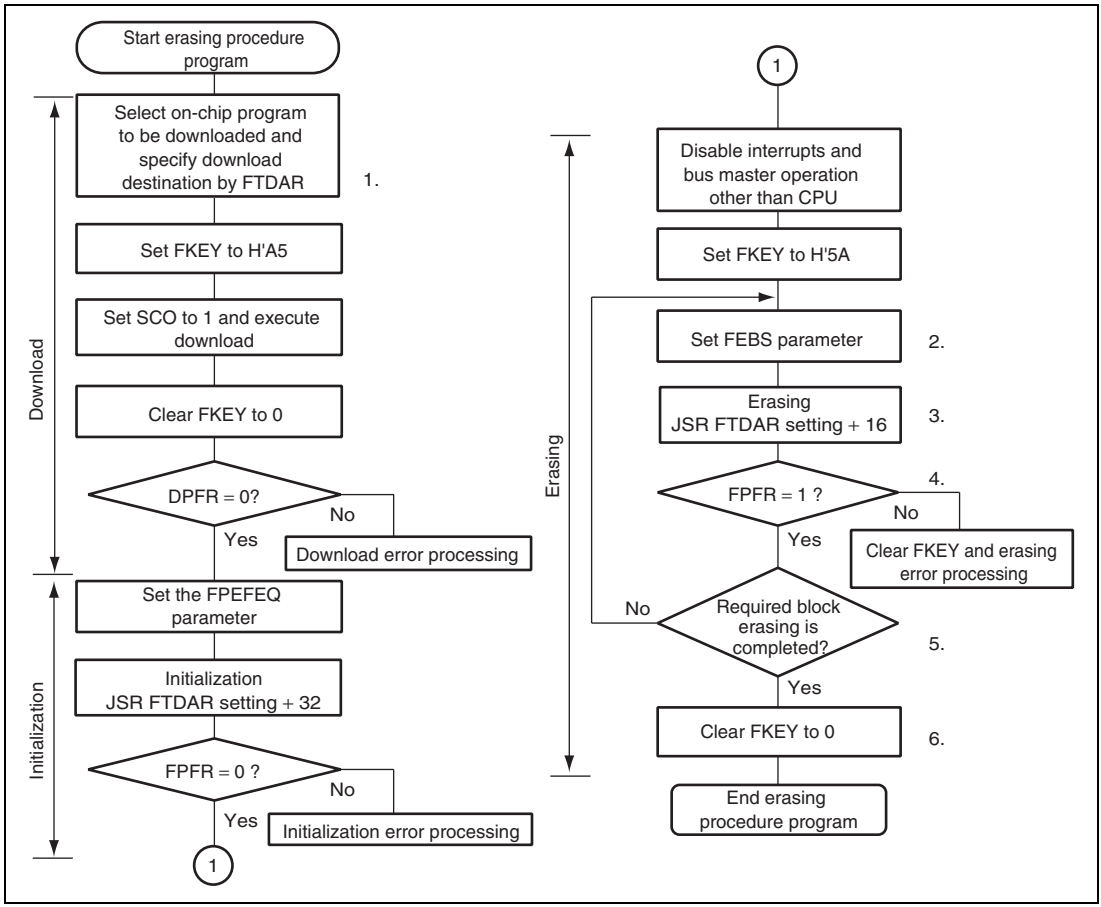

Figure 24.13 Erasing Procedure in User Program Mode

The procedure program must be executed in an area other than the user MAT to be erased. Setting the SCO bit in FCCS to 1 to request download must be executed in the on-chip RAM. The area that can be executed in the steps of the procedure program (on-chip RAM and user MAT) is shown in section 24.8.4, Storable Areas for On-Chip Program and Program Data. For the downloaded on-chip program area, see figure 24.11.

3. Programming/erasing state

   Programming and erasure by the boot program take place in this state. The boot program is made to transfer the programming/erasing programs to the on-chip RAM by commands from the host. Sum checks and blank checks are executed by sending these commands from the host.

These boot program states are shown in figure 24.18.

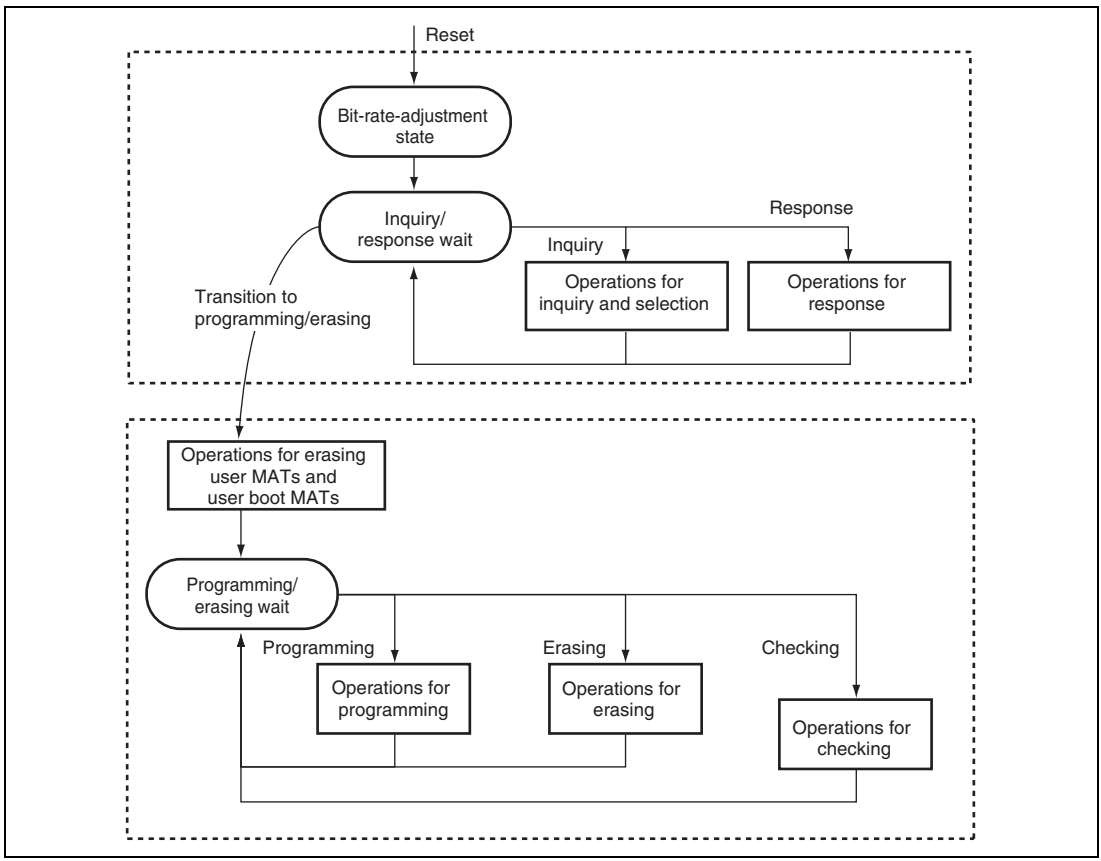

Figure 24.18 Boot Program States

Module	Register Abbreviation	Number of Bits	Address	Data Bus Width	Access States
TDP_0	TDPCNT_0	8	H'FB40	8	2
TDP_0	TDPWDMX_0	8	H'FB42	8	2
TDP_0	TDPWDMN_0	8	H'FB44	8	2
TDP_0	TDPPDMX_0	8	H'FB46	8	2
TDP_0	TDPICR_0	8	H'FB48	8	2
TDP_0	TDPICRF_0	8	H'FB8A	8	2
TDP_0	TDPCSR_0	8	H'FB8C	8	2
TDP_0	TDPCR1_0	8	H'FB4D	8	2
TDP_0	TDPIER_0	8	H'FB4E	8	2
TDP_0	TDPCR2_0	8	H'FB4F	8	2
TDP_0	TDPPDMN_0	16	H'FB50	16	2
TDP_1	TDPCNT_1	16	H'FB60	16	2
TDP_1	TDPWDMX_1	16	H'FB62	6	2
TDP_1	TDPWDMN_1	16	H'FB64	16	2
TDP_1	TDPPDMX_1	16	H'FB66	16	2
TDP_1	TDPICR_1	16	H'FB68	16	2
TDP_1	TDPICRF_1	16	H'FB6A	16	2
TDP_1	TDPCSR_1	8	H'FB6C	8	2
TDP_1	TDPCR1_1	8	H'FB6D	8	2
TDP_1	TDPIER_1	8	H'FB6E	8	2
TDP_1	TDPCR2_1	8	H'FB6F	8	2
TDP_1	TDPPDMN_1	16	H'FB70	16	2
TDP_2	TDPCNT_2	16	H'FB80	16	2
TDP_2	TDPWDMX_2	16	H'FB82	16	2
TDP_2	TDPWDMN_2	16	H'FB84	16	2
TDP_2	TDPPDMX_2	16	H'FB86	16	2
TDP_2	TDPICR_2	16	H'FB88	16	2
TDP_2	TDPICRF_2	16	H'FB8A	16	2
TDP_2	TDPCSR_2	8	H'FB8C	8	2
TDP_2	TDPCR1_2	8	H'FB8D	8	2
TDP_2	TPDIER_2	8	H'FB8E	8	2