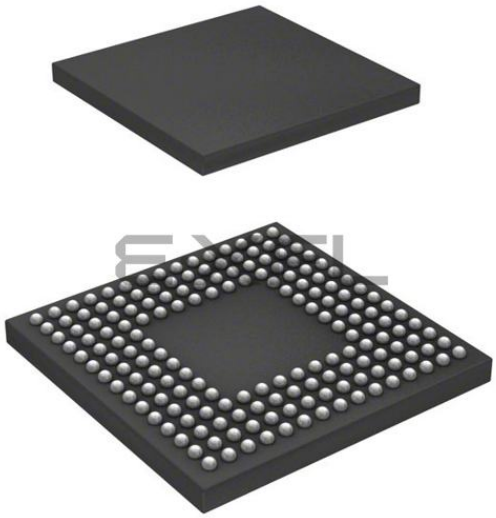
Renesas Electronics America Inc - DF2117RVBG20V Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2600
Core Size	16-Bit
Speed	20MHz
Connectivity	FIFO, I²C, LPC, SCI, SmartCard
Peripherals	POR, PWM, WDT
Number of I/O	128
Program Memory Size	160KB (160K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LFBGA
Supplier Device Package	176-LFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2117rvbg20v

Bit	Bit Name	Initial Value	R/W	Description
1	V	Undefined	R/W	Overflow Flag Set to 1 when an arithmetic overflow occurs, and cleared to 0 at other times.
0	C	Undefined	R/W	Carry Flag Set to 1 when a carry occurs, and cleared to 0 otherwise. Used by: • Add instructions, to indicate a carry • Subtract instructions, to indicate a borrow • Shift and rotate instructions, to indicate a carry The carry flag is also used as a bit accumulator by bit manipulation instructions.

2.4.5 Multiply-Accumulate Register (MAC)

This 64-bit register stores the results of multiply-and-accumulate operations. It consists of two 32-bit registers denoted MACH and MACL. The lower 10 bits of MACH are valid; the upper bits are a sign extension.

2.4.6 Initial Values of CPU Registers

Reset exception handling loads the CPU's program counter (PC) from the vector table, clears the trace bit in EXR to 0, and sets the interrupt mask bits in CCR and EXR to 1. The other CCR bits and the general registers are not initialized. In particular, the stack pointer (ER7) is not initialized. The stack pointer should therefore be initialized by an MOV.L instruction executed immediately after a reset.

(2) P51/FRxD

The pin function is switched as shown below according to the SCIFOE1 bit in SCIFCR of the SCIF and the SCIFE bit in HICR5 of the SCIF, and the P51DDR bit.

SCIFENABLE = 1: SCIFOE1 + SCIFE

		Setting	
		Logical Expression	I/O Port
Module Name	Pin Function	SCIFENABLE	P51DDR
SCIF	FRxD input	1	—
I/O port	P51 output	0	1
	P51 input (initial setting)	0	0

(3) P50/FTxD

The pin function is switched as shown below according to the SCIFOE1 bit in SCIFCR of the SCIF, the SCIFE bit in HICR5, and the P50DDR bit.

SCIFENABLE = 1: SCIFOE1 + SCIFE

		Setting	
		Logical Expression	I/O Port
Module Name	Pin Function	SCIFENABLE	P50DDR
SCIF	FTxD output	1	—
I/O port	P50 output	0	1
	P50 input (initial setting)	0	0

(2) 16-Bit Single Pulse Mode

When 16-bit single pulse mode is selected, PWMPRE0, PWMPRE2, and PWMPRE4 are valid. The settings of PWMPRE1, PWMPRE3, and PWMPRE5 are invalid.

PWM cycle = [65535 × (n + 1)] / internal clock frequency (0 ≤ n ≤ 255)

Table 8.4 Resolution, PWM Conversion Period, and Carrier Frequency (16-Bit Counter Operation) when ϕ = 20 MHz

Internal Clock Frequency	Resolution	PWM Conversion Period		Carrier Frequency Single Pulse Mode	
		Min.	Max.	Min.	Max.
ϕ	50 ns	3.3 ms	838.9 ms	1.2 Hz	305.1 Hz
ϕ/2	100 ns	6.5 ms	1.7 s	0.6 Hz	152.6 Hz
ϕ/4	200 ns	13.1 ms	3.4 s	0.3 Hz	76.3 Hz
ϕ/8	400 ns	26.2 ms	6.7 s	0.15 Hz	38.1 Hz

(3) 8-Bit Pulse Division Mode

PWM cycle = [16 × (n + 1)] / internal clock frequency (0 ≤ n ≤ 255)

PWM conversion cycle = [256 × (n + 1)] / internal clock frequency (0 ≤ n ≤ 255)

Table 8.5 Resolution, PWM Conversion Period, and Carrier Frequency when ϕ = 20 MHz (at 8-bit counter operation)

Internal Clock Frequency	Resolution	PWM Conversion Period		Carrier Frequency (1/PWM cycle)	
		Min.	Max.	Min.	Max.
ϕ	50 ns	12.8 μs	3.3ms	4882.8Hz	1250.0 kHz
ϕ/2	100 ns	25.6 μs	6.6ms	2441.4Hz	625.0 kHz
ϕ/4	200 ns	51.2 μs	13.1ms	1220.7Hz	312.5 kHz
ϕ/8	400 ns	102.4 μs	26.2ms	610.4Hz	156.3 kHz

When the PWMnE bit (n = 0 to 5) in PWMCONB is set to 1, the PWMU outputs pulses that start with a high level. The updated PWMREG value is written in REGLAT, and the updated PWMPRE value is written in PRELAT.

When the REGLAT value is less than the duty counter value, the PWMU outputs a high level (when direct output is selected). At each PWM clock timing, the duty counter is incremented. When the clock generator counter is H'00, the PWM clock is generated by decrementing the PRELAT value.

Figure 8.4 shows an example of duty counter and clock generator counter operation.

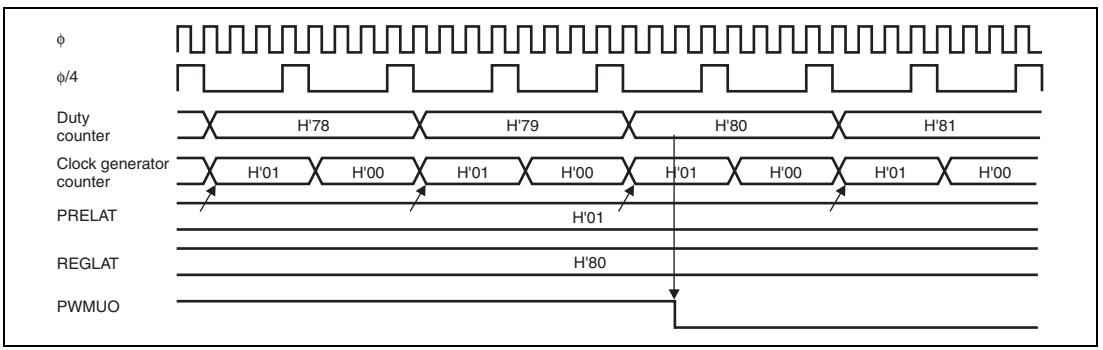


Figure 8.4 Example of Duty Counter and Clock Generator Counter Operation (When PWMPRE = H'01 and PWMREG = H'80 with φ/4 Selected as Count Clock Source)

The following shows the duty counter value and PWMU output timing.

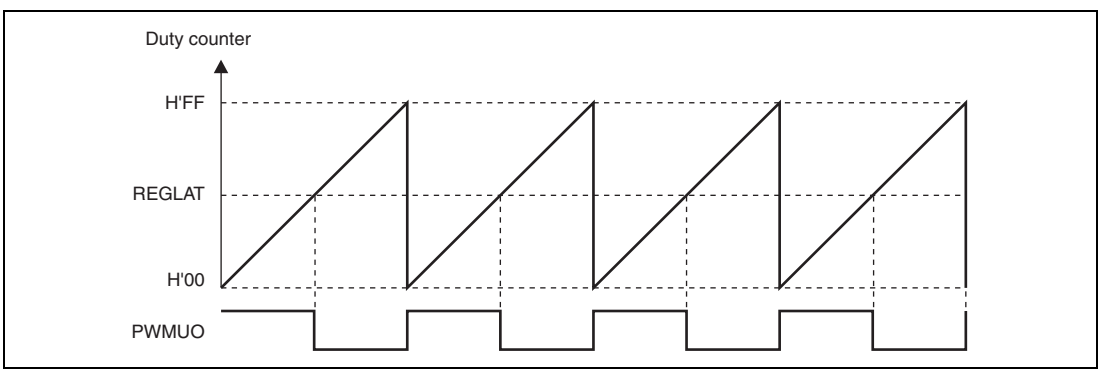


Figure 8.5 Duty Counter Value and PWMU Output Timing

Table 10.11 TIORH_0 (channel 0)

				Description	
Bit 3 IOA3	**Bit 2 IOA2**	**Bit 1 IOA1**	**Bit 0 IOA0**	**TGRA_0 Function**	**TIOCA0 Pin Function**
0	0	0	0	Output compare register	Output disabled
			1		Initial output is 0 output 0 output at compare match
		1	0		Initial output is 0 output 1 output at compare match
			1		Initial output is 0 output Toggle output at compare match
	1	0	0		Output disabled
			1		Initial output is 1 output 0 output at compare match
		1	0		Initial output is 1 output 1 output at compare match
			1		Initial output is 1 output Toggle output at compare match
1	0	0	0	Input capture register	Capture input source is TIOCA0 pin Input capture at rising edge
			1		Capture input source is TIOCA0 pin Input capture at falling edge
		1	×		Capture input source is TIOCA0 pin Input capture at both edges
	1	×	×		Setting prohibited

[Legend]

×: Don't care

Table 10.16 TIOR_2 (channel 2)

				Description	
Bit 7 IOB3	**Bit 6 IOB2**	**Bit 5 IOB1**	**Bit 4 IOB0**	**TGRB_2 Function**	**TIOCB2 Pin Function**
0	0	0	0	Output compare register	Output disabled
			1		Initial output is 0 output 0 output at compare match
		1	0		Initial output is 0 output 1 output at compare match
			1		Initial output is 0 output Toggle output at compare match
	1	0	0		Output disabled
			1		Initial output is 1 output 0 output at compare match
		1	0		Initial output is 1 output 1 output at compare match
			1		Initial output is 1 output Toggle output at compare match
1	×	0	0	Input capture register	Capture input source is TIOCB2 pin Input capture at rising edge
			1		Capture input source is TIOCB2 pin Input capture at falling edge
		1	×		Capture input source is TIOCB2 pin Input capture at both edges

[Legend]

×: Don't care

10.3.4 Timer Interrupt Enable Register (TIER)

The TIER registers control enabling or disabling of interrupt requests for each channel. The TPU has three TIER registers, one for each channel.

Bit	Bit Name	Initial value	R/W	Description
7	TTGE	0	R/W	A/D Conversion Start Request Enable Enables or disables generation of A/D conversion start requests by TGRA input capture/compare match. 0: A/D conversion start request generation disabled 1: A/D conversion start request generation enabled
6	—	1	R	Reserved This bit is always read as 1 and cannot be modified.
5	TCIEU	0	R/W	Underflow Interrupt Enable Enables or disables interrupt requests (TCIU) by the TCFU flag when the TCFU flag in TSR is set to 1 in channels 1 and 2. In channel 0, bit 5 is reserved. 0: Interrupt requests (TCIU) by TCFU disabled 1: Interrupt requests (TCIU) by TCFU enabled
4	TCIEV	0	R/W	Overflow Interrupt Enable Enables or disables interrupt requests (TCIV) by the TCFV flag when the TCFV flag in TSR is set to 1. 0: Interrupt requests (TCIV) by TCFV disabled 1: Interrupt requests (TCIV) by TCFV enabled
3	TGIED	0	R/W	TGR Interrupt Enable D Enables or disables interrupt requests (TGID) by the TGFD bit when the TGFD bit in TSR is set to 1 in channel 0. In channels 1 and 2, bit 3 is reserved. It is always read as 0 and cannot be modified. 0: Interrupt requests (TGID) by TGFD disabled 1: Interrupt requests (TGID) by TGFD enabled.

10.8.10 Conflict between Overflow/Underflow and Counter Clearing

If overflow/underflow and counter clearing occur simultaneously, the TCFV/TCFU flag in TSR is not set and TCNT clearing takes precedence. Figure 10.51 shows the operation timing when a TGR compare match is specified as the clearing source, and H'FFFF is set in TGR.

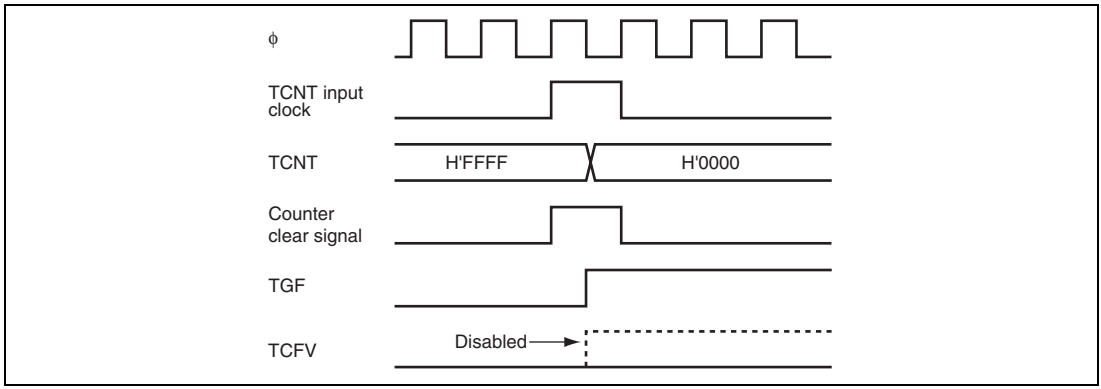


Figure 10.51 Conflict between Overflow and Counter Clearing

15.3.5 Serial Mode Register (SMR)

SMR is used to set the SCI's serial transfer format and select the baud rate generator clock source. Some bits in SMR have different functions in normal mode and smart card interface mode. The CPU can always read SMR. The CPU can write to SMR only at the initial settings; do not have the CPU write to SMR in transmission, reception, and simultaneous data transmission and reception.

- Bit Functions in Normal Serial Communication Interface Mode (when SMIF in SCMR = 0)

Bit	Bit Name	Initial Value	R/W	Description
7	C/$\overline{A}$	0	R/W	Communication Mode 0: Asynchronous mode 1: Clocked synchronous mode
6	CHR	0	R/W	Character Length (enabled only in asynchronous mode) 0: Selects 8 bits as the data length. 1: Selects 7 bits as the data length. LSB-first is fixed and the MSB of TDR is not transmitted in transmission. In clocked synchronous mode, a fixed data length of 8 bits is used.
5	PE	0	R/W	Parity Enable (enabled only in asynchronous mode) When this bit is set to 1, the parity bit is added to transmit data before transmission, and the parity bit is checked in reception. For a multiprocessor format, parity bit addition and checking are not performed regardless of the PE bit setting.
4	O/$\overline{E}$	0	R/W	Parity Mode (enabled only when the PE bit is 1 in asynchronous mode) 0: Selects even parity. 1: Selects odd parity.
3	STOP	0	R/W	Stop Bit Length (enabled only in asynchronous mode) Selects the stop bit length in transmission. 0: 1 stop bit 1: 2 stop bits In reception, only the first stop bit is checked. If the second stop bit is 0, it is treated as the start bit of the next transmit frame.

Bit	Bit Name	Initial Value	R/W	Description
2	STOP	0	R/W	Stop Bit Specifies the stop bit length for data transmission. For data reception, only the first stop bit is checked regardless of the setting. 0: 1 stop bit 1: 1.5 stop bits (data length: 5 bits) or 2 stop bits (data length: 6 to 8 bits)
1	CLS1	0	R/W	Character Length Select 1, 0
0	CLS0	0	R/W	These bits specify transmit/receive character data length. 00: Data length is 5 bits 01: Data length is 6 bits 10: Data length is 7 bits 11: Data length is 8 bits

17.3.10 Modem Control Register (FMCR)

FMCR controls output signals.

Bit	Bit Name	Initial Value	R/W	Description
7 to 5	—	All 0	R	Reserved These bits are always read as 1 and cannot be modified.
4	LOOP BACK	0	R/W	Loopback Test The transmit data output is internally connected to the receive data input, and the transmit data output pin (FRxD) becomes 1. The receive data input pin is disconnected from external sources. The four modem control input pins ($\overline{\text{DSR}}$, $\overline{\text{CTS}}$, $\overline{\text{RI}}$, and $\overline{\text{DCD}}$) are disconnected from external sources, and the pins are internally connected to the four modem control output signals ($\overline{\text{DTR}}$, $\overline{\text{RTS}}$, $\overline{\text{OUT1}}$, and $\overline{\text{OUT2}}$), respectively. The transmit data is received immediately in loopback mode. Enabling/disabling of interrupts is set by the OUT2LOOP bit in SCIFCR and FIER. 0: Loopback function disabled 1: Loopback function enabled

19.3.5 Keyboard Data Buffer Register (KBBR)

KBBR stores receive data. Its value is valid only when KBF = 1.

Bit	Bit Name	Initial Value	R/W	Description
7	KB7	0	R	Keyboard Data 7 to 0
6	KB6	0	R	8-bit read only data.
5	KB5	0	R	Initialized to H'00 by a reset or when KBIOE is cleared to 0.
4	KB4	0	R	
3	KB3	0	R	
2	KB2	0	R	
1	KB1	0	R	
0	KB0	0	R	

19.3.6 Keyboard Buffer Transmit Data Register (KBTR)

KBTR stores transmit data.

Bit	Bit Name	Initial Value	R/W	Description
7	KBT7	1	R/W	Keyboard Buffer Transmit Data Register 7 to 0
6	KBT6	1	R/W	Initialized to H'FF at reset.
5	KBT5	1	R/W	
4	KBT4	1	R/W	
3	KBT3	1	R/W	
2	KBT2	1	R/W	
1	KBT1	1	R/W	
0	KBT0	1	R/W	

- Host select register

I/O Address			Transfer	
Bits 5 to 3	**Bit 2**	**Bits 1 and 0**	**Cycle**	**Host Select Register**
Bits 15 to 3 in LADR1	0	Bits 1 and 0 in LADR1	I/O write	IDR1 write (data)
Bits 15 to 3 in LADR1	1	Bits 1 and 0 in LADR1	I/O write	IDR1 write (command)
Bits 15 to 3 in LADR1	0	Bits 1 and 0 in LADR1	I/O read	ODR1 read
Bits 15 to 3 in LADR1	1	Bits 1 and 0 in LADR1	I/O read	STR1 read

Note: * When channel 1 is used, the content of LADR1 must be set so that the addresses for channels 2, 3, 4, and SCIF are different.

20.3.6 LPC Channel 2 Address Registers H and L (LADR2H and LADR2L)

LADR2 sets the LPC channel 2 host address. The LADR2 contents must not be changed while channel 2 is operating (while LPC2E is set to 1).

- LADR2H

		Initial	R/W		
Bit	**Bit Name**	**Value**	**Slave**	**Host**	**Description**
7	Bit 15	0	R/W	—	Channel 2 Address Bits 15 to 8
6	Bit 14	0	R/W	—	Set the LPC channel 2 host address.
5	Bit 13	0	R/W	—	
4	Bit 12	0	R/W	—	
3	Bit 11	0	R/W	—	
2	Bit 10	0	R/W	—	
1	Bit 9	0	R/W	—	
0	Bit 8	0	R/W	—	

21.3.1 FSI Control Register 1 (FSICR1)

The FSICR1 control bits are classified into three functionalities: resetting the FSI internal signals, enabling/disabling FSI functions, and selecting FSI functions.

Bit	Bit Name	Initial Value	R/W		Description
			EC	Host	
7	SRES	0	R/W	—	Software Reset Controls initialization of the FSI internal sequencer. 0: Normal state 1: Clears the internal sequencer. Writing 1 to this bit generates a clear signal for the sequencer in the corresponding module, resulting in the initialization of the FSI's internal state.
6	FSIE	0	R/W	—	FSI Enable 0: Disables FSI operation. 1: Enables FSI operation. The following shows the initial state of the FSI pins when FSIE is set to 1: FSISS: Outputs high level. FSICK: Outputs high level or low level depending on DPHS and CPOS. FSIDO: Outputs high level. FSIDI: Inputs data.
5	FRDE	0	R/W	—	Fast-Read Enable 0: The FSI is in normal read operation mode. 1: The FSI is in fast-read operation mode.
4	AAIE	0	R/W	—	AAI (Auto Address Increment) Program Enable 0: The FSI performs byte-program operation. 1: The FSI performs AAI program operation.

(3) AAI-Program Instruction

If an LPC/FW memory write cycle occurs while the AAIE bit in FSICR1 is set to 1 and the FSIDMYE bit in FSILSTR1 is cleared to 0, and the FLDCT bit in SLCR and the FLWAIT bit in SLCR are set to 1, the flash memory address and write data are stored in FSIAR and FSIWDR, respectively. Then, the flash memory address, write data, and the AAI-Program instruction which is stored in FSI hardware in advance are transferred to FSITDR. After SYNC (long wait) has been returned, the transmit enable signal TE is set, and AAI-Program instruction execution starts. In the first byte, the instruction, address, and data in this order are transmitted to the SPI flash memory. In the second and the following bytes, an instruction and data in this order are transmitted to the SPI flash memory. When the transmission has been completed, SYNC (Ready) and TAR are returned to the host. To execute the AAI-Program instruction, byte transfer access in LPC memory write cycle or FW memory write cycle should be performed. To return to the AAI-Program instruction (first byte), clear the AAIE bit once or perform initialization of the FSI internal sequencer in SRES of FSICR1. After the Read instruction or the LPC-SPI command is transferred during the AAI-Program instruction execution, the FSI internal sequencer is initialized to return to the AAI-Program Instruction (first byte). Figures 21.6 and 21.7 show AAI-Program execution timings.

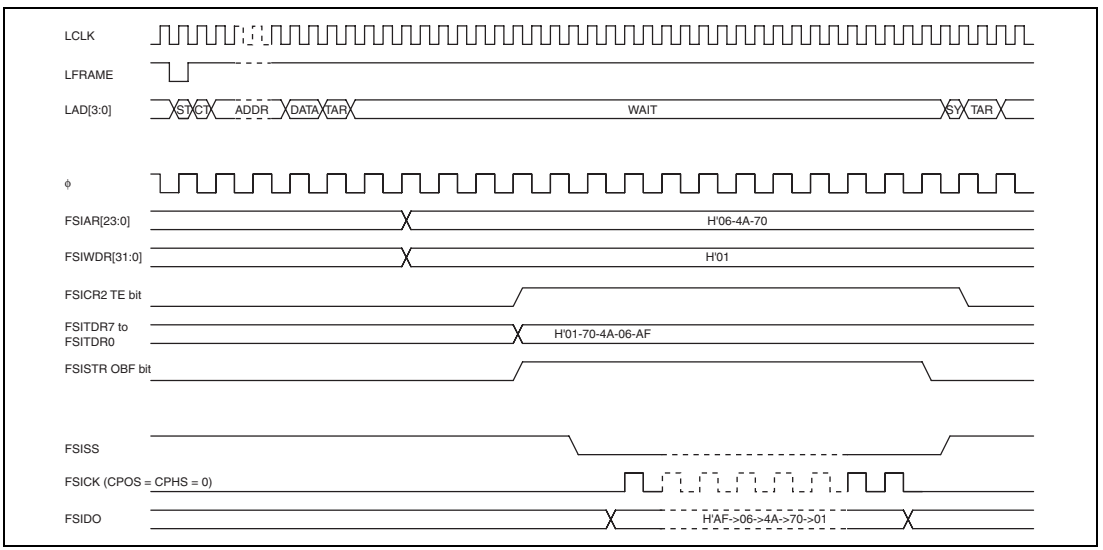


Figure 21.6 AAI-Program Instruction Execution Timing (First Byte)

4. Execute the SPI flash memory erasure instruction.
   — Set the TE bit in FSICR2 to 1.
   — Set the TBN bit in FSIBNR to 4-byte transfer.
   — Write the FSI address stored in FSIAR to FSITDR1 to FSITDR3.
   — Write the erasure instruction to FSIINS (start the SPI flash memory erasure instruction execution).
5. Complete the interrupt processing.
6. Generate an FSITEI interrupt request.
7. Clear the FSIDMYE and CMDBUSY bits in FSILSTR1 to 0.
8. Complete the interrupt processing.
9. Check that the FSIDMYE, CMDBUSY, and FSICMDI bits in FSILSTR1 are cleared to 0 (Host).

(6) FSI Command Usage Example 2 (SPI Flash Memory Status Read)

Figure 21.17 shows an example of the execution timing of the SPI flash memory status read instruction.

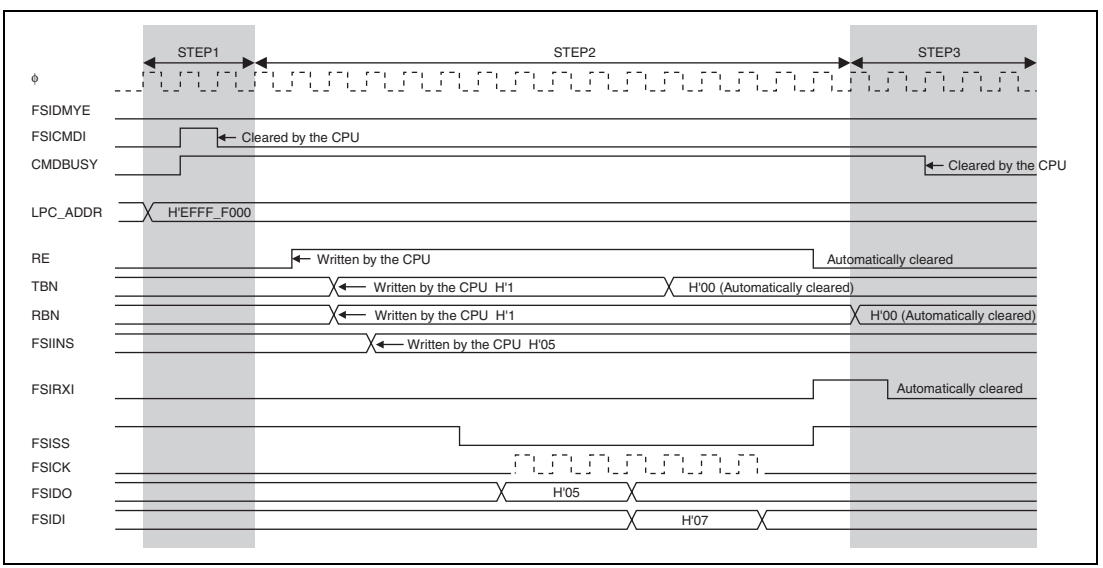


Figure 21.17 Execution Timing of SPI Flash Memory Status Read Instruction

The SPI flash memory status read instruction is executed in the following sequence.

(c) 128-Byte Programming

The boot program will use the programming program transferred by the programming selection to program the user MATs in response to 128-byte programming.

Command

H'50	Address						
Data	…						
…							
SUM							

- Command, H'50, (one byte): 128-byte programming
- Programming Address (four bytes): Start address for programming
  Multiple of the size specified in response to the programming unit inquiry
  (i.e. H'00, H'01, H'00, H'00 : H'00010000)
- Program data (128 bytes): Data to be programmed
  The size is specified in the response to the programming unit inquiry.
- SUM (one byte): Checksum

Response

H'06

- Response, H'06, (one byte): Response to 128-byte programming
  On completion of programming, the boot program will return ACK.

Error Response

H'D0	ERROR

- Error response, H'D0, (one byte): Error response for 128-byte programming
- ERROR: (one byte): Error code

  H'11: Checksum Error

  H'2A: Address Error

  The address is not within the specified MAT range.

  H'53: Programming error

  A programming error has occurred and programming cannot be continued.

The specified address should match the unit for programming of data. For example, when the programming is in 128-byte units, the lower eight bits of the address should be H'00 or H'80. When there are less than 128 bytes of data to be programmed, the host should fill the rest with H'FF.

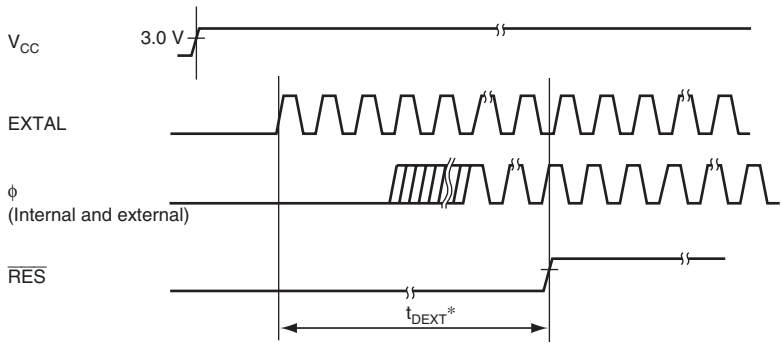
Sending the 128-byte programming command with the address of H'FFFFFFFF will stop the programming operation. The boot program will interpret this as the end of the programming and wait for selection of programming or erasing.

Table 25.4 External Clock Output Stabilization Delay Time

Condition: VCC = 3.0 V to 3.6 V, AVCC = 3.0 V to 3.6 V, VSS = AVSS = 0 V

Item	Symbol	Min.	Max.	Unit	Remarks
External clock output stabilization delay time	t_{DEXT}*	500	—	μs	Figure 25.6

Note: * t_{DEXT} includes a $\overline{RES}$ pulse width (t_{RESW}).



Note: * The external clock output stabilization delay time (t_{DEXT}) includes a $\overline{RES}$ pulse width (t_{RESW}).

Figure 25.6 Timing of External Clock Output Stabilization Delay Time

Register Name	Abbreviation	Number of bits	Address	Module	Data Width	Access States
LPC channel 3 address register L	LADR3L	8	H'FE35	LPC	8	2
SERIRQ control register 0	SIRQCR0	8	H'FE36	LPC	8	2
SERIRQ control register 1	SIRQCR1	8	H'FE37	LPC	8	2
Input data register 1	IDR1	8	H'FE38	LPC	8	2
Output data register 1	ODR1	8	H'FE39	LPC	8	2
Status register 1	STR1	8	H'FE3A	LPC	8	2
Input data register 2	IDR2	8	H'FE3C	LPC	8	2
SERIRQ control register 4	SIRQCR4	8	H'FE3B	LPC	8	2
Output data register 2	ODR2	8	H'FE3D	LPC	8	2
Status register 2	STR2	8	H'FE3E	LPC	8	2
Host interface select register	HISEL	8	H'FE3F	LPC	8	2
Host interface control register 0	HICR0	8	H'FE40	LPC	8	2
Host interface control register 1	HICR1	8	H'FE41	LPC	8	2
Host interface control register 2	HICR2	8	H'FE42	LPC	8	2
Host interface control register 3	HICR3	8	H'FE43	LPC	8	2
Wakeup event interrupt mask register	WUEMR	8	H'FE45	INT	8	2
Port G output data register	PGODR	8	H'FE46 (PORTS = 0)	PORT	8	2
Port G input data register	PGPIN	8	H'FE47 (Read) (PORTS = 0)	PORT	8	2
Port G data direction register	PGDDR	8	H'FE47 (Write) (PORTS = 0)	PORT	8	2
Port F output data register	PFODR	8	H'FE49 (PORTS = 0)	PORT	8	2
Port E input data register	PEPIN	8	H'FE4A (Read) (write prohibited) (PORTS = 0)	PORT	8	2
Port F input data register	PFPIN	8	H'FE4B (Read) (PORTS = 0)	PORT	8	2
Port F data direction register	PFDDR	8	H'FE4B (Write) (PORTS = 0)	PORT	8	2
Port C output data register	PCODR	8	H'FE4C (PORTS = 0)	PORT	8	2
Port D output data register	PDODR	8	H'FE4D (PORTS = 0)	PORT	8	2

Register Abbreviation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
KBCRH_3	KBIOE	KCLKI	KDI	KBFSEL	KBIE	KBF	PER	KBS	PS2_3
KBCRL_3	KBE	KCLKO	KDO	—	RXCR3	RXCR2	RXCR1	RXCR0	
KBBR_3	KB7	KB6	KB5	KB4	KB3	KB2	KB1	KB0	
KBCR2_3	—	—	—	—	TXCR3	TXCR2	TXCR1	TXCR0	
TCSR_1	OVF	WT/$\overline{IT}$	TME	PSS	RST/$\overline{NMI}$	CKS2	CKS1	CKS0	WDT_1
TCNT_1	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
TCR_X	CMIEB	CMIEA	OVIE	CCLR1	CCLR0	CKS2	CKS1	CKS0	TMR_X
TCSR_X	CMFB	CMFA	OVF	ICF	OS3	OS2	OS1	OS0	
TICRR	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
TICRF	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
TCNT_X	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
TCORC	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
TCORA_X	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
TCORB_X	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
TCONRI	—	—	—	ICST	—	—	—	—	
TCONRS	TMRX/Y	—	—	—	—	—	—	—	TMR_X, TMR_Y

Notes: 1. In normal mode and smart card interface mode, bit names differ in part.
( ) : Bit name in smart card interface mode.
2. When TWRE = 1 or SELSTR3 = 0.
3. When TWRE = 0 and SELSTR3 = 1.

Register Abbreviation	Reset	High-Speed/Medium speed	Watch	Sleep	Module Stop	Software Standby	Module
ISCR16L	Initialized	—	—	—	—	—	INT
ISSR16	Initialized	—	—	—	—	—	
ISSR	Initialized	—	—	—	—	—	
PCSR	Initialized	—	—	—	—	—	PWMX
SBYCR	Initialized	—	—	—	—	—	SYSTEM
LPWRCR	Initialized	—	—	—	—	—	
MSTPCRH	Initialized	—	—	—	—	—	
MSTPCRL	Initialized	—	—	—	—	—	
SMR_1	Initialized	—	—	—	—	—	SCI_1
BRR_1	Initialized	—	—	—	—	—	
SCR_1	Initialized	—	—	—	—	—	
TDR_1	Initialized	—	Initialized	—	Initialized	Initialized	
SSR_1	Initialized	—	Initialized	—	Initialized	Initialized	
RDR_1	Initialized	—	Initialized	—	Initialized	Initialized	
SCMR_1	Initialized	—	—	—	—	—	
SMR_2	Initialized	—	—	—	—	—	SCI_2
BRR_2	Initialized	—	—	—	—	—	
SCR_2	Initialized	—	—	—	—	—	
TDR_2	Initialized	—	Initialized	—	Initialized	Initialized	
SSR_2	Initialized	—	Initialized	—	Initialized	Initialized	
RDR_2	Initialized	—	Initialized	—	Initialized	Initialized	
SCMR_2	Initialized	—	—	—	—	—	
TCSR_0	Initialized	—	—	—	—	—	WDT_0
TCNT_0	Initialized	—	—	—	—	—	
PAODR	Initialized	—	—	—	—	—	PORT
PAPIN	—	—	—	—	—	—	
PADDR	Initialized	—	—	—	—	—	
P1PCR	Initialized	—	—	—	—	—	
P2PCR	Initialized	—	—	—	—	—	
P3PCR	Initialized	—	—	—	—	—	