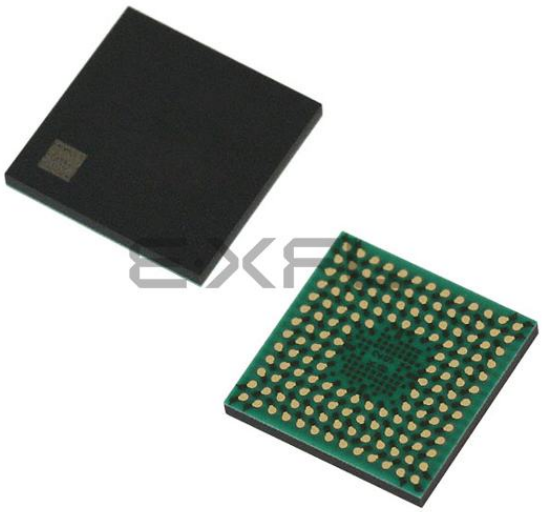

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2600
Core Size	16-Bit
Speed	20MHz
Connectivity	FIFO, I²C, LPC, SCI, SmartCard
Peripherals	POR, PWM, WDT
Number of I/O	112
Program Memory Size	160KB (160K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	145-TFLGA
Supplier Device Package	145-TFLGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2117rvlp20hv

Section 1 Overview

1.1 Features

The core of each product in the H8S/2117R Group of CISC (complex instruction set computer) microcomputers is an H8S/2600 CPU, which has an internal 16-bit architecture. The H8S/2600 CPU provides upward-compatibility with the CPUs of other Renesas Technology-original microcomputers; H8/300, H8/300H, and H8S.

As peripheral functions, each LSI of the group includes a serial communication interface with FIFO, an I^2C bus interface, an A/D converter, and various types of timers. Together, the modules realize low-cost system configurations. The power consumption of these modules is kept down dynamically by power-down modes. The on-chip ROM is a flash memory (F-ZTAT™*) with a capacity of 160 Kbytes.

Note: * F-ZTAT™ is a trademark of Renesas Technology Corp.

1.1.1 Applications

Examples of the applications of this LSI include PC peripheral equipment, office automation equipment, and industrial equipment.

3.2.4 System Control Register 3 (SYSCR3)

SYSCR3 selects the register map and interrupt vector.

Bit	Bit Name	Initial Value	R/W	Description
7	—	0	R/W	Reserved The initial value should not be changed.
6	EIVS*	1	R/W	Extended interrupt Vector Select* Selects compatible mode or extended mode for the interrupt vector table. 0: H8S/2140B Group compatible vector mode 1: Extended vector mode For details, see section 5, Interrupt Controller.
5	RELOCATE	1	R/W	Register Address Map Select Selects compatible mode or extended mode for the register map. When extended mode is selected for the register map, CPU access for registers can be controlled without using the KINWUE bit in SYSCR or the IICE bit in STCR to switch the registers to be accessed. 0: H8S/2140B Group compatible register map mode 1: Extended register map mode For details, see section 27, List of Registers.
4 to 0	—	All 0	R/W	Reserved The initial value should not be changed.

Note: * Switch the modes when an interrupt occurrence is disabled.

3.3 Operating Mode Descriptions

3.3.1 Mode 2

The CPU can access a 16-Mbyte address space in either advanced mode or single-chip mode. The on-chip ROM is enabled.

Port	Description	Bit	Function			Input Pull-up MOS Function	LED Drive Capability (5 mA Sink Current)	On-Chip Noise Canceler
			I/O	Input	Output			
Port D	General I/O port also functioning as A/D converter analog input	7	PD7	AN15	—	O	O	—
		6	PD6	AN14	—			
		5	PD5	AN13	—			
		4	PD4	AN12	—			
		3	PD3	AN11	—			
		2	PD2	AN10	—			
		1	PD1	AN9	—			
		0	PD0	AN8	—			
Port E	General input port also functioning as external sub-clock input, emulator input/output	4	—	PE4*[1]/ETMS	—	—	—	—
		3	—	PE3*[1]	ETDO			
		2	—	PE2*[1]/ETDI	—			
		1	—	PE1*[1] /ETCK	—			
		0	—	PE0/ExEXCL	—			
Port F	General I/O port also functioning as interrupt and TDP inputs, TMR_X, TMR_Y, and PWM outputs	7	PF7	—	PWMU5A	O	—	—
		6	PF6	—	PWMU4A			
		5	PF5	—	PWMU3A			
		4	PF4	—	PWMU2A			
		3	PF3	TDPCKI0/ TDPMCI0/$\overline{\text{IRQ11}}$	TMOX			
		2	PF2	TDPCYI0//$\overline{\text{IRQ10}}$	TMOY			
		1	PF1	$\overline{\text{IRQ9}}$	PWMU1A			
		0	PF0	$\overline{\text{IRQ8}}$	PWMU0A			

8.4 Operation

The PWMU operates in 8-bit single pulse mode, 16-bit single pulse mode, or 8-bit division pulse mode.

8.4.1 Single-Pulse Mode (8 Bits, 16 Bits)

Figure 8.2 shows a block diagram of 8-bit single pulse mode. Figure 8.3 shows a block diagram of 16-bit single pulse mode.

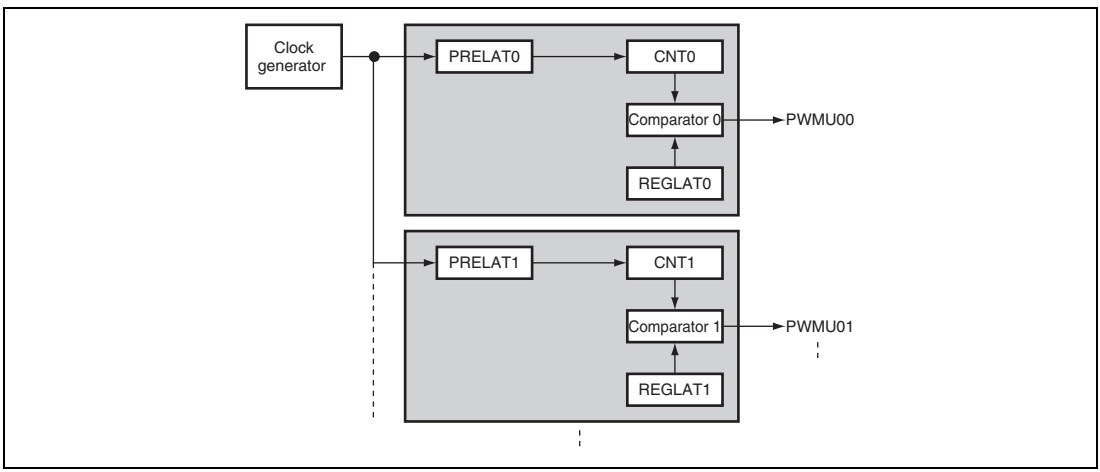

Figure 8.2 Block Diagram of 8-Bit Single Pulse Mode

10.6 Interrupts

10.6.1 Interrupt Source and Priority

There are three kinds of TPU interrupt source: TGR input capture/compare match, TCNT overflow, and TCNT underflow. Each interrupt source has its own status flag and enable/disabled bit, allowing generation of interrupt request signals to be enabled or disabled individually. When an interrupt request is generated, the corresponding status flag in TSR is set to 1. If the corresponding enable/disable bit in TIER is set to 1 at this time, an interrupt is requested. The interrupt request is cleared by clearing the status flag to 0. Relative channel priorities can be changed by the interrupt controller, but the priority order within a channel is fixed. For details, see section 5, Interrupt Controller. Table 10.25 lists the TPU interrupt sources.

Table 10.25 TPU Interrupts

Channel	Name	Interrupt Source	Interrupt Flag	Priority*
0	TGI0A	TGRA_0 input capture/compare match	TGFA	High
	TGI0B	TGRB_0 input capture/compare match	TGFB	
	TGI0C	TGRC_0 input capture/compare match	TGFC	
	TGI0D	TGRD_0 input capture/compare match	TGFD	
	TCI0V	TCNT_0 overflow	TCFV	
1	TGI1A	TGRA_1 input capture/compare match	TGFA	
	TGI1B	TGRB_1 input capture/compare match	TGFB	
	TCI1V	TCNT_1 overflow	TCFV	
	TCI1U	TCNT_1 underflow	TCFU	
2	TGI2A	TGRA_2 input capture/compare match	TGFA	
	TGI2B	TGRB_2 input capture/compare match	TGFB	
	TCI2V	TCNT_2 overflow	TCFV	
	TCI2U	TCNT_2 underflow	TCFU	Low

Note: * This table shows the initial state immediately after a reset. The relative channel priorities can be changed by the interrupt controller.

11.3.6 TCM Status Register (TCMCSR)

TCMCSR is an 8-bit readable/writable register that controls operation of the interrupt sources.

Bit	Bit Name	Initial Value	R/W	Description
7	OVF	0	R/(W)*	Timer Overflow This flag indicates that the TCMCNT has overflowed. [Setting condition] Overflow of TCMCNT (change in value from H'FFFF to H'0000) [Clearing condition] Reading OVF when OVF = 1 and then writing 0 to OVF.
6	MAXOVF	0	R/(W)*	Measurement Period Upper Limit Overflow This flag indicates that the measured number of cycles of the waveform for measurement in cycle measurement mode has reached the upper limit set in TCMMLCM, causing an overflow. [Setting condition] A greater value for TCMICR than TCMMLCM [Clearing condition] Reading MAXOVF when MAXOVF = 1 and then writing 0 to MAXOVF
5	CMF	0	R/(W)*	Compare Match Flag (only valid in timer mode) [Setting condition] When the values in TCMCNT and TCMMLCM match. [Clearing condition] Reading CMF when CMF = 1 and then writing 0 to CMF Note: CMF is not set in cycle measurement mode, even when the values in TCMCNT and TCMMLCM match.
4	CKSEG	0	R/W	External Clock Edge Select When bits CKS2 to CKS0 in TCMCR are set to B'111, this bit selects the edge for counting of external count clock edge. 0: Count falling edges of the external clock. 1: Count rising edges of the external clock.

(2) Reception

Before making the transition to module stop, software standby or watch mode, stop reception (RE = 0). RSR, RDR, and SSR are reset. If transition is made during data reception, the data being received will be invalid.

To receive data in the same reception mode after mode cancellation, set RE to 1, and then start reception. To receive data in a different reception mode, initialize the SCI first.

Figure 15.36 shows a sample flowchart for mode transition during reception.

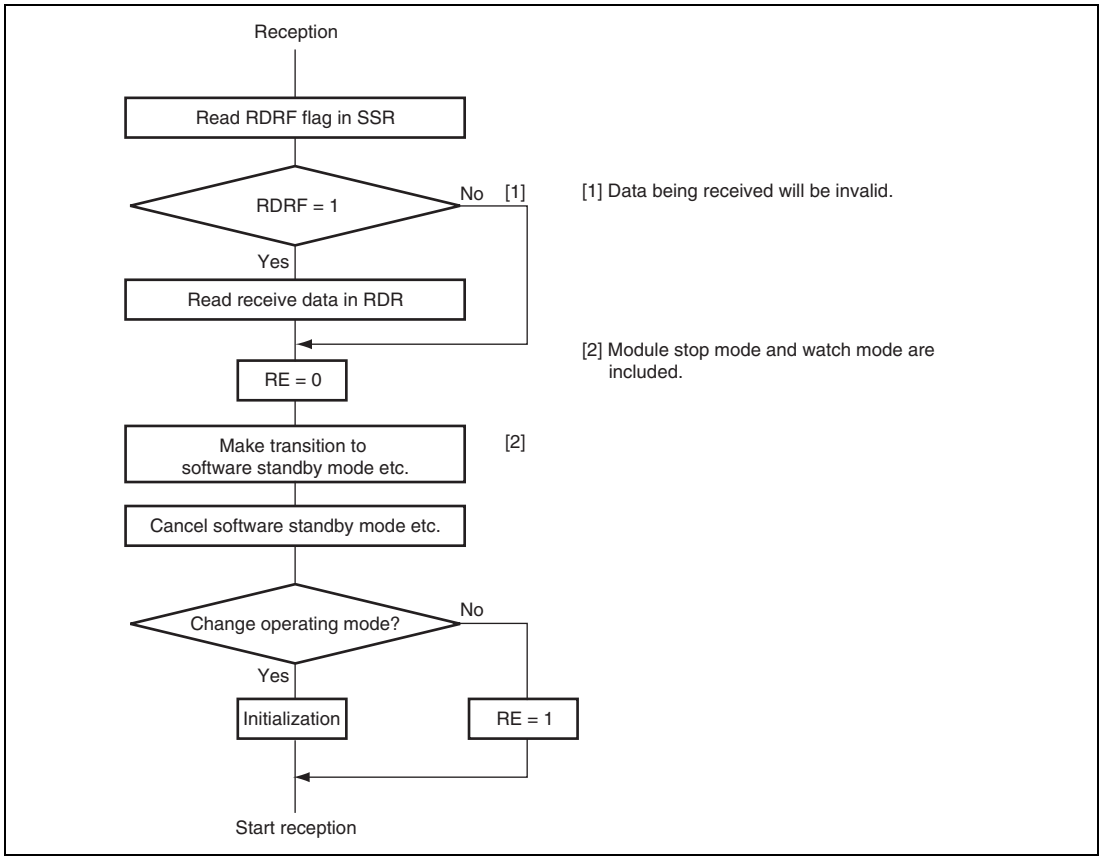

Figure 15.36 Sample Flowchart for Mode Transition during Reception

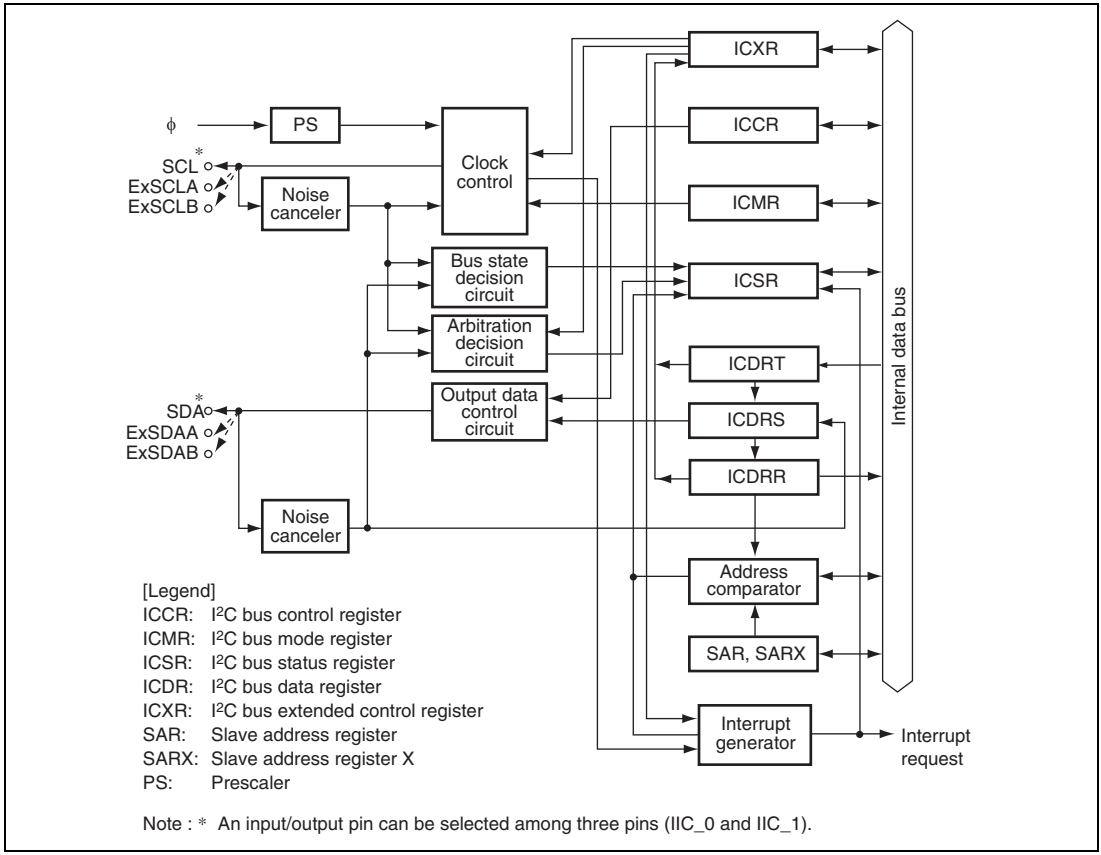

Figure 18.1 Block Diagram of I²C Bus Interface

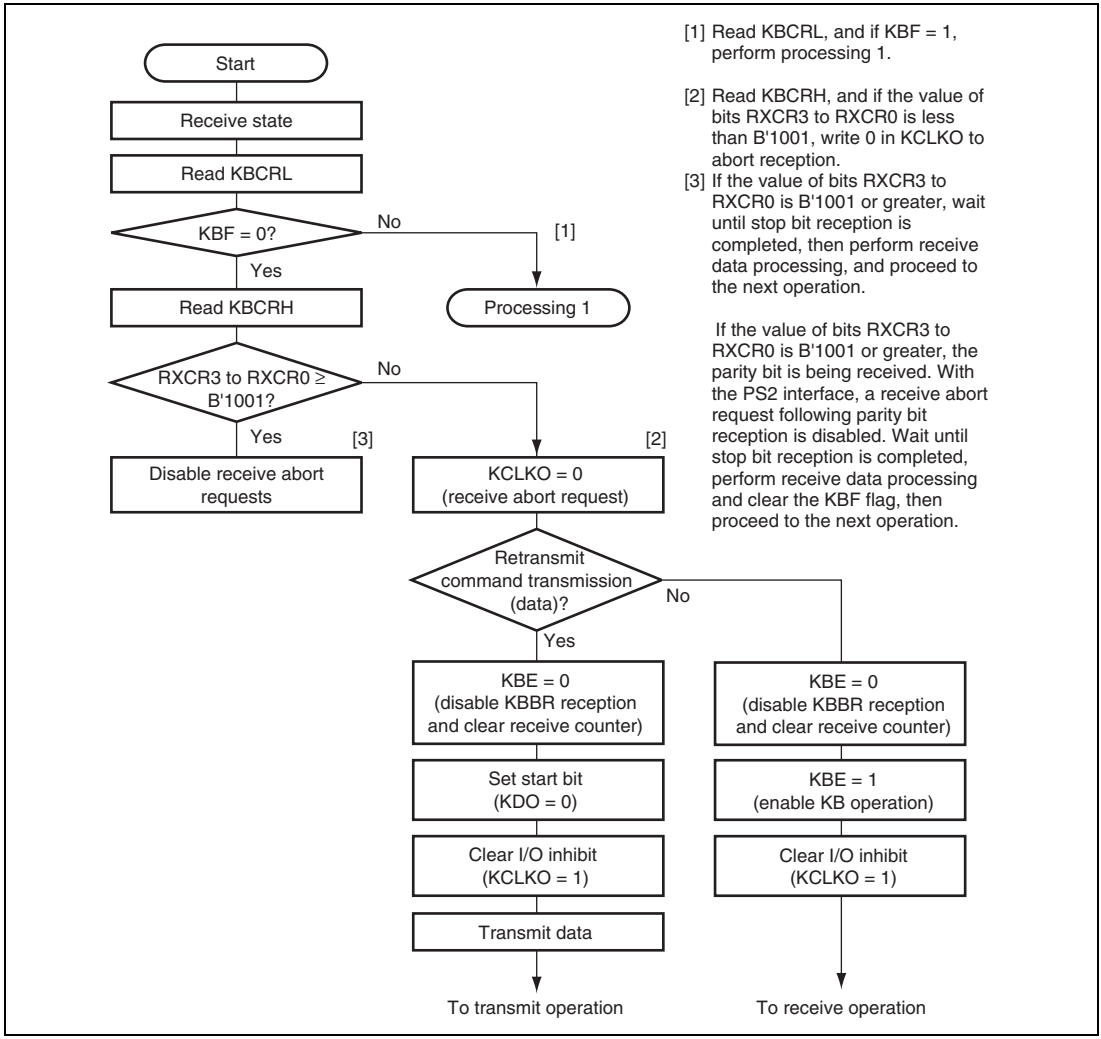

Figure 19.7 Sample Receive Abort Processing Flowchart (1)

20.3.18 SCIF Address Register (SCIFADRH, SCIFADRL)

SCIFADR sets the host addresses of the SCIF. Do not change the contents of SCIFADR during operation of the SCIF (i.e. while SCIFE is set to 1).

- SCIFADRH

Bit	Bit Name	Initial Value	R/W		Description
			Slave	Host	
7	—	0	R/W	—	SCIF Addresses 15 to 8
6	—	0	R/W	—	These bits set the host addresses of the SCIF.
5	—	0	R/W	—	
4	—	0	R/W	—	
3	—	0	R/W	—	
2	—	0	R/W	—	
1	—	1	R/W	—	
0	—	1	R/W	—	

- SCIFADRL

Bit	Bit Name	Initial Value	R/W		Description
			Slave	Host	
7	—	1	R/W	—	SCIF Addresses 7 to 0
6	—	1	R/W	—	These bits set the host addresses of the SCIF.
5	—	1	R/W	—	
4	—	1	R/W	—	
3	—	1	R/W	—	
2	—	0	R/W	—	
1	—	0	R/W	—	
0	—	0	R/W	—	

Note: When the SCIF is in use, set different addresses in the SCIFADR for channels 1, 2, 3, and 4.

20.6 Usage Note

20.6.1 Data Conflict

The LPC interface provides buffering of asynchronous data from the host and slave (this LSI), but an interface protocol that uses the flags in STR must be followed to avoid data conflict. For example, if the host and slave both try to access IDR or ODR at the same time, the data will be corrupted. To prevent simultaneous accesses, IBF and OBF must be used to allow access only to data for which writing has finished.

Unlike the IDR and ODR registers, the transfer direction is not fixed for the bidirectional data registers (TWR). MWMF and SWMF are provided in STR to handle this situation. After writing to TWR0, MWMF and SWMF must be used to confirm that the write authority for TWR1 to TWR15 has been obtained.

Table 20.12 shows host address examples for LADR3 and registers, IDR3, ODR3, STR3, TWR0MW, TWR0SW, and TWR1 to TWR15.

Bit	Bit Name	Initial Value	R/W EC	R/W Host	Description
2 to 0	RBN2	0	R/W	—	Receive Byte Count 2-0
	RBN1	0			These bits specify the number of data bytes to be received. After the FSI reception operation ends (when FSIRXI in FSISTR is 1), the RBN value is decremented (–1) each time FSIRDR is read. When all the data bytes have been received, RBN is cleared to B'000.
	RBN0	0			
					000: Receives no data
					001: Receives one byte of data
					010: Receives two bytes of data
					011: Receives three bytes of data
					100: Receives four bytes of data
					101 to 111: Setting prohibited
					If reception of five bytes or more is specified, FSIRDR is overwritten.

21.3.4 FSI Instruction Register (FSIINS)

FSIINS sets an instruction to be sent to the SPI flash memory during command transfer. When LFBUSY is 1, a write to this register by the EC (this LSI) is invalid. This register should not be set in the processing other than FSICMDI and FSIWI interrupt processing.

Bit	Bit Name	Initial Value	R/W EC	R/W Host	Description
7 to 0	bit 7 to bit 0	All 0	R/W	—	These bits store an instruction to be transmitted to the SPI flash memory.

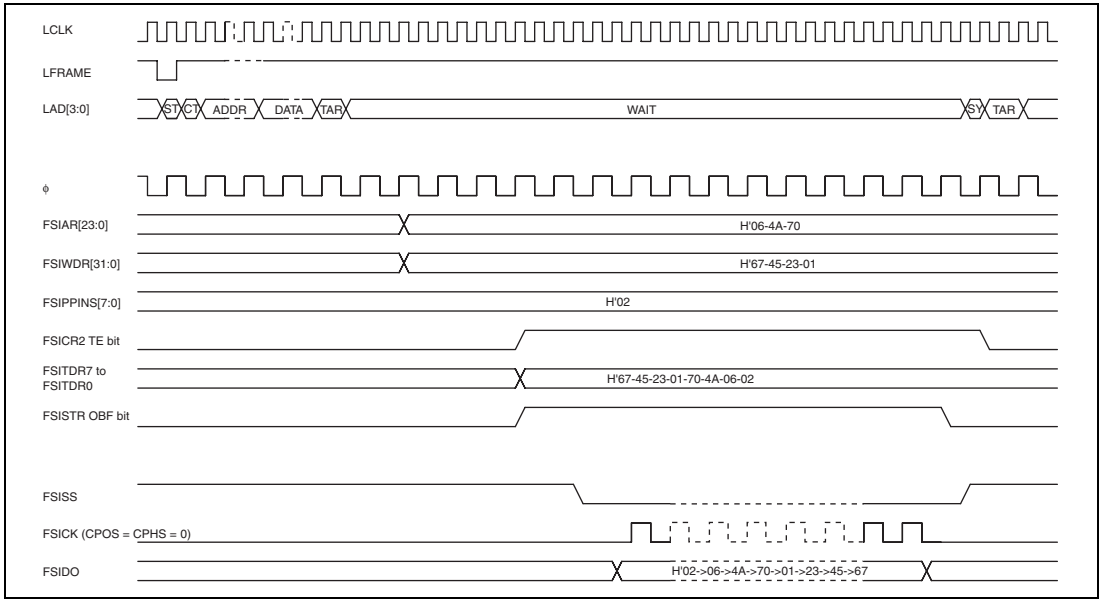

Figure 21.5 Page-Program Instruction Execution Timing

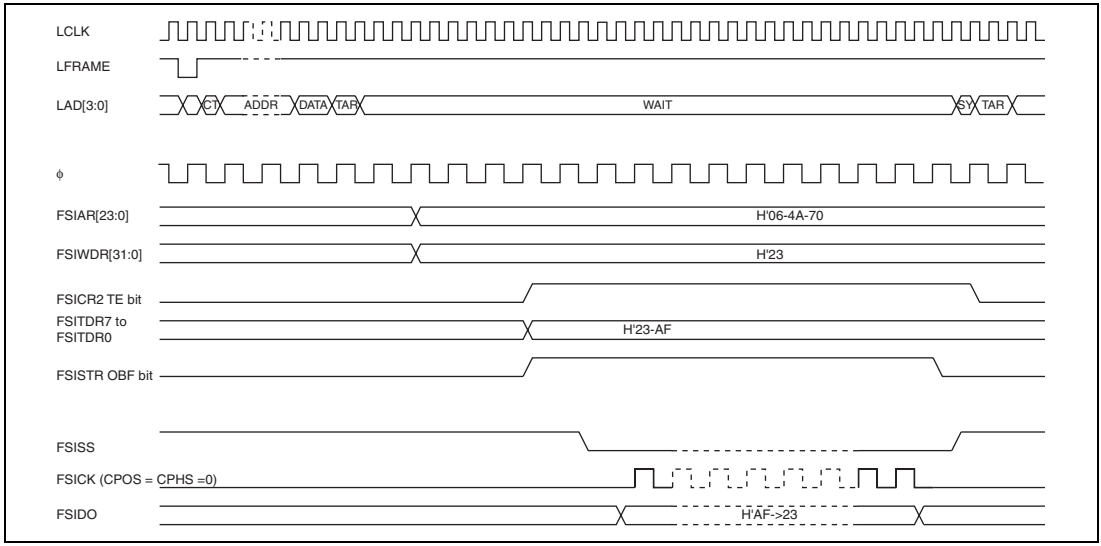

Figure 21.7 AAI-Program Instruction Execution Timing (Second and Following Bytes)

(4) Read Instructions

If an LPC/FW memory read cycle occurs while the FRDE bit in FSICR1 is cleared to 0, the SPI flash memory address is stored in FSIAR. Then, the SPI flash memory address and the instruction which is stored in FSIRDINS in advance are transferred to FSITDR. After SYNC (long wait) has been returned, the RE bit in FSICR2 is set, and Read instruction execution starts. The read data is then received and stored in FSIRDR. When the reception has been completed, SYNC (Ready), read data, and TAR are returned to the host. Figure 21.8 shows an example of data transfer to FSIRDR. Figure 21.9 shows the Read instruction execution timing.

- The user boot MAT can be programmed or erased only in boot mode and programmer mode.
- In boot mode, the user boot MAT are totally erased. Then, the user MAT or user boot MAT can be programmed by means of commands. Note that the contents of the MAT cannot be read until this state.

  Boot mode can be used for programming only the boot MAT and then programming the user MAT in user boot mode. Another way is to program only the user MAT since user boot mode is not used.
- In user boot mode, boot operation of the optional interface can be performed with mode pin settings different from those in user program mode.

24.3 Flash Memory MAT Configuration

This LSI's flash memory is configured by the 160-Kbyte user MAT and 8-Kbyte user boot MAT. The start address is allocated to the same address in the user MAT and user boot MAT. Therefore, when program execution or data access is performed between two MATs, the MAT must be switched by using FMATS.

The user MAT or user boot MAT can be read in all modes. However, the user boot MAT can be programmed only in boot mode and programmer mode.

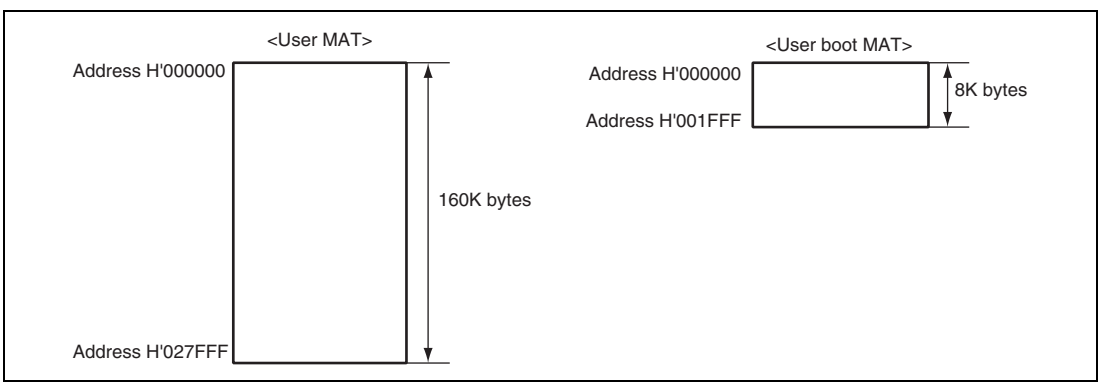

Figure 24.3 Flash Memory Configuration

The size of the user MAT is different from that of the user boot MAT. An address that exceeds the size of the 8-Kbyte user boot MAT should not be accessed. If the attempt is made, data is read as an undefined value.

Register Abbreviation	Reset	High-Speed/Medium speed	Watch	Sleep	Module Stop	Software Standby	Module
TCMCNT_3	Initialized	—	—	—	—	—	TCM_3
TCMMLCM_3	Initialized	—	—	—	—	—	
TCMICR_3	Initialized	—	—	—	—	—	
TCMICRF_3	Initialized	—	—	—	—	—	
TCMCSR_3	Initialized	—	—	—	—	—	
TCMCR_3	Initialized	—	—	—	—	—	
TCMIER_3	Initialized	—	—	—	—	—	
TCMMINCM_3	Initialized	—	—	—	—	—	
ADDRA	Initialized	—	Initialized	—	Initialized	Initialized	A/D converter
ADDRB	Initialized	—	Initialized	—	Initialized	Initialized	
ADDRC	Initialized	—	Initialized	—	Initialized	Initialized	
ADDRD	Initialized	—	Initialized	—	Initialized	Initialized	
ADDRE	Initialized	—	Initialized	—	Initialized	Initialized	
ADDRF	Initialized	—	Initialized	—	Initialized	Initialized	
ADDRG	Initialized	—	Initialized	—	Initialized	Initialized	
ADDRH	Initialized	—	Initialized	—	Initialized	Initialized	
ADCSR	Initialized	—	Initialized	—	Initialized	Initialized	
ADCR	Initialized	—	Initialized	—	Initialized	Initialized	
FRBR	Initialized	—	—	—	—	—	SCIF
FTHR	—	—	—	—	—	—	
FDLL	Initialized	—	—	—	—	—	
FIER	Initialized	—	—	—	—	—	
FDLH	Initialized	—	—	—	—	—	
FIIR	Initialized	—	—	—	—	—	
FFCR	Initialized	—	—	—	—	—	
FLCR	Initialized	—	—	—	—	—	
FMCR	Initialized	—	—	—	—	—	
FLSR	Initialized	—	—	—	—	—	
FMSR	—	—	—	—	—	—	
FSCR	Initialized	—	—	—	—	—	
SCIFCR	Initialized	—	—	—	—	—	

Lower Address	Register Abbreviation	Register Selection Condition	Module
H'FD10	PWMREG0_B	MSTPB0 = 0	PWMU_B
H'FD11	PWMPRE0_B		
H'FD12	PWMREG1_B		
H'FD13	PWMPRE1_B		
H'FD14	PWMREG2_B		
H'FD15	PWMPRE2_B		
H'FD16	PWMREG3_B		
H'FD17	PWMPRE3_B		
H'FD18	PWMREG4_B		
H'FD19	PWMPRE4_B		
H'FD1A	PWMREG5_B		
H'FD1B	PWMPRE5_B		
H'FD1C	PWMCONA_B		
H'FD1D	PWMCONB_B		
H'FD1E	PWMCONC_B		
H'FD1F	PWMCOND_B		
H'FD3A	SYTSR0	No condition	SYSTEM
H'FD3B	SYTSR1		
H'FD40	TCR_1	MSTP1 = 0	TPU_1
H'FD41	TMDR_1		
H'FD42	TIOR_1		
H'FD44	TIER_1		
H'FD45	TSR_1		
H'FD46	TCNT_1		
H'FD48	TGRA_1		
H'FD4A	TGRB_1		

27.5 Register Addresses (Classification by Type of Module)

Module	Register Abbreviation	Number of Bits	Address	Data Bus Width	Access States
INT	WUEMR	8	H'FE45	8	2
INT	KMIMR	8	H'FE81 (RELOCATE = 1)	8	2
INT	KMIMRA	8	H'FE83 (RELOCATE = 1)	8	2
INT	WUESCR	8	H'FE84	8	2
INT	WUESR	8	H'FE85	8	2
INT	WER	8	H'FE86	8	2
INT	ICRD	8	H'FE87	8	2
INT	ICRA	8	H'FEE8	8	2
INT	ICRB	8	H'FEE9	8	2
INT	ICRC	8	H'FEEA	8	2
INT	ISR	8	H'FEEB	8	2
INT	ISCRH	8	H'FEEC	8	2
INT	ISCRL	8	H'FEED	8	2
INT	KMIMR	8	H'FFF1 (RELOCATE = 0)	8	2
INT	ABRKCR	8	H'FEF4	8	2
INT	BARA	8	H'FEF5	8	2
INT	BARB	8	H'FEF6	8	2
INT	BARC	8	H'FEF7	8	2
INT	IER16	8	H'FEF8	8	2
INT	ISR16	8	H'FEF9	8	2
INT	ISCR16H	8	H'FEFA	8	2
INT	ISCR16L	8	H'FEFB	8	2
INT	ISSR16	8	H'FEFC	8	2
INT	ISSR	8	H'FEFD	8	2
INT	IER	8	H'FFC2	8	2
INT	KMIMRA	8	H'FFF3 (RELOCATE = 0)	8	2

Module	Register Abbreviation	Number of Bits	Address	Data Bus Width	Access States
IIC_2	ICMR_2	8	H'FE8F	8	2
IIC_2	SAR_2	8	H'FE8F	8	2
IIC_0	ICRES_0	8	H'FEE6	8	2
PS2_0	KBCR1_0	8	H'FEC0	8	2
PS2_0	KBTR_0	8	H'FEC1	8	2
PS2_0	KBCRH_0	8	H'FED8	8	2
PS2_0	KBCRL_0	8	H'FED9	8	2
PS2_0	KBBR_0	8	H'FEDA	8	2
PS2_0	KBCR2_0	8	H'FEDB	8	2
PS2_1	KBCR1_1	8	H'FEC2	8	2
PS2_1	KBTR_1	8	H'FEC3	8	2
PS2_1	KBCRH_1	8	H'FEDC	8	2
PS2_1	KBCRL_1	8	H'FEDD	8	2
PS2_1	KBBR_1	8	H'FEDE	8	2
PS2_1	KBCR2_1	8	H'FEDF	8	2
PS2_2	KBCR1_2	8	H'FEC4	8	2
PS2_2	KBTR_2	8	H'FEC5	8	2
PS2_2	KBCRH_2	8	H'FEE0	8	2
PS2_2	KBCRL_2	8	H'FEE1	8	2
PS2_2	KBBR_2	8	H'FEE2	8	2
PS2_2	KBCR2_2	8	H'FEE3	8	2
PS2_3	KBCR1_3	8	H'FED2	8	2
PS2_3	KBTR_3	8	H'FED3	8	2
PS2_3	KBCRH_3	8	H'FFE0	8	2
PS2_3	KBCRL_3	8	H'FFE1	8	2
PS2_3	KBBR_3	8	H'FFE2	8	2
PS2_3	KBCR2_3	8	H'FFE3	8	2
LPC	LADR1H	8	H'FDC0	8	2
LPC	LADR1L	8	H'FDC1	8	2
LPC	LADR2H	8	H'FDC2	8	2
LPC	LADR2L	8	H'FDC3	8	2

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Hardware Manual
H8S/2117R Group

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