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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	H8S/2600
Core Size	16-Bit
Speed	20MHz
Connectivity	FIFO, I ² C, LPC, SCI, SmartCard
Peripherals	POR, PWM, WDT
Number of I/O	128
Program Memory Size	160KB (160K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LFBGA
Supplier Device Package	176-LFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2117rvpbg20hv

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

2. Description of Numbers and Symbols

Aspects of the notations for register names, bit names, numbers, and symbolic names in this manual are explained below.

(1)	Dverall notation n descriptions involving the names of bits and bit fields within this manual, the modules and egisters to which the bits belong may be clarified by giving the names in the forms module name"."register name"."bit name" or "register name"."bit name".							
(2)	Register notation The style "register name"_"instance number" is used in cases where there is more than one instance of the same function or similar functions. [Example] CMCSR_0: Indicates the CMCSR register for the compare-match timer of channel 0.							
(3)	Number notation Binary numbers are given as B'nnnn (B' may be omitted if the number is obviously binary), hexadecimal numbers are given as H'nnnn or 0xnnnn, and decimal numbers are given as nnnn. [Examples] Binary: B'11 or 11 Hexadecimal: H'EFA0 or 0xEFA0 Decimal: 1234							
(4)	Notation for active-low An overbar on the name indicates that a signal or pin is active-low. [Example] WDTOVF							
	(4) (2)							
_								
	14.2.2 Compare Match Control/Status Register_0, _1 (CMCSR_0, CMCSR_1)							
L T	CMCSR indicates compare match generation, enables or disables interrupts, and selects the counter ut clock. Generation of a WDTOVF signal or interrupt initializes the TCNT value to 0.							
	14.3 Opt-							
	14.3.1 Interval Count Operation							
	When an internal clock is selected with the CKS1 and CKS0 bits in CMCSR and the STR bit in CMSTR is set to 1, CMCNT starts incrementing using the selected clock. When the values in CMCNT and the compare match constant register (CMCOR) match, CMCNT is cleared to H'0000 and the CMF flag in CMCSR is set to 1. When the CKS1 and CKS0 bits are set to B'01 at this time, a f/4 clock is selected.							
	Rev. 0.50, 10/04, page 416 of 914							
L	(3)							
	Note: The bit names and sentences in the above figure are examples and have nothing to do with the contents of this manual.							

Contents

Secti	on 1 O	verview	1
1.1	Feature	s	1
	1.1.1	Applications	1
	1.1.2	Overview of Functions	2
1.2	List of	Products	7
1.3	Block I	Diagram	8
1.4	Pin Des	scriptions	9
	1.4.1	Pin Assignments	9
	1.4.2	Pin Assignment in Each Operating Mode	. 12
	1.4.3	Pin Functions	. 19
Secti	on 2 C	PU	29
2.1		S	
2.1	2.1.1	Differences between H8S/2600 CPU and H8S/2000 CPU	
	2.1.2	Differences from H8/300 CPU	
	2.1.3	Differences from H8/300H CPU	
2.2	CPU O	perating Modes	
	2.2.1	Normal Mode	
	2.2.2	Advanced Mode	
2.3	Addres	s Space	. 36
2.4	Registe	rs	. 37
	2.4.1	General Registers	. 38
	2.4.2	Program Counter (PC)	. 39
	2.4.3	Extended Control Register (EXR)	. 39
	2.4.4	Condition-Code Register (CCR)	
	2.4.5	Multiply-Accumulate Register (MAC)	.41
	2.4.6	Initial Values of CPU Registers	.41
2.5	Data Fo	ormats	. 42
	2.5.1	General Register Data Formats	. 42
	2.5.2	Memory Data Formats	. 44
2.6	Instruct	ion Set	. 45
	2.6.1	Table of Instructions Classified by Function	. 46
	2.6.2	Basic Instruction Formats	. 56
2.7	Addres	sing Modes and Effective Address Calculation	. 57
	2.7.1	Register Direct—Rn	. 57
	2.7.2	Register Indirect—@ERn	. 57

	15.9.8	Note on Writing to Registers in Transmission, Reception, and	
		Simultaneous Transmission and Reception	467
Secti	on 16 (CIR Interface	469
16.1	Feature	² S	469
16.2	Input P	'ins	471
16.3	Registe	er Description	471
	16.3.1	Receive Control Register 1 (CCR1)	472
	16.3.2	Receive Control Register 2 (CCR2)	473
	16.3.3	Receive Status Register (CSTR)	474
	16.3.4	Interrupt Enable Register (CEIR)	476
	16.3.5	Bit Rate Register (BRR)	477
	16.3.6	Receive Data Register 0 to 17 (CIRRDR0 to CIRRDR17)	478
	16.3.7	Header Minimum/Maximum High-Level Period Register	
		(HHMIN and HHMAX)	478
	16.3.8	Header Minimum/Maximum Low-Level Period Register (HLMIN/HLMAX)	480
	16.3.9	Data Level 1 Minimum/Maximum Period Register (DT1MIN/DT1MAX)	480
	16.3.10) Data Level 0 Minimum/Maximum Period Register (DT0MIN/DT0MAX)	481
	16.3.11	Repeat Header Minimum/Maximum Low-Level Period Register	
		(RMIN/RMAX)	481
16.4	Operati	ion	482
	16.4.1	Determination of Signal Type by Low/High-Level Period	484
	16.4.2	Operation of FIFO Register	486
	16.4.3	Operation in Watch Mode	487
	16.4.4	Switching between System Clock and Sub Clock	487
16.5	Noise (Canceler Circuit	488
16.6	Reset C	Conditions	490
16.7	Interrup	pt Sources	490
16.8	Usage I	Note	491
Secti	on 17 S	Serial Communication Interface with FIFO (SCIF)	493
17.1	Feature	28	493
17.2	Input/C	Dutput Pins	495
17.3	Registe	er Descriptions	496
	17.3.1	Receive Shift Register (FRSR)	497
		Receive Buffer Register (FRBR)	
	17.3.3	Transmitter Shift Register (FTSR)	498
		Transmitter Holding Register (FTHR)	
		Divisor Latch H, L (FDLH, FDLL)	
	17.3.6	Interrupt Enable Register (FIER)	499

TFP- 144V BP. 176V TLP- 145V Single-Chip Mode 45 R5 N4 PF5/PWMU3A 46 M6 M5 PF4/PWMU2A 47 N6 L5 PF3/IRQ11/TMOX/TDPCKI0/TDPMCI0 48 R6 M6 PF2/IRQ3/IRQ1/TMOY/TDPCYI0 49 P6 N5 PF1/IRQ9/PWMU1A 50 M7 K5 PF0/IRQ8/PWMU0A - N7 (N) - PI1 51 (N) R7 (N) L6 (N) PG7/EXIRQ15/ExSCLB 52 (N) P7 (N) M7 (N) PG6/EXIRQ14/ExSDAB 53 (N) M8 (N) N6 (N) PG5/EXIRQ13/ExSCLA - N8 (N) N6 (N) PG3/EXIRQ13/ExSCLA - N8 (N) N6 (N) PG3/EXIRQ13/ExSCLA - M9 (N) - NC 56 (N) P8 (N) K7 (N) PG3/EXIRQ17/SD2L - M9 (N) N7 (N) PG1/EXIRQ17/SD2L - M9 (N) N7 (N) PG1/EXIRQ17/SD2L 57 (N) </th <th></th> <th>Pin No</th> <th></th> <th>Pin Name</th>		Pin No		Pin Name
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47 N6 L5 PF3/IRQ11/TMOX/TDPCKI0/TDPMCI0 48 R6 M6 PF2/IRQ10/TMOY/TDPCYI0 49 P6 N5 PF1/IRQ9/PWMU1A 50 M7 K5 PF0/IRQ6/PWMU0A - N7 (N) - PI1 51 (N) R7 (N) L6 (N) PG7/EXIRQ15/ExSCLB 52 (N) P7 (N) M7 (N) PG6/EXIRQ14/ExSDAB 53 (N) M8 (N) N6 (N) PG5/EXIRQ13/ExSCLA - N8 (N) - PI0 54 (N) R6 (N) PG4/EXIRQ12/ExSDAA 55 (N) P8 (N) K7 (N) PG3/EXIRQ11/SCL2 - M9 (N) - NC 56 (N) N9 (N) K8 (N) PG2/EXIRQ10/SDA2 57 (N) R9 (N) N7 (N) PG1/EXIRQ8/TMIX/TDPCKI1/TDPMCI1 58 (N) P9 (N) M8 (N) PG0/EXIRQ8/TMIX/TDPCYI1 59 M10 L7 PD7/AN15 60 N10 K9 PD6/AN14 61 R10	45	R5	N4	PF5/PWMU3A
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58 (N) P9 (N) M8 (N) PG0/ExIRQ8/TMIX/TDPCYI1 59 M10 L7 PD7/AN15 60 N10 K9 PD6/AN14 61 R10 N8 PD5/AN13 62 P10 M9 PD4/AN12 63 N11 L8 PD3/AN11 64 R11 K10 PD2/AN10 65 P11 N9 PD1/AN9 66 M11 M10 PD0/AN8 67 R12 L9 AVSS - P12 - AVSS 68 N12 N10 P70/AN0	56 (N)	N9 (N)	K8 (N)	PG2/ExIRQ10/SDA2
59 M10 L7 PD7/AN15 60 N10 K9 PD6/AN14 61 R10 N8 PD5/AN13 62 P10 M9 PD4/AN12 63 N11 L8 PD3/AN11 64 R11 K10 PD2/AN10 65 P11 N9 PD1/AN9 66 M11 M10 PD0/AN8 67 R12 L9 AVSS P12 AVSS 68 N12 N10 P70/AN0	57 (N)	R9 (N)	N7 (N)	PG1/ExIRQ9/TMIY/TDPCKI1/TDPMCI1
60 N10 K9 PD6/AN14 61 R10 N8 PD5/AN13 62 P10 M9 PD4/AN12 63 N11 L8 PD3/AN11 64 R11 K10 PD2/AN10 65 P11 N9 PD1/AN9 66 M11 M10 PD0/AN8 67 R12 L9 AVSS P12 AVSS 68 N12 N10 P70/AN0	58 (N)	P9 (N)	M8 (N)	PG0/ExIRQ8/TMIX/TDPCYI1
61 R10 N8 PD5/AN13 62 P10 M9 PD4/AN12 63 N11 L8 PD3/AN11 64 R11 K10 PD2/AN10 65 P11 N9 PD1/AN9 66 M11 M10 PD0/AN8 67 R12 L9 AVSS P12 AVSS 68 N12 N10 P70/AN0	59	M10	L7	PD7/AN15
62 P10 M9 PD4/AN12 63 N11 L8 PD3/AN11 64 R11 K10 PD2/AN10 65 P11 N9 PD1/AN9 66 M11 M10 PD0/AN8 67 R12 L9 AVSS P12 AVSS 68 N12 N10 P70/AN0	60	N10	K9	PD6/AN14
63 N11 L8 PD3/AN11 64 R11 K10 PD2/AN10 65 P11 N9 PD1/AN9 66 M11 M10 PD0/AN8 67 R12 L9 AVSS P12 AVSS 68 N12 N10 P70/AN0	61	R10	N8	PD5/AN13
64 R11 K10 PD2/AN10 65 P11 N9 PD1/AN9 66 M11 M10 PD0/AN8 67 R12 L9 AVSS P12 AVSS 68 N12 N10 P70/AN0	62	P10	M9	PD4/AN12
65 P11 N9 PD1/AN9 66 M11 M10 PD0/AN8 67 R12 L9 AVSS P12 AVSS 68 N12 N10 P70/AN0	63	N11	L8	PD3/AN11
66 M11 M10 PD0/AN8 67 R12 L9 AVSS P12 AVSS 68 N12 N10 P70/AN0	64	R11	K10	PD2/AN10
67 R12 L9 AVSS P12 AVSS 68 N12 N10 P70/AN0	65	P11	N9	PD1/AN9
P12 AVSS 68 N12 N10 P70/AN0	66	M11	M10	PD0/AN8
68 N12 N10 P70/AN0	67	R12	L9	AVSS
	_	P12		AVSS
69 R13 M11 P71/AN1	68	N12	N10	P70/AN0
	69	R13	M11	P71/AN1

1.4.3 Pin Functions

Table 1.4Pin Functions

Pin No.						
Туре	Symbol	TFP-144V	BP-176V	TLP-145V	I/O	Name and Function
Power supply	VCC	1, 36, 86	A1, J15, P1, P2	B1, M1, H10	Input	Power supply pins. Connect all these pins to the system power supply. Connect the bypass capacitor between VCC and VSS (that is located near these pins).
	VCL	13	F1	E1	Input	External capacitance pin for internal step-down power. Connect this pin to VSS through an external capacitor (that is located near this pin) to stabilize internal step-down power.
	VSS	7, 42, 95, 111, 139	D1, D2, P4, R4, F12, F13, B13, A13, A4, B4	D2, L3, F10, B11, C5	Input	Ground pins. Connect all these pins to the system power supply (0 V).
Clock	XTAL	143	A2	A3	Input	For connection to a crystal
	EXTAL	144	B2	A2	Input	resonator. An external clock can be supplied from the EXTAL pin. For an example of crystal resonator connection, see section 25, Clock Pulse Generator.
	φ	18	H1	F4	Output	Supplies the system clock to external devices.
	EXCL	18	H1	F4	Input	32.768 kHz external sub clock
	ExEXCL	32	M3	K1	Input	should be supplied. To which pin the external clock is input can be selected from the EXCL or ExEXCL pin.
Operating mode control	MD2 MD1	25 9	K1 E2	H1 D1	Input	These pins set the operating mode. Inputs at these pins should not be changed during operation.
System control	RES	8	E3	D3	Input	Reset pin. When this pin is low, the chip is reset.

RENESAS

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Rev. 2.00 Sep. 28, 2009 Page 19 of 994 REJ09B0452-0200

2.4.1 General Registers

The H8S/2600 CPU has eight 32-bit general registers. These general registers are all functionally identical and can be used as both address registers and data registers. When a general register is used as a data register, it can be accessed as a 32-bit, 16-bit, or 8-bit register. Figure 2.7 illustrates the usage of the general registers. When the general registers are used as 32-bit registers or address registers, they are designated by the letters ER (ER0 to ER7).

The ER registers divide into 16-bit general registers designated by the letters E (E0 to E7) and R (R0 to R7). These registers are functionally equivalent, providing a maximum of sixteen 16-bit registers. The E registers (E0 to E7) are also referred to as extended registers.

The R registers divide into 8-bit general registers designated by the letters RH (R0H to R7H) and RL (R0L to R7L). These registers are functionally equivalent, providing a maximum of sixteen 8-bit registers.

The usage of each register can be selected independently.

General register ER7 has the function of stack pointer (SP) in addition to its general-register function, and is used implicitly in exception handling and subroutine calls. Figure 2.8 shows the stack.

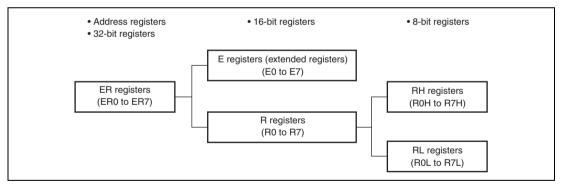


Figure 2.7 Usage of General Registers



Instructio	on S	Size*	Function
ADD SUB	E	3/W/L	$Rd \pm Rs \rightarrow Rd$, $Rd \pm \#IMM \rightarrow Rd$ Performs addition or subtraction on data in two general registers, or on immediate data and data in a general register (immediate byte data cannot be subtracted from byte data in a general register. Use the SUBX or ADD instruction.)
ADDX SUBX	E	3	$Rd \pm Rs \pm C \rightarrow Rd$, $Rd \pm \#IMM \pm C \rightarrow Rd$ Performs addition or subtraction with carry on byte data in two general registers, or on immediate data and data in a general register.
INC DEC	E	3/W/L	$Rd \pm 1 \rightarrow Rd$, $Rd \pm 2 \rightarrow Rd$ Increments or decrements a general register by 1 or 2. (Byte operands can be incremented or decremented by 1 only.)
ADDS SUBS	L	_	$Rd \pm 1 \rightarrow Rd$, $Rd \pm 2 \rightarrow Rd$, $Rd \pm 4 \rightarrow Rd$ Adds or subtracts the value 1, 2, or 4 to or from data in a 32-bit register.
DAA DAS	E	3	Rd decimal adjust \rightarrow Rd Decimal-adjusts an addition or subtraction result in a general register by referring to the CCR to produce 4-bit BCD data.
MULXU	E	3/W	$Rd \times Rs \rightarrow Rd$ Performs unsigned multiplication on data in two general registers: either 8 bits × 8 bits \rightarrow 16 bits or 16 bits × 16 bits \rightarrow 32 bits.
MULXS	E	3/W	$Rd \times Rs \rightarrow Rd$ Performs signed multiplication on data in two general registers: either 8 bits \times 8 bits \rightarrow 16 bits or 16 bits \times 16 bits \rightarrow 32 bits.
DIVXU	E	3/W	Rd ÷ Rs → Rd Performs unsigned division on data in two general registers: either 16 bits ÷ 8 bits → 8-bit quotient and 8-bit remainder or 32 bits ÷ 16 bits → 16-bit quotient and 16-bit remainder.
Note: *	Refer	s to the	operand size.
		Byte Vord	

Arithmetic Operations Instructions (1) Table 2.4

L: Longword

Origin of		N (Vector Address		
Interrupt Source	Name	Vector Number	Advanced Mode	ICR	Priority
_	Reserved for system use	24	H'000060	_	High
WDT_0	WOVI0 (Interval timer)	25	H'000064	ICRA1	_ ↑
WDT_1	WOVI1 (Interval timer)	26	H'000068	ICRA0	-
_	Address break	27	H'00006C	_	-
A/D converter	ADI (A/D conversion end)	28	H'000070	ICRB7	-
_	Reserved for system use	29	H'000074	_	-
		32	H'000080		
External pin	WUE15 to WUE8	33	H'000084	ICRD4	-
TPU_0	TGI0A (TGR0A input	34	H'000088	ICRD3	-
	capture/compare match) TGI0B (TGR0B input capture/compare match)	35	H'00008C		
	TGI0C (TGR0C input	36	H'000090		
	capture/compare match) TGI0D (TGR0D input capture/compare match)	37	H'000094		
	TGI0V (Overflow 0)	38	H'000098		
TPU_1	TGI1A (TGR1A input	39	H'00009C	ICRD2	_
	capture/compare match) TGI1B (TGR1B input capture/compare match)	40	H'0000A0		
	TGI1V (Overflow 1)	41	H'0000A4		
	TGI1U (Underflow 1)	42	H'0000A8		
TPU_2	TGI2A (TGR2A input capture/compare match)	43	H'0000AC	ICRD1	_
	TGI2B (TGR2B input capture/compare match)	44	H'0000B0		
	TGI2V (Overflow 2)	45	H'0000B4		
	TGI2U (Underflow 2)	46	H'0000B8		
_	Reserved for system use	47	H'0000BC	_	
TCM_0	TICI0 (Input capture) TCMI0 (Compare match) TOVMI0 (Cycle overflow) TUDI0 (Cycle underflow) TOVI0 (Overflow)	48	H'0000C0	ICRB6	_
TCM_1	TICI1 (Input capture) TCMI1 (Compare match) TOVMI1 (Cycle overflow) TUDI1 (Cycle underflow) TOVI1 (Overflow)	49	H'0000C4	_	Low

Origin of Interrupt		Vector	Vector Address		
Source	Name	Number	Advanced Mode	ICR	Priority
SCI_2	ERI2 (Reception error)	88	H'000160	ICRC5	High
	RXI2 (Reception completion) TXI2 (Transmission data empty 2)	89 90	H'000164 H'000168		
	TEI2 (Transmission end 2)	90 91	H'00016C		
IIC_0	IICI0 (1-byte transmission/reception completion)	92	H'000170	ICRC4	-
CIR	RENDI (Reception end) OVEI (Overrun error) REPI (Repeat detection) FREI (Framing error) ABI (Abort) HEADFI (Header detection)	93	H'000174	ICRB4	-
IIC_1	IICI1 (1-byte transmission/reception completion)	94	H'000178	ICRC3	-
IIC_2	IICl2 (1-byte transmission/reception completion)	95	H'00017C		
PS2	KBIA (Reception completion A)	96	H'000180	ICRB0	-
	KBIB (Reception completion B)	97	H'000184		
	KBIC (Reception completion C)	98	H'000188		
	KBTIA (Transmission completion A)/ KBCA (1st KCLKA)	99	H'00018C		
	KBTIB (Transmission completion B)/ KBCB (1st KCLKB)	100	H'000190		
	KBTIC (Transmission completion C)/ KBCC (1st KCLKC)	101	H'000194		
	KBID (Reception completion D)	102	H'000198		
	KBTID (Transmission completion D)/KBCD (1st KCLKD)	103	H'00019C		
FSI	LFSII (Command reception)/(Write reception)	104	H'0001A0	ICRC1	-
_	Reserved for system use	105	H'0001A4	—	-
LPC	OBEI (ODR1 to 4 transmission completion)	106	H'0001A8	ICRC1	-
	IBFI4 (IDR4 reception completion)	107	H'0001AC		
	ERR1 (Transfer error, etc.)	108	H'0001B0		
	IBFI1 (IDR1 reception completion)	109	H'0001B4		
	IBFI2 (IDR2 reception completion)	110	H'0001B8		
	IBFI3 (IDR3 reception completion)	111	H'0001BC		_
	Reserved for system use	112	H'0001C0		
		127	H'0001FC		Low

5.6.2 Interrupt Control Mode 1

In interrupt control mode 1, mask control is applied to three levels for interrupt requests other than NMI and address break by comparing the I and UI bits in CCR in the CPU, and the ICR setting.

- An interrupt request with interrupt control level 0 is accepted when the I bit in CCR is cleared to 0. When the I bit is set to 1, the interrupt request is held pending.
- An interrupt request with interrupt control level 1 is accepted when the I bit or UI bit in CCR is cleared to 0. When both the I and UI bits are set to 1, the interrupt request is held pending.

For instance, the state transition when the interrupt enable bit corresponding to each interrupt is set to 1, and ICRA to ICRD are set to H'20, H'00, H'00, and H'00, respectively (IRQ2 and IRQ3 interrupts are set to interrupt control level 1, and other interrupts are set to interrupt control level 0) is shown below. Figure 5.8 shows a state transition diagram.

- All interrupt requests are accepted when I = 0. (Priority order: NMI > IRQ2 > IRQ3 > address break > IRQ0 > IRQ1 ...)
- Only NMI, IRQ2, IRQ3, and address break interrupt requests are accepted when I = 1 and UI = 0.
- Only NMI and address break interrupt requests are accepted when I = 1 and UI = 1.

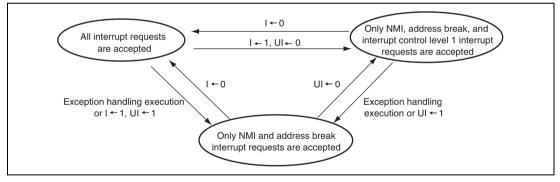


Figure 5.8 State Transition in Interrupt Control Mode 1

8.3.3 PWM Control Register C (PWMCONC)

PWMCONC selects the PWM count mode and operating mode for each channel.

Bit	Bit Name	Initial Value	R/W	Description
7		0	R/W	Reserved
				The initial value should not be changed.
6	CNTMD01	0	R/W	Channels 0 and 1 Counter Select
				0: Channels 0 and 1 are in 8-bit counter operation.
				 Channels 0 and 1 are in 16-bit counter operation (Upper: channel 1, lower: channel 0).
				Note: When the 16-bit counter is selected, specify single pulse mode.
5	PWMSL5	0	R/W	Channel 5 Operating Mode Select
				0: Single-pulse mode
				1: Pulse division mode (Specify 8-bit counter mode.)
4	PWMSL4	0	R/W	Channel 4 Operating Mode Select
				0: Single pulse mode
				1: Pulse division mode (Specify 8-bit counter mode.)
3	PWMSL3	0	R/W	Channel 3 Operating Mode Select
				0: Single pulse mode
				1: Pulse division mode (Specify 8-bit counter mode.)
2	PWMSL2	0	R/W	Channel 2 Operating Mode Select
				0: Single pulse mode
_				1: Pulse division mode (Specify 8-bit counter mode.)
1	PWMSL1	0	R/W	Channel 1 Operating Mode Select
				0: Single pulse mode
				1: Pulse division mode (Specify 8-bit counter mode.)
0	PWMSL0	0	R/W	Channel 0 Operating Mode Select
				0: Single pulse mode
				1: Pulse division mode (Specify 8-bit counter mode.)

(1) Example of Buffer Operation Setting Procedure

Figure 10.18 shows an example of the buffer operation setting procedure.

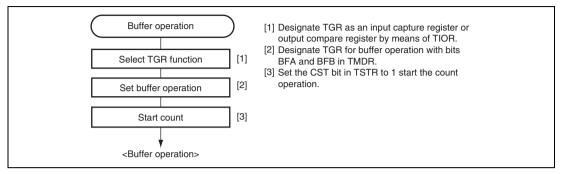


Figure 10.18 Example of Buffer Operation Setting Procedure



12.4 Operation

The TDP operates in timer mode or cycle measurement mode. After a reset, the TDP is in timer mode.

12.4.1 Timer Mode

When the TDPMDS bit in TDPCR1 is cleared to 0, the TDP operates in timer mode.

(1) Counter Operation

The TDP operates as a free-running counter in timer mode. The TDP starts counting up when the CST bit in TDPCR1 is set to 1. When TDPCNT overflows (H'FFFF changes to H'0000), the OVF bit in TDPCSR is set to 1 and an interrupt request is generated if the OVIE bit in TDPIER is 1. Figure 12.2 shows an example of free-running counter operation. In addition, figure 12.3 shows TDPCNT count timing for external clock operation. Note that the external clock requires a pulse width of at least 1.5 cycles. The counter will not operate correctly if the pulses are narrower than this.

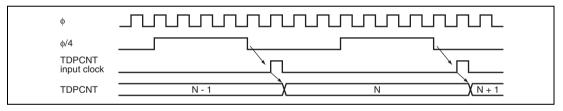


Figure 12.2 Example of Free-Running Counter Operation

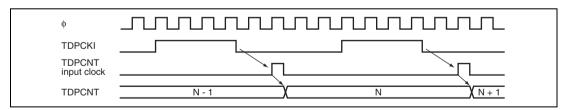


Figure 12.3 Count Timing of External Clock Operation (Falling Edges)

15.7.7 Serial Data Reception (Except in Block Transfer Mode)

Data reception in smart card interface mode is identical to that in normal serial communication interface mode. Figure 15.29 shows the data re-transfer operation during reception.

- 1. If a parity error is detected in receive data, the PER bit in SSR is set to 1. Here, an ERI interrupt request is generated if the RIE bit in SCR is set to 1. Clear the PER bit to 0 before the next parity bit is sampled.
- 2. For the frame in which a parity error is detected, the RDRF bit in SSR is not set to 1.
- 3. If no parity error is detected, the PER bit in SSR is not set to 1. In this case, data is determined to have been received successfully, and the RDRF bit in SSR is set to 1. Here, an RXI interrupt request is generated if the RIE bit in SCR is set.

Figure 15.30 shows a sample flowchart for reception. In reception, setting the RIE bit to 1 allows an RXI interrupt request to be generated when the RDRF flag is set to 1. If an error occurs during reception, i.e., either the ORER or PER flag is set to 1, a transmit/receive error interrupt (ERI) request is generated and the error flag must be cleared. Even if a parity error occurs and PER is set to 1 in reception, receive data is transferred to RDR, thus allowing the data to be read.

Note: For operations in block transfer mode, see section 15.4, Operation in Asynchronous Mode.

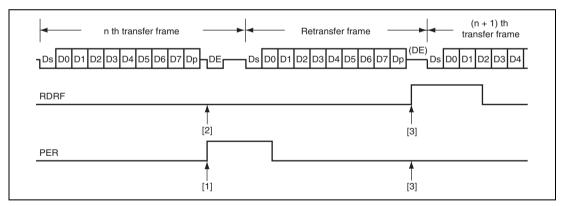


Figure 15.29 Data Re-transfer Operation in SCI Reception Mode

Section 19 Keyboard Buffer Control Unit (PS2)

This LSI has four on-chip keyboard buffer control unit (PS2) channels. The PS2 is provided with functions conforming to the PS/2 interface specifications.

Data transfer using the PS2 employs a data line (KD) and a clock line (KCLK), providing economical use of connectors, board surface area, etc. Figure 19.1 shows a block diagram of the PS2.

19.1 Features

- Conforms to PS/2 interface specifications
- Direct bus drive (via the KCLK and KD pins)
- Interrupt sources: on completion of data reception/transmission, on detection of clock falling edge, and on detection of the first falling edge of a clock
- Error detection: parity error, stop bit monitoring, and receive notify monitoring



24.8.3 User Boot Mode

This LSI has user boot mode that is initiated with different mode pin settings than those in boot mode or user program mode. User boot mode is a user-arbitrary boot mode, unlike boot mode that uses the on-chip SCI.

Only the user MAT can be programmed/erased in user boot mode. Programming/erasing of the user boot MAT is only enabled in boot mode or programmer mode.

(1) User Boot Mode Initiation

For the mode pin settings to start up user boot mode, see table 24.7.

When the reset start is executed in user boot mode, the built-in check routine runs. The user MAT and user boot MAT states are checked by this check routine.

While the check routine is running, NMI and all other interrupts cannot be accepted.

Next, processing starts from the execution start address of the reset vector in the user boot MAT. At this point, H'AA is set to FMATS because the execution target MAT is the user boot MAT.

(2) User MAT Programming in User Boot Mode

For programming the user MAT in user boot mode, additional processing made by setting FMATS is required: switching from user-boot-MAT selection state to user-MAT selection state, and switching back to user-boot-MAT selection state after programming completes.

Figure 24.14 shows the procedure for programming the user MAT in user boot mode.

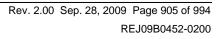


Function		High Speed	Medium Speed	Sleep	Module Stop	Watch	Software Standby
System clock pulse generator Subclock input		Functioning	Functioning	Functioning	Functioning	Stopped	Stopped
		Functioning	Functioning	Functioning	Functioning	Functioning	Stopped
CPU	Instruction execution	Functioning	Medium-speed operation	Stopped	Functioning	Stopped	Stopped
	Registers	-		Retained	-	Retained	Retained
External interrupts	NMI	Functioning	Functioning	Functioning	Functioning	Functioning	Functioning
interrupts	IRQ0 to IRQ15	-					
	KIN0 to KIN15	-					
	WUE8 to WUE15	-					
On-chip	WDT_1	Functioning	Functioning	Functioning	Functioning	Subclock	Stopped
peripheral modules	CIR	-				operation	(retained)
	WDT_0	-				Stopped	_
	TMR_0, TMR_1	-			Functioning/ stopped	(retained)	
	TPU TCM_0 to 3 TDP_0 to 2	-			(retained)		
	TMR_X, TMR_Y	-					
	SCIF	-					
	IIC_0 to 2	-					
	LPC	-					
	FSI						
	PS2_0 to 3	_	Medium-speed operation/functioning				
	PWMU	-	Functioning	-	Functioning/	Stopped	Stopped
	PWM	-			stopped (reset)	(reset)	(reset)
	PWMX	-			(
	SCI_1, SCI_2	-					
	A/D converter	-					
	RAM	Functioning	Functioning	Functioning	Functioning	Retained	Retained
	I/O	Functioning	Functioning	Functioning	Functioning	Retained	Retained

Table 26.3 LSI Internal States in Each Operating Mode

Note: Stopped (retained) means that the internal register values are retained and the internal state is operation suspended. Stopped (reset) means that the internal register values and the internal state are initialized. In module stop mode, only modules for which a stop setting has been made are stopped (reset or retained).

Abbreviation Reset speed Watch Sleep Stop Standby Module IDR1 Initialized LPC ODR1 Initialized LPC STR1 Initialized <t< th=""><th>Register</th><th></th><th>High- Speed/Medium</th><th></th><th></th><th>Module</th><th>Software</th><th></th></t<>	Register		High- Speed/Medium			Module	Software	
ODR1 Initialized - - - - STR1 Initialized - - - - - SIRQCR4 Initialized - - - - - DR2 Initialized - - - - - - ODR2 Initialized - - - - - - STR2 Initialized - - - - - - HICR1 Initialized - - - - - - HICR2 - - - - - - - HICR3 - - - - - - PORT PGDDR Initialized - - - - - PORT PGDDR Initialized - - - - - - PFDDR Initialized - -	•	Reset	•	Watch	Sleep			Module
STR1 Initialized -	IDR1	Initialized		_	_	_		LPC
SIRQCR4 Initialized IDR2 Initialized ODR2 Initialized STR2 Initialized HISEL Initialized HICR0 Initialized HICR1 Initialized HICR3 PORT PGDDR Initialized PORT PGPIN PGDDR Initialized PORT PGDR PFODR Initialized PORT PGPIN PORT PGPIN	ODR1	Initialized			_	_		
IDR2 Initialized ODR2 Initialized STR2 Initialized HISEL Initialized HICR0 Initialized HICR1 Initialized HICR3 WEMR Initialized PGODR Initialized PGDDR Initialized PGDDR Initialized PFDDR Initialized PFDDR Initialized PFDDR Initialized PCDDR Initialized <t< td=""><td>STR1</td><td>Initialized</td><td></td><td></td><td>_</td><td>_</td><td></td><td></td></t<>	STR1	Initialized			_	_		
ODR2 Initialized STR2 Initialized HISEL Initialized HICR0 Initialized HICR1 Initialized HICR3 WUEMR Initialized PORT PORT PGODR Initialized PORT PGDDR Initialized PORT PFDDR Initialized PORT PFDDR Initialized PFDIN	SIRQCR4	Initialized		_	_	_		
STR2 Initialized HISEL Initialized HICR0 Initialized HICR1 Initialized HICR2 HICR3 WUEMR Initialized PORT PGODR Initialized PORT PGDDR Initialized PORT PGDDR Initialized PORT PFDR Initialized PFDR Initialized PCODR Initialized <t< td=""><td>IDR2</td><td>Initialized</td><td></td><td></td><td>_</td><td>_</td><td></td><td></td></t<>	IDR2	Initialized			_	_		
HISEL Initialized HICR0 Initialized HICR1 Initialized HICR2 HICR3 VUEMR Initialized PORT PGODR Initialized PORT PORT PGDDR Initialized PORT PGDDR Initialized PORT PFDR Initialized PORT PFDR Initialized PORT PFDR Initialized PCODR Initialized	ODR2	Initialized		—	_	_	_	_
HICR0 Initialized HICR1 Initialized HICR2 HICR3 WUEMR Initialized PORT PGODR Initialized PORT PGDDR Initialized PORT PGDDR Initialized PORT PGDDR Initialized PORT PFDR Initialized PORT PFDR Initialized PORT PFDR Initialized PORT POPDR Initialized <td< td=""><td>STR2</td><td>Initialized</td><td></td><td>—</td><td>_</td><td>_</td><td>_</td><td>_</td></td<>	STR2	Initialized		—	_	_	_	_
HICR1 Initialized HICR2 HICR3 WUEMR Initialized INT PGODR Initialized PORT PGDDR Initialized PORT PGDDR Initialized PORT PFODR Initialized PORT PFDDR Initialized PFDDR Initialized PCODR Initialized PCDDR Initialized PDDR Initialized <	HISEL	Initialized		—	_	_	_	_
HICR2 HICR3 INT PGODR Initialized INT PGODR Initialized PORT PGDIN PORT PGDDR Initialized PORT PGDDR Initialized PFODR Initialized PFDIN PFDR Initialized PCODR Initialized PCDDR Initialized PDDR Initialized <td>HICR0</td> <td>Initialized</td> <td></td> <td>—</td> <td>_</td> <td>_</td> <td>_</td> <td>_</td>	HICR0	Initialized		—	_	_	_	_
HICR3 WUEMR Initialized INT PGODR Initialized PORT PGDDR Initialized PORT PGDDR Initialized PGDDR Initialized PFODR Initialized PFDDR Initialized PFDDR Initialized PCODR Initialized PCDDR Initialized PCDDR Initialized PCDDR Initialized PDDR Initialized TORH_0 Initialized	HICR1	Initialized	_	_	_	_	_	_
WUEMR Initialized INT PGODR Initialized PORT PGDIN PORT PGDDR Initialized PGDDR Initialized PFODR Initialized PFDDR Initialized PFDDR Initialized PFDDR Initialized PCODR Initialized PCDDR Initialized PCDDR Initialized PDDDR Initialized TORL_0 Initialized	HICR2	_		_	_	_		_
PGODR Initialized PORT PGPIN PORT PGDDR Initialized PFODR Initialized PFDR Initialized PFDIN PFDDR Initialized	HICR3	_		_	_	_		_
PGPIN PGDDR Initialized PFODR Initialized PEPIN PFDDR Initialized PFDDR Initialized PCDDR Initialized PCDDR Initialized </td <td>WUEMR</td> <td>Initialized</td> <td></td> <td>_</td> <td>_</td> <td>_</td> <td></td> <td>INT</td>	WUEMR	Initialized		_	_	_		INT
PGDDR Initialized PFODR Initialized PEPIN PFPIN PFDIR Initialized PFDDR Initialized PCODR Initialized PCODR Initialized PCDDR Initialized PDDR Initialized PDDDR Initialized TIORH_0 Initialized	PGODR	Initialized	_		_	_		PORT
PFODR Initialized PEPIN PFPIN PFDDR Initialized PCODR Initialized PDODR Initialized PCDR Initialized PCDDR Initialized PCDDR Initialized PDDR Initialized PDDR Initialized TOR_0 Initialized TIORL_0 Initialized	PGPIN	_	_		_	_		
PEPIN P P P P P P P Initialized P P P Initialized P P P Initialized P P P Initialized P P P P P P P P P P P P P P P P P P P P P P P P P P P P </td <td>PGDDR</td> <td>Initialized</td> <td>—</td> <td>_</td> <td>_</td> <td>_</td> <td>_</td> <td></td>	PGDDR	Initialized	—	_	_	_	_	
PFPIN PFDDR Initialized PCODR Initialized PDODR Initialized PDDR Initialized PCPIN PCDDR Initialized PDDR Initialized PDDR Initialized PDDR Initialized PDDR Initialized TPU_0 TMDR_0 Initialized TIORL_0 Initialized TIER_0 Initialized	PFODR	Initialized	—	_	_	_	_	
PFDDR Initialized PCODR Initialized PDDDR Initialized PCPIN PCDDR Initialized PCDDR Initialized PDDR Initialized PDDR Initialized TCR_0 Initialized TIORH_0 Initialized TIORL_0 Initialized TIRR_0 Initialized	PEPIN	_	—	_	_	_	_	
PCODR Initialized PDODR Initialized PCPIN PCDDR Initialized PCDDR Initialized PDDR Initialized PDDDR Initialized PDDDR Initialized TCR_0 Initialized TIORH_0 Initialized TIORL_0 Initialized TIER_0 Initialized TSR_0 Initialized	PFPIN	_		_	_	_		_
PDODR Initialized PCPIN PCDDR Initialized PDPIN PDDDR Initialized PDDDR Initialized TCR_0 Initialized TMDR_0 Initialized TIORH_0 Initialized <t< td=""><td>PFDDR</td><td>Initialized</td><td></td><td>_</td><td>_</td><td>_</td><td></td><td>_</td></t<>	PFDDR	Initialized		_	_	_		_
PCPIN — — — — — — — — — P PCDDR Initialized — — — — — — P	PCODR	Initialized		_	_	_		_
PCDDR Initialized PDPIN PDPIN PDPIN PDPIN PDPIN PDDDR Initialized PDDDR Initialized PDD_0 Initialized PDU_0 Initialized PDU_0 Initialized PDU_0 Initialized PDU_0 Initialized PDU_0 Initialized	PDODR	Initialized	—	_	_	_	_	
PDPIN	PCPIN	_	—	_	_	_	_	
PDDDR Initialized TPU_0 TCR_0 Initialized TPU_0 TMDR_0 Initialized	PCDDR	Initialized	—	_	_	_	_	
TCR_0 Initialized - - - - TPU_0 TMDR_0 Initialized - - - - - - TIORH_0 Initialized - - - - - - TIORL_0 Initialized - - - - - - TIER_0 Initialized - - - - - - - TSR_0 Initialized - - - - - - - -	PDPIN	_	—	_	_	_	_	
TMDR_0 Initialized TIORH_0 Initialized TIORL_0 Initialized TIORL_0 Initialized TIER_0 Initialized TSR_0 Initialized	PDDDR	Initialized		_	_	_		_
TIORH_0 Initialized TIORL_0 Initialized TIER_0 Initialized TSR_0 Initialized	TCR_0	Initialized		_	_	_		TPU_0
TIORL_0 Initialized TIER_0 Initialized TSR_0 Initialized	TMDR_0	Initialized	_	_	_	_	_	
TIER_0 Initialized — — — — TSR_0 Initialized — — — — —	TIORH_0	Initialized	_	_				
TSR_0 Initialized	TIORL_0	Initialized		_	_	_		_
	TIER_0	Initialized		_	_	_	_	
TCNT_0 Initialized	TSR_0	Initialized		_	_	_	_	
	TCNT_0	Initialized		_	_	_		_



Module	Register Abbreviation	Number of Bits	Address	Data Bus Width	Access States
PORT	PFODR	8	H'F973 (PORTS = 1)	8	2
PORT	PEPIN	8	H'F974 (Read) (PORTS = 1)	8	2
PORT	PFPIN	8	H'F975 (Read) (PORTS = 1)	8	2
PORT	PFPCR	8	H'F977 (PORTS = 1)	8	2
PORT	PFNOCR	8	H'F979 (PORTS = 1)	8	2
PORT	PGDDR	8	H'F980 (PORTS = 1)	8	2
PORT	PHDDR	8	H'F981 (PORTS = 1)	8	2
PORT	PGODR	8	H'F982 (PORTS = 1)	8	2
PORT	PHODR	8	H'F983 (PORTS = 1)	8	2
PORT	PGPIN	8	H'F984 (Read) (PORTS = 1)	8	2
PORT	PHPIN	8	H'F985 (Read) (PORTS = 1)	8	2
PORT	PHPCR	8	H'F987 (PORTS = 1)	8	2
PORT	PGNOCR	8	H'F988 (PORTS = 1)	8	2
PORT	PHNOCR	8	H'F989 (PORTS = 1)	8	2
PORT	PGNCE	8	H'F98A (PORTS = 1)	8	2
PORT	PGNCMC	8	H'F98C (PORTS = 1)	8	2
PORT	PGNCCS	8	H'F98E (PORTS = 1)	8	2
PORT	PIDDR	8	H'F990	8	2
PORT	PJDDR	8	H'F991	8	2

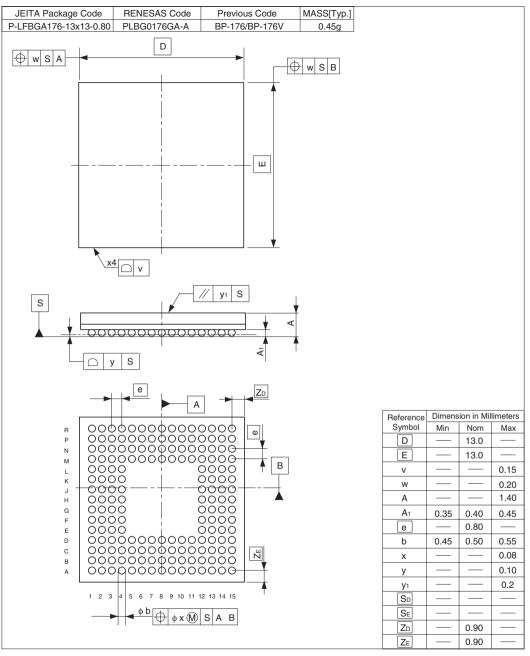


Figure C.2 Package Dimensions (BP-176V)