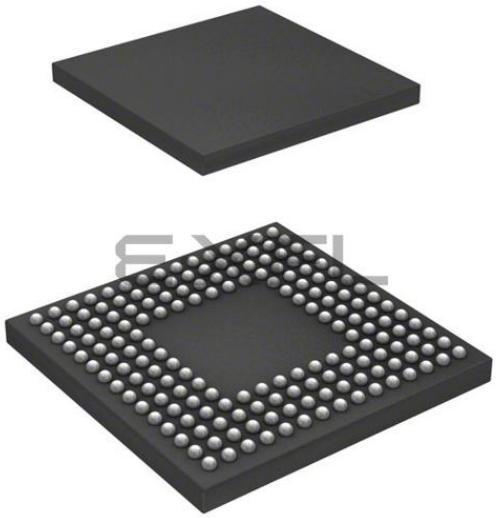

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Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
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Oscillator Type	External
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2. Description of Numbers and Symbols

Aspects of the notations for register names, bit names, numbers, and symbolic names in this manual are explained below.

(1) Overall notation

In descriptions involving the names of bits and bit fields within this manual, the modules and registers to which the bits belong may be clarified by giving the names in the forms "module name"."register name"."bit name" or "register name"."bit name".

(2) Register notation

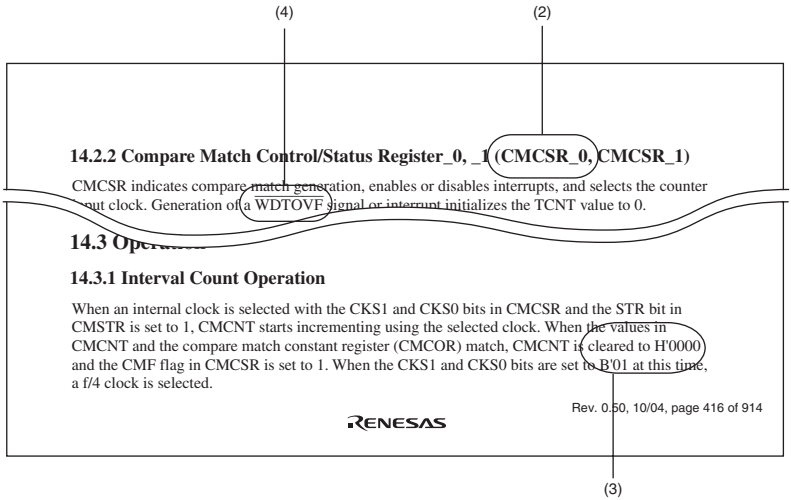
The style "register name"_"instance number" is used in cases where there is more than one instance of the same function or similar functions.
[Example] CMCSR_0: Indicates the CMCSR register for the compare-match timer of channel 0.

(3) Number notation

Binary numbers are given as B'nnnn (B' may be omitted if the number is obviously binary), hexadecimal numbers are given as H'nnnn or 0xnnnn, and decimal numbers are given as nnnn.
[Examples] Binary: B'11 or 11
Hexadecimal: H'EFA0 or 0xEFA0
Decimal: 1234

(4) Notation for active-low

An overbar on the name indicates that a signal or pin is active-low.
[Example] $\overline{\text{WDTOVF}}$



Note: The bit names and sentences in the above figure are examples and have nothing to do with the contents of this manual.

Contents

Pin No.			Pin Name
TFP-144V	BP-176V	TLP-145V	Single-Chip Mode
			Mode 2 (EXPE = 0)
45	R5	N4	PF5/PWMU3A
46	M6	M5	PF4/PWMU2A
47	N6	L5	PF3/$\overline{\text{IRQ11}}$/TMOX/TDPCKI0/TDPMCI0
48	R6	M6	PF2/$\overline{\text{IRQ10}}$/TMOY/TDPCYI0
49	P6	N5	PF1/$\overline{\text{IRQ9}}$/PWMU1A
50	M7	K5	PF0/$\overline{\text{IRQ8}}$/PWMU0A
—	N7 (N)	—	PI1
51 (N)	R7 (N)	L6 (N)	PG7/$\overline{\text{ExIRQ15}}$/ExSCLB
52 (N)	P7 (N)	M7 (N)	PG6/$\overline{\text{ExIRQ14}}$/ExSDAB
53 (N)	M8 (N)	N6 (N)	PG5/$\overline{\text{ExIRQ13}}$/ExSCLA
—	N8 (N)	—	PI0
54 (N)	R8 (N)	K6 (N)	PG4/$\overline{\text{ExIRQ12}}$/ExSDAA
55 (N)	P8 (N)	K7 (N)	PG3/$\overline{\text{ExIRQ11}}$/SCL2
—	M9 (N)	—	NC
56 (N)	N9 (N)	K8 (N)	PG2/$\overline{\text{ExIRQ10}}$/SDA2
57 (N)	R9 (N)	N7 (N)	PG1/$\overline{\text{ExIRQ9}}$/TMIY/TDPCKI1/TDPMCI1
58 (N)	P9 (N)	M8 (N)	PG0/$\overline{\text{ExIRQ8}}$/TMIX/TDPCYI1
59	M10	L7	PD7/AN15
60	N10	K9	PD6/AN14
61	R10	N8	PD5/AN13
62	P10	M9	PD4/AN12
63	N11	L8	PD3/AN11
64	R11	K10	PD2/AN10
65	P11	N9	PD1/AN9
66	M11	M10	PD0/AN8
67	R12	L9	AVSS
—	P12	—	AVSS
68	N12	N10	P70/AN0
69	R13	M11	P71/AN1

1.4.3 Pin Functions

Table 1.4 Pin Functions

Type	Symbol	Pin No. TFP-144V	BP-176V	TLP-145V	I/O	Name and Function
Power supply	VCC	1, 36, 86	A1, J15, P1, P2	B1, M1, H10	Input	Power supply pins. Connect all these pins to the system power supply. Connect the bypass capacitor between VCC and VSS (that is located near these pins).
	VCL	13	F1	E1	Input	External capacitance pin for internal step-down power. Connect this pin to VSS through an external capacitor (that is located near this pin) to stabilize internal step-down power.
	VSS	7, 42, 95, 111, 139	D1, D2, P4, R4, F12, F13, B13, A13, A4, B4	D2, L3, F10, B11, C5	Input	Ground pins. Connect all these pins to the system power supply (0 V).
Clock	XTAL	143	A2	A3	Input	For connection to a crystal resonator. An external clock can be supplied from the EXTAL pin. For an example of crystal resonator connection, see section 25, Clock Pulse Generator.
	EXTAL	144	B2	A2	Input	
	ϕ	18	H1	F4	Output	Supplies the system clock to external devices.
	EXCL	18	H1	F4	Input	32.768 kHz external sub clock should be supplied. To which pin the external clock is input can be selected from the EXCL or ExEXCL pin.
	ExEXCL	32	M3	K1	Input	
Operating mode control	MD2 MD1	25 9	K1 E2	H1 D1	Input	These pins set the operating mode. Inputs at these pins should not be changed during operation.
System control	$\overline{\text{RES}}$	8	E3	D3	Input	Reset pin. When this pin is low, the chip is reset.

2.4.1 General Registers

The H8S/2600 CPU has eight 32-bit general registers. These general registers are all functionally identical and can be used as both address registers and data registers. When a general register is used as a data register, it can be accessed as a 32-bit, 16-bit, or 8-bit register. Figure 2.7 illustrates the usage of the general registers. When the general registers are used as 32-bit registers or address registers, they are designated by the letters ER (ER0 to ER7).

The ER registers divide into 16-bit general registers designated by the letters E (E0 to E7) and R (R0 to R7). These registers are functionally equivalent, providing a maximum of sixteen 16-bit registers. The E registers (E0 to E7) are also referred to as extended registers.

The R registers divide into 8-bit general registers designated by the letters RH (R0H to R7H) and RL (R0L to R7L). These registers are functionally equivalent, providing a maximum of sixteen 8-bit registers.

The usage of each register can be selected independently.

General register ER7 has the function of stack pointer (SP) in addition to its general-register function, and is used implicitly in exception handling and subroutine calls. Figure 2.8 shows the stack.

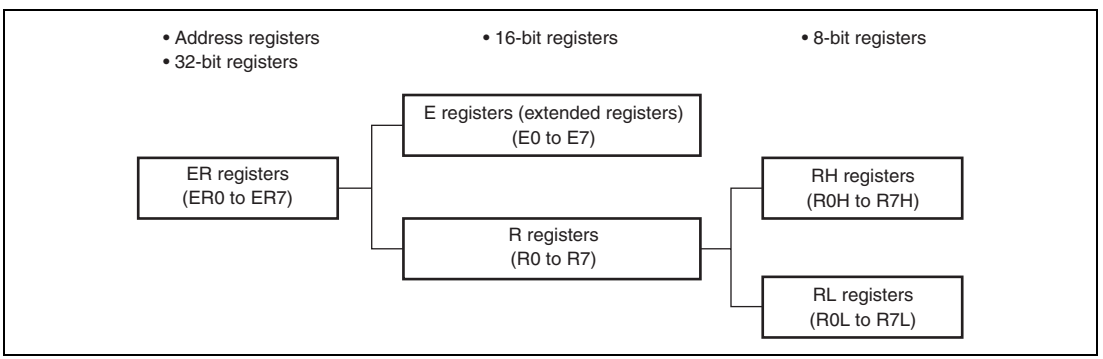


Figure 2.7 Usage of General Registers

Table 2.4 Arithmetic Operations Instructions (1)

Instruction	Size*	Function
ADD SUB	B/W/L	Rd ± Rs → Rd, Rd ± #IMM → Rd Performs addition or subtraction on data in two general registers, or on immediate data and data in a general register (immediate byte data cannot be subtracted from byte data in a general register. Use the SUBX or ADD instruction.)
ADDX SUBX	B	Rd ± Rs ± C → Rd, Rd ± #IMM ± C → Rd Performs addition or subtraction with carry on byte data in two general registers, or on immediate data and data in a general register.
INC DEC	B/W/L	Rd ± 1 → Rd, Rd ± 2 → Rd Increments or decrements a general register by 1 or 2. (Byte operands can be incremented or decremented by 1 only.)
ADDS SUBS	L	Rd ± 1 → Rd, Rd ± 2 → Rd, Rd ± 4 → Rd Adds or subtracts the value 1, 2, or 4 to or from data in a 32-bit register.
DAA DAS	B	Rd decimal adjust → Rd Decimal-adjusts an addition or subtraction result in a general register by referring to the CCR to produce 4-bit BCD data.
MULXU	B/W	Rd × Rs → Rd Performs unsigned multiplication on data in two general registers: either 8 bits × 8 bits → 16 bits or 16 bits × 16 bits → 32 bits.
MULXS	B/W	Rd × Rs → Rd Performs signed multiplication on data in two general registers: either 8 bits × 8 bits → 16 bits or 16 bits × 16 bits → 32 bits.
DIVXU	B/W	Rd ÷ Rs → Rd Performs unsigned division on data in two general registers: either 16 bits ÷ 8 bits → 8-bit quotient and 8-bit remainder or 32 bits ÷ 16 bits → 16-bit quotient and 16-bit remainder.

Note: * Refers to the operand size.
B: Byte
W: Word
L: Longword

Origin of Interrupt Source	Name	Vector Number	Vector Address Advanced Mode	ICR	Priority
—	Reserved for system use	24	H'000060	—	High
WDT_0	WOVI0 (Interval timer)	25	H'000064	ICRA1	
WDT_1	WOVI1 (Interval timer)	26	H'000068	ICRA0	
—	Address break	27	H'00006C	—	
A/D converter	ADI (A/D conversion end)	28	H'000070	ICRB7	
—	Reserved for system use	29 | 32	H'000074 | H'000080	—	
External pin	WUE15 to WUE8	33	H'000084	ICRD4	
TPU_0	TGI0A (TGR0A input capture/compare match)	34	H'000088	ICRD3	
	TGI0B (TGR0B input capture/compare match)	35	H'00008C		
	TGI0C (TGR0C input capture/compare match)	36	H'000090		
	TGI0D (TGR0D input capture/compare match)	37	H'000094		
	TGI0V (Overflow 0)	38	H'000098		
TPU_1	TGI1A (TGR1A input capture/compare match)	39	H'00009C	ICRD2	
	TGI1B (TGR1B input capture/compare match)	40	H'0000A0		
	TGI1V (Overflow 1)	41	H'0000A4		
	TGI1U (Underflow 1)	42	H'0000A8		
TPU_2	TGI2A (TGR2A input capture/compare match)	43	H'0000AC	ICRD1	
	TGI2B (TGR2B input capture/compare match)	44	H'0000B0		
	TGI2V (Overflow 2)	45	H'0000B4		
	TGI2U (Underflow 2)	46	H'0000B8		
—	Reserved for system use	47	H'0000BC	—	
TCM_0	TICI0 (Input capture) TCMI0 (Compare match) TOVMI0 (Cycle overflow) TUDI0 (Cycle underflow) TOVI0 (Overflow)	48	H'0000C0	ICRB6	
TCM_1	TICI1 (Input capture) TCMI1 (Compare match) TOVMI1 (Cycle overflow) TUDI1 (Cycle underflow) TOVI1 (Overflow)	49	H'0000C4		Low

Origin of Interrupt Source	Name	Vector Number	Vector Address Advanced Mode	ICR	Priority
SCI_2	ERI2 (Reception error) RXI2 (Reception completion) TXI2 (Transmission data empty 2) TEI2 (Transmission end 2)	88 89 90 91	H'000160 H'000164 H'000168 H'00016C	ICRC5	High
IIC_0	IICI0 (1-byte transmission/reception completion)	92	H'000170	ICRC4	
CIR	RENDI (Reception end) OVEI (Overrun error) REPI (Repeat detection) FREI (Framing error) ABI (Abort) HEADFI (Header detection)	93	H'000174	ICRB4	
IIC_1	IICI1 (1-byte transmission/reception completion)	94	H'000178	ICRC3	
IIC_2	IICI2 (1-byte transmission/reception completion)	95	H'00017C		
PS2	KBIA (Reception completion A) KBIB (Reception completion B) KBIC (Reception completion C) KBTIA (Transmission completion A)/ KBCA (1st KCLKA) KBTIB (Transmission completion B)/ KBCB (1st KCLKB) KBTIC (Transmission completion C)/ KBCC (1st KCLKC) KBID (Reception completion D) KBTID (Transmission completion D)/KBCD (1st KCLKD)	96 97 98 99 100 101 102 103	H'000180 H'000184 H'000188 H'00018C H'000190 H'000194 H'000198 H'00019C	ICRB0	
FSI	LFSII (Command reception)/(Write reception)	104	H'0001A0	ICRC1	
—	Reserved for system use	105	H'0001A4	—	
LPC	OBEI (ODR1 to 4 transmission completion) IBFI4 (IDR4 reception completion) ERR1 (Transfer error, etc.) IBFI1 (IDR1 reception completion) IBFI2 (IDR2 reception completion) IBFI3 (IDR3 reception completion)	106 107 108 109 110 111	H'0001A8 H'0001AC H'0001B0 H'0001B4 H'0001B8 H'0001BC	ICRC1	
—	Reserved for system use	112 ⋮ 127	H'0001C0 ⋮ H'0001FC	—	Low

5.6.2 Interrupt Control Mode 1

In interrupt control mode 1, mask control is applied to three levels for interrupt requests other than NMI and address break by comparing the I and UI bits in CCR in the CPU, and the ICR setting.

- An interrupt request with interrupt control level 0 is accepted when the I bit in CCR is cleared to 0. When the I bit is set to 1, the interrupt request is held pending.
- An interrupt request with interrupt control level 1 is accepted when the I bit or UI bit in CCR is cleared to 0. When both the I and UI bits are set to 1, the interrupt request is held pending.

For instance, the state transition when the interrupt enable bit corresponding to each interrupt is set to 1, and ICRA to ICRD are set to H'20, H'00, H'00, and H'00, respectively (IRQ2 and IRQ3 interrupts are set to interrupt control level 1, and other interrupts are set to interrupt control level 0) is shown below. Figure 5.8 shows a state transition diagram.

- All interrupt requests are accepted when I = 0. (Priority order: NMI > IRQ2 > IRQ3 > address break > IRQ0 > IRQ1 …)
- Only NMI, IRQ2, IRQ3, and address break interrupt requests are accepted when I = 1 and UI = 0.
- Only NMI and address break interrupt requests are accepted when I = 1 and UI = 1.

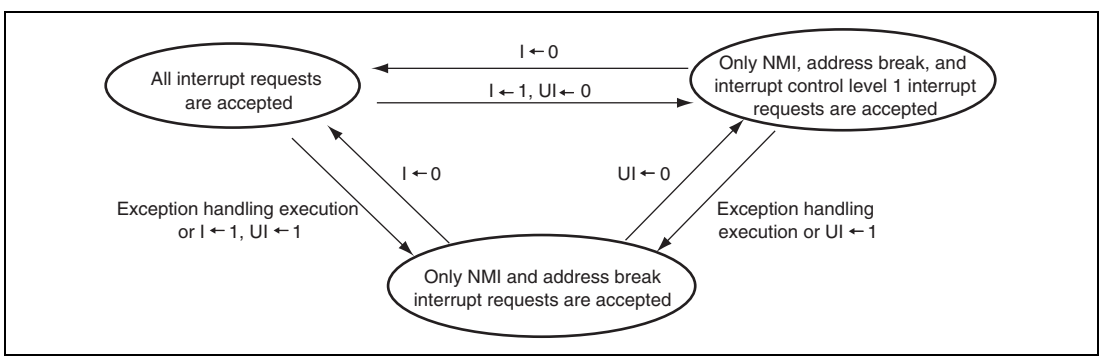


Figure 5.8 State Transition in Interrupt Control Mode 1

8.3.3 PWM Control Register C (PWMCONC)

PWMCONC selects the PWM count mode and operating mode for each channel.

Bit	Bit Name	Initial Value	R/W	Description
7	—	0	R/W	Reserved The initial value should not be changed.
6	CNTMD01	0	R/W	Channels 0 and 1 Counter Select 0: Channels 0 and 1 are in 8-bit counter operation. 1: Channels 0 and 1 are in 16-bit counter operation (Upper: channel 1, lower: channel 0). Note: When the 16-bit counter is selected, specify single pulse mode.
5	PWMSL5	0	R/W	Channel 5 Operating Mode Select 0: Single-pulse mode 1: Pulse division mode (Specify 8-bit counter mode.)
4	PWMSL4	0	R/W	Channel 4 Operating Mode Select 0: Single pulse mode 1: Pulse division mode (Specify 8-bit counter mode.)
3	PWMSL3	0	R/W	Channel 3 Operating Mode Select 0: Single pulse mode 1: Pulse division mode (Specify 8-bit counter mode.)
2	PWMSL2	0	R/W	Channel 2 Operating Mode Select 0: Single pulse mode 1: Pulse division mode (Specify 8-bit counter mode.)
1	PWMSL1	0	R/W	Channel 1 Operating Mode Select 0: Single pulse mode 1: Pulse division mode (Specify 8-bit counter mode.)
0	PWMSL0	0	R/W	Channel 0 Operating Mode Select 0: Single pulse mode 1: Pulse division mode (Specify 8-bit counter mode.)

(1) Example of Buffer Operation Setting Procedure

Figure 10.18 shows an example of the buffer operation setting procedure.

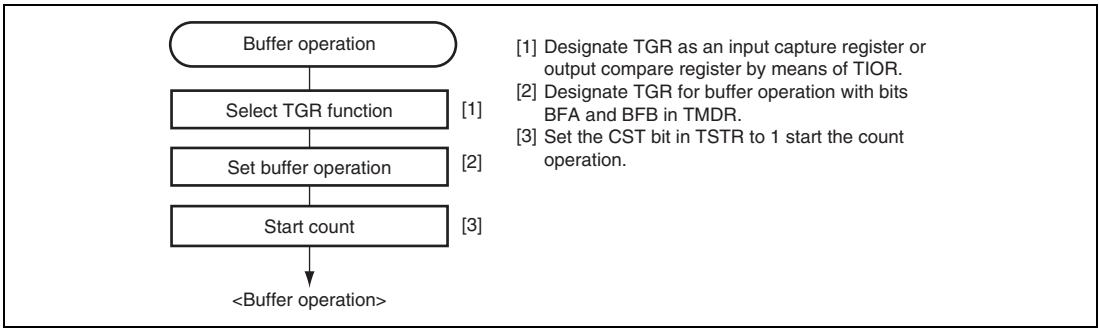


Figure 10.18 Example of Buffer Operation Setting Procedure

12.4 Operation

The TDP operates in timer mode or cycle measurement mode. After a reset, the TDP is in timer mode.

12.4.1 Timer Mode

When the TDPMDS bit in TDPCR1 is cleared to 0, the TDP operates in timer mode.

(1) Counter Operation

The TDP operates as a free-running counter in timer mode. The TDP starts counting up when the CST bit in TDPCR1 is set to 1. When TDPCNT overflows (H'FFFF changes to H'0000), the OVF bit in TDPCSR is set to 1 and an interrupt request is generated if the OVIE bit in TDPIER is 1. Figure 12.2 shows an example of free-running counter operation. In addition, figure 12.3 shows TDPCNT count timing for external clock operation. Note that the external clock requires a pulse width of at least 1.5 cycles. The counter will not operate correctly if the pulses are narrower than this.

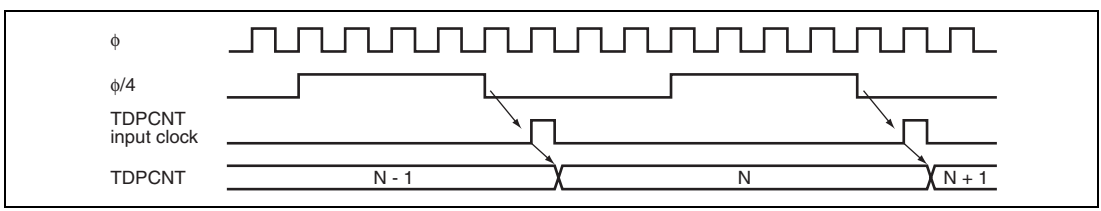


Figure 12.2 Example of Free-Running Counter Operation

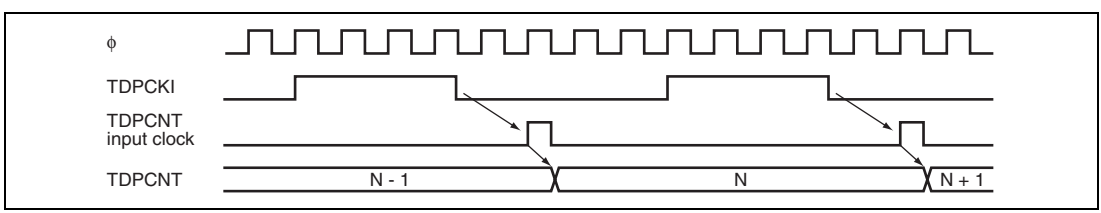


Figure 12.3 Count Timing of External Clock Operation (Falling Edges)

15.7.7 Serial Data Reception (Except in Block Transfer Mode)

Data reception in smart card interface mode is identical to that in normal serial communication interface mode. Figure 15.29 shows the data re-transfer operation during reception.

1. If a parity error is detected in receive data, the PER bit in SSR is set to 1. Here, an ERI interrupt request is generated if the RIE bit in SCR is set to 1. Clear the PER bit to 0 before the next parity bit is sampled.
2. For the frame in which a parity error is detected, the RDRF bit in SSR is not set to 1.
3. If no parity error is detected, the PER bit in SSR is not set to 1. In this case, data is determined to have been received successfully, and the RDRF bit in SSR is set to 1. Here, an RXI interrupt request is generated if the RIE bit in SCR is set.

Figure 15.30 shows a sample flowchart for reception. In reception, setting the RIE bit to 1 allows an RXI interrupt request to be generated when the RDRF flag is set to 1. If an error occurs during reception, i.e., either the ORER or PER flag is set to 1, a transmit/receive error interrupt (ERI) request is generated and the error flag must be cleared. Even if a parity error occurs and PER is set to 1 in reception, receive data is transferred to RDR, thus allowing the data to be read.

Note: For operations in block transfer mode, see section 15.4, Operation in Asynchronous Mode.

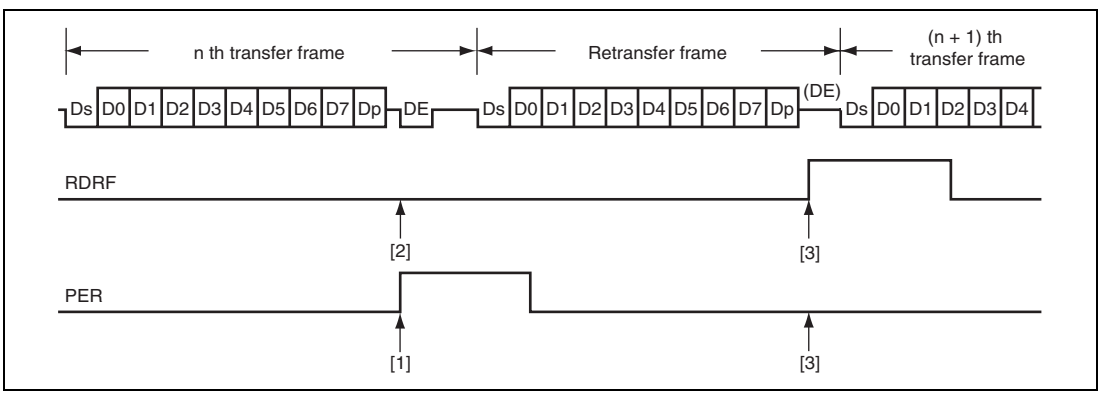


Figure 15.29 Data Re-transfer Operation in SCI Reception Mode

Section 19 Keyboard Buffer Control Unit (PS2)

This LSI has four on-chip keyboard buffer control unit (PS2) channels. The PS2 is provided with functions conforming to the PS/2 interface specifications.

Data transfer using the PS2 employs a data line (KD) and a clock line (KCLK), providing economical use of connectors, board surface area, etc. Figure 19.1 shows a block diagram of the PS2.

19.1 Features

- Conforms to PS/2 interface specifications
- Direct bus drive (via the KCLK and KD pins)
- Interrupt sources: on completion of data reception/transmission, on detection of clock falling edge, and on detection of the first falling edge of a clock
- Error detection: parity error, stop bit monitoring, and receive notify monitoring

24.8.3 User Boot Mode

This LSI has user boot mode that is initiated with different mode pin settings than those in boot mode or user program mode. User boot mode is a user-arbitrary boot mode, unlike boot mode that uses the on-chip SCI.

Only the user MAT can be programmed/erased in user boot mode. Programming/erasing of the user boot MAT is only enabled in boot mode or programmer mode.

(1) User Boot Mode Initiation

For the mode pin settings to start up user boot mode, see table 24.7.

When the reset start is executed in user boot mode, the built-in check routine runs. The user MAT and user boot MAT states are checked by this check routine.

While the check routine is running, NMI and all other interrupts cannot be accepted.

Next, processing starts from the execution start address of the reset vector in the user boot MAT. At this point, H'AA is set to FMATS because the execution target MAT is the user boot MAT.

(2) User MAT Programming in User Boot Mode

For programming the user MAT in user boot mode, additional processing made by setting FMATS is required: switching from user-boot-MAT selection state to user-MAT selection state, and switching back to user-boot-MAT selection state after programming completes.

Figure 24.14 shows the procedure for programming the user MAT in user boot mode.

Table 26.3 LSI Internal States in Each Operating Mode

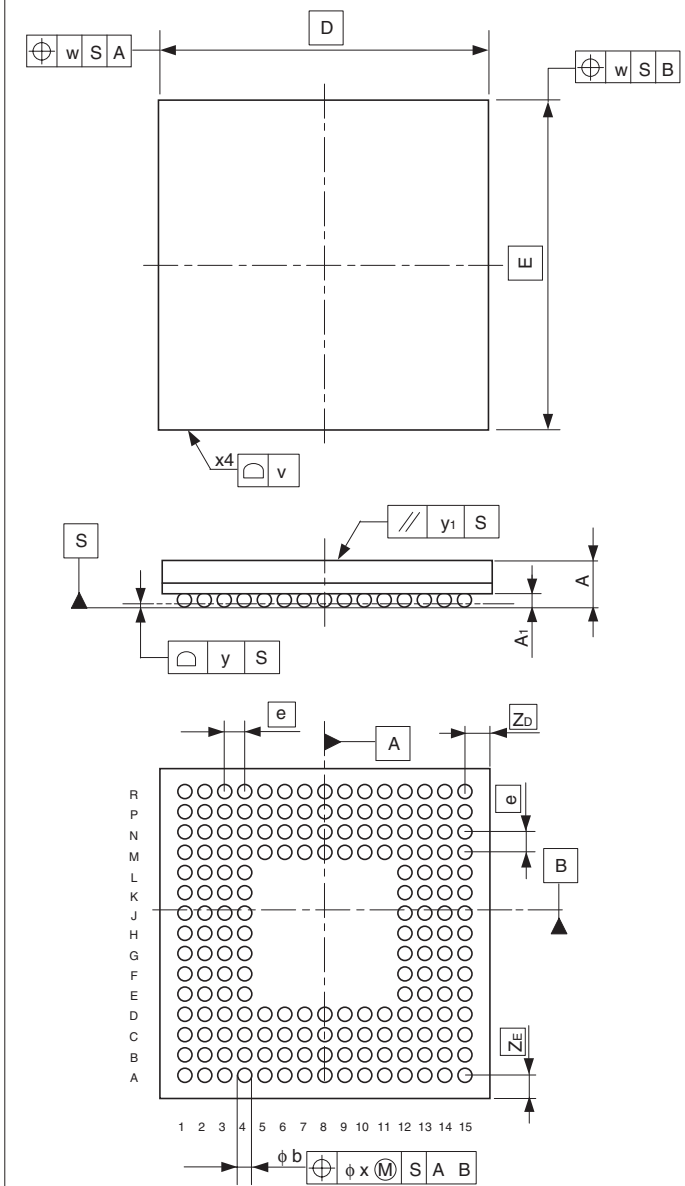
Function		High Speed	Medium Speed	Sleep	Module Stop	Watch	Software Standby
System clock pulse generator		Functioning	Functioning	Functioning	Functioning	Stopped	Stopped
Subclock input		Functioning	Functioning	Functioning	Functioning	Functioning	Stopped
CPU	Instruction execution	Functioning	Medium-speed operation	Stopped	Functioning	Stopped	Stopped
	Registers			Retained		Retained	Retained
External interrupts	NMI	Functioning	Functioning	Functioning	Functioning	Functioning	Functioning
	IRQ0 to IRQ15						
	KIN0 to KIN15						
	WUE8 to WUE15						
On-chip peripheral modules	WDT_1	Functioning	Functioning	Functioning	Functioning	Subclock operation	Stopped (retained)
	CIR						
	WDT_0					Stopped (retained)	
	TMR_0, TMR_1				Functioning/ stopped (retained)		
	TPU TCM_0 to 3 TDP_0 to 2						
	TMR_X, TMR_Y						
	SCIF						
	IIC_0 to 2						
	LPC						
	FSI						
	PS2_0 to 3		Medium-speed operation/functioning				
	PWMU		Functioning		Functioning/ stopped (reset)	Stopped (reset)	Stopped (reset)
	PWM						
	PWMX						
	SCI_1, SCI_2						
	A/D converter						
	RAM	Functioning	Functioning	Functioning	Functioning	Retained	Retained
	I/O	Functioning	Functioning	Functioning	Functioning	Retained	Retained

Note: Stopped (retained) means that the internal register values are retained and the internal state is operation suspended. Stopped (reset) means that the internal register values and the internal state are initialized. In module stop mode, only modules for which a stop setting has been made are stopped (reset or retained).

Register Abbreviation	Reset	High-Speed/Medium speed	Watch	Sleep	Module Stop	Software Standby	Module
IDR1	Initialized	—	—	—	—	—	LPC
ODR1	Initialized	—	—	—	—	—	
STR1	Initialized	—	—	—	—	—	
SIRQCR4	Initialized	—	—	—	—	—	
IDR2	Initialized	—	—	—	—	—	
ODR2	Initialized	—	—	—	—	—	
STR2	Initialized	—	—	—	—	—	
HISEL	Initialized	—	—	—	—	—	
HICR0	Initialized	—	—	—	—	—	
HICR1	Initialized	—	—	—	—	—	
HICR2	—	—	—	—	—	—	
HICR3	—	—	—	—	—	—	
WUEMR	Initialized	—	—	—	—	—	INT
PGODR	Initialized	—	—	—	—	—	PORT
PGPIN	—	—	—	—	—	—	
PGDDR	Initialized	—	—	—	—	—	
PFODR	Initialized	—	—	—	—	—	
PEPIN	—	—	—	—	—	—	
PFPIN	—	—	—	—	—	—	
PFDDR	Initialized	—	—	—	—	—	
PCODR	Initialized	—	—	—	—	—	
PDODR	Initialized	—	—	—	—	—	
PCPIN	—	—	—	—	—	—	
PCDDR	Initialized	—	—	—	—	—	
PDPIN	—	—	—	—	—	—	
PDDDR	Initialized	—	—	—	—	—	
TCR_0	Initialized	—	—	—	—	—	TPU_0
TMDR_0	Initialized	—	—	—	—	—	
TIORH_0	Initialized	—	—	—	—	—	
TIORL_0	Initialized	—	—	—	—	—	
TIER_0	Initialized	—	—	—	—	—	
TSR_0	Initialized	—	—	—	—	—	
TCNT_0	Initialized	—	—	—	—	—	

Module	Register Abbreviation	Number of Bits	Address	Data Bus Width	Access States
PORT	PFODR	8	H'F973 (PORTS = 1)	8	2
PORT	PEPIN	8	H'F974 (Read) (PORTS = 1)	8	2
PORT	PFPIN	8	H'F975 (Read) (PORTS = 1)	8	2
PORT	PFPCR	8	H'F977 (PORTS = 1)	8	2
PORT	PFNOCR	8	H'F979 (PORTS = 1)	8	2
PORT	PGDDR	8	H'F980 (PORTS = 1)	8	2
PORT	PHDDR	8	H'F981 (PORTS = 1)	8	2
PORT	PGODR	8	H'F982 (PORTS = 1)	8	2
PORT	PHODR	8	H'F983 (PORTS = 1)	8	2
PORT	PGPIN	8	H'F984 (Read) (PORTS = 1)	8	2
PORT	PHPIN	8	H'F985 (Read) (PORTS = 1)	8	2
PORT	PHPCR	8	H'F987 (PORTS = 1)	8	2
PORT	PGNOCR	8	H'F988 (PORTS = 1)	8	2
PORT	PHNOCR	8	H'F989 (PORTS = 1)	8	2
PORT	PGNCE	8	H'F98A (PORTS = 1)	8	2
PORT	PGNCMC	8	H'F98C (PORTS = 1)	8	2
PORT	PGNCCS	8	H'F98E (PORTS = 1)	8	2
PORT	PIDDR	8	H'F990	8	2
PORT	PJDDR	8	H'F991	8	2

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFBGA176-13x13-0.80	PLBG0176GA-A	BP-176/BP-176V	0.45g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	13.0	—
E	—	13.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.40
A_1	0.35	0.40	0.45
e	—	0.80	—
b	0.45	0.50	0.55
x	—	—	0.08
y	—	—	0.10
y_1	—	—	0.2
S_D	—	—	—
S_E	—	—	—
Z_D	—	0.90	—
Z_E	—	0.90	—

Figure C.2 Package Dimensions (BP-176V)