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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2600
Core Size	16-Bit
Speed	20MHz
Connectivity	FIFO, I²C, LPC, SCI, SmartCard
Peripherals	POR, PWM, WDT
Number of I/O	112
Program Memory Size	160KB (160K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	144-TQFP
Supplier Device Package	144-TQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2117rvt20hv

User's Manual

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The revision list can be viewed directly by clicking the title page.
The revision list summarizes the locations of revisions and additions.
Details should always be checked by referring to the relevant text.

H8S/2117R Group

Hardware Manual

Renesas 16-Bit Single-Chip Microcomputer
H8S Family / H8S/2100 Series

H8S/2117R R4F2117R

Renesas Electronics
www.renesas.com

Rev.2.00 2009.09

3. Description of Registers

Each register description includes a bit chart, illustrating the arrangement of bits, and a table of bits, describing the meanings of the bit settings. The standard format and notation for bit charts and tables are described below.

[Table of Bits]

Bit	Bit Name	Initial Value	R/W	Description
15	–	0	R	Reserved
14	–	0	R	These bits are always read as 0.
13 to 11	ASID2 to ASID0	All 0	R/W	Address Identifier These bits enable or disable the pin function.
10	–	0	R	Reserved This bit is always read as 0.
9	–	1	R	Reserved This bit is always read as 1.
	–	0		

(1) (2) (3) (4) (5)

Note: The bit names and sentences in the above figure are examples, and have nothing to do with the contents of this manual.

(1) Bit
Indicates the bit number or numbers.
In the case of a 32-bit register, the bits are arranged in order from 31 to 0. In the case of a 16-bit register, the bits are arranged in order from 15 to 0.

(2) Bit name
Indicates the name of the bit or bit field.
When the number of bits has to be clearly indicated in the field, appropriate notation is included (e.g., ASID[3:0]).
A reserved bit is indicated by "–".
Certain kinds of bits, such as those of timer counters, are not assigned bit names. In such cases, the entry under Bit Name is blank.

(3) Initial value
Indicates the value of each bit immediately after a power-on reset, i.e., the initial value.
0: The initial value is 0
1: The initial value is 1
–: The initial value is undefined

(4) R/W
For each bit and bit field, this entry indicates whether the bit or field is readable or writable, or both writing to and reading from the bit or field are impossible.
The notation is as follows:

R/W: The bit or field is readable and writable.
R/(W): The bit or field is readable and writable.
However, writing is only performed to flag clearing.
R: The bit or field is readable.
"R" is indicated for all reserved bits. When writing to the register, write the value under Initial Value in the bit chart to reserved bits or fields.
W: The bit or field is writable.

(5) Description
Describes the function of the bit or field and specifies the values for writing.

Item	Page	Revision (See Manual for Details)
27.1 Register Addresses (Address Order)	863	Table amended

Register Name	Abbreviation	Number of bits	Address	Module	Data Width	Access States
A/D control/status register	ADCSR	8	H'FC10	A/D converter	8	2
A/D control register	ADCR	8	H'FC11	A/D converter	8	2

28.2 DC Characteristics Table 28.2 DC Characteristics (1)	958	Figure amended						

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input high voltage	$\overline{RES}$, NMI, MD2, MD1, and $\overline{ETRST}$	(2)	V_{IH}	$V_{CC} \times 0.9$	—	$V_{CC} + 0.3$	V	
	EXTAL			$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$		
	Port 7			$AV_{CC} \times 0.7$	—	$AV_{CC} + 0.3$		
	Ports A, G, PE4, PE2 to PE0, P97, and P52			$V_{CC} \times 0.7$	—	5.5		

Table 28.2 DC Characteristics (4) Using FSI Function	961	Figure amended						

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high voltage	PB7 to PB4	V_{OH}	$V_{CC} - 0.5$	—	—	V	$I_{OH} = -200\ \mu A$
			$V_{CC} - 1.0$	—	—		$I_{OH} = -1mA$
Output low voltage		V_{OL}	—	—	0.4		$I_{OL} = 1.6\ mA$

28.3.2 Control Signal Timing Figure 28.8 Interrupt Input Timing	967	Figure amended	$\overline{KINi}$ (i = 0 to 15) $\overline{WUEi}$ (i = 8 to 15)

3.2.2 System Control Register (SYSCR)

SYSCR monitors a reset source, selects the interrupt control mode and the detection edge for NMI, enables or disables access to the on-chip peripheral module registers, and enables or disables the on-chip RAM address space.

Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	All 0	R	Reserved The initial value should not be changed.
5	INTM1	0	R	Interrupt Control Select Mode 1 and 0
4	INTM0	0	R/W	These bits select the interrupt control mode of the interrupt controller. For details on the interrupt control modes, see section 5.6, Interrupt Control Modes and Interrupt Operation. 00: Interrupt control mode 0 01: Interrupt control mode 1 10: Setting prohibited 11: Setting prohibited
3	XRST	1	R	External Reset Indicates the reset source. A reset is caused by an external reset input, or when the watchdog timer overflows. 0: A reset is caused when the watchdog timer overflows 1: A reset is caused by an external reset
2	NMIEG	0	R/W	NMI Edge Select Selects the valid edge of the NMI interrupt input. 0: An interrupt is requested at the falling edge of NMI input 1: An interrupt is requested at the rising edge of NMI input

Section 5 Interrupt Controller

5.1 Features

- Two interrupt control modes

  Two interrupt control modes can be set by means of the INTM1 and INTM0 bits in the system control register (SYSCR).
- Priorities settable with ICR

  An interrupt control register (ICR) is provided for setting in each module interrupt priority levels for all interrupt requests excluding NMI and address breaks.
- Three-level interrupt mask control

  By means of the interrupt control mode, I and UI bits in CCR and ICR, 3-level interrupt mask control is performed.
- Forty-one external interrupt pins

  NMI is the highest-priority interrupt, and is accepted at all times. Rising edge or falling edge detection can be selected for NMI. Falling-edge, rising-edge, or both-edge detection, or level sensing, can be independently selected for $\overline{\text{IRQ15}}$ to $\overline{\text{IRQ0}}$. When the EIVS bit in the system control register 3 (SYSCR3) is cleared to 0, the IRQ6 interrupt is generated by $\overline{\text{IRQ6}}$ or $\overline{\text{KIN7}}$ to $\overline{\text{KIN0}}$. The IRQ7 interrupt is generated by $\overline{\text{IRQ7}}$ or $\overline{\text{KIN15}}$ to $\overline{\text{KIN8}}$. When the EIVS bit in the system control register 3 (SYSCR3) is set to 1, interrupts are requested on the falling edge of $\overline{\text{KIN15}}$ to $\overline{\text{KIN0}}$. For $\overline{\text{WUE15}}$ to $\overline{\text{WUE8}}$, either rising-edge or falling-edge detection can be selected individually for each pin regardless of the EIVS bit setting.
- Two interrupt vector addresses are selectable

  H8S/2140B Group compatible interrupt vector addresses or extended interrupt vector addresses are selected depending on the EIVS bit in system control register 3 (SYSCR3). In extended mode, independent vector addresses are assigned for the interrupt vector addresses of KIN7 to KIN0 or KIN15 to KIN8 interrupts.
- General ports for $\overline{\text{IRQ15}}$ to $\overline{\text{IRQ6}}$ input are selectable

5.3 Register Descriptions

The interrupt controller has the following registers. For details on the system control register (SYSCR), see section 3.2.2, System Control Register (SYSCR). For details on system control register 3 (SYSCR3), see section 3.2.4, System Control Register 3 (SYSCR3).

Table 5.2 Register Configuration

Register Name	Abbreviation	R/W	Initial Value	Address	Data Bus Width
Interrupt control registers A	ICRA	R/W	H'00	H'FEE8	8
Interrupt control registers B	ICRB	R/W	H'00	H'FEE9	8
Interrupt control registers C	ICRC	R/W	H'00	H'FEEA	8
Interrupt control registers D	ICRD	R/W	H'00	H'FE87	8
Address break control register	ABRKCR	R/W	—	H'FEF4	8
Break address registers A	BARA	R/W	H'00	H'FEF5	8
Break address registers B	BARB	R/W	H'00	H'FEF6	8
Break address registers C	BARC	R/W	H'00	H'FEF7	8
IRQ sense control register 16H	ISCR16H	R/W	H'00	H'FEFA	8
IRQ sense control register 16L	ISCR16L	R/W	H'00	H'FEFB	8
IRQ sense control register H	ISCRH	R/W	H'00	H'FEEC	8
IRQ sense control register L	ISCRL	R/W	H'00	H'FEED	8
IRQ enable register 16	IER16	R/W	H'00	H'FEF8	8
IRQ enable register	IER	R/W	H'00	H'FFC2	8
IRQ status register 16	ISR16	R/W	H'00	H'FEF9	8
IRQ status register	ISR	R/W	H'00	H'FEEB	8
Keyboard matrix interrupt mask register A	KMIMRA	R/W	H'FF	H'FFF3 H'FE83*[1]	8
Keyboard matrix interrupt mask register	KMIMR	R/W	H'BF H'FF*[2]	H'FFF1 H'FE81*[1]	8
Wake-up event interrupt mask registers	WUEMR	R/W	H'00	H'FE45	8
IRQ sense port select register 16	ISSR16	R/W	H'00	H'FEFC	8
IRQ sense port select register	ISSR	R/W	H'00	H'FEFD	8

Port	Description	Bit	Function			Input Pull-up MOS Function	LED Drive Capability (5 mA Sink Current)	On-Chip Noise Canceler
			I/O	Input	Output			
Port J	General I/O port	7	PJ7*[2]	—	—	O	—	—
		6	PJ6*[2]	—	—			
		5	PJ5*[2]	—	—			
		4	PJ4*[2]	—	—			
		3	PJ3*[2]	—	—			
		2	PJ2*[2]	—	—			
		1	PJ1*[2]	—	—			
		0	PJ0*[2]	—	—			

Notes: 1. Not supported by the system development tool (emulator).
2. Not supported by TFP-144V and TLP-145V.

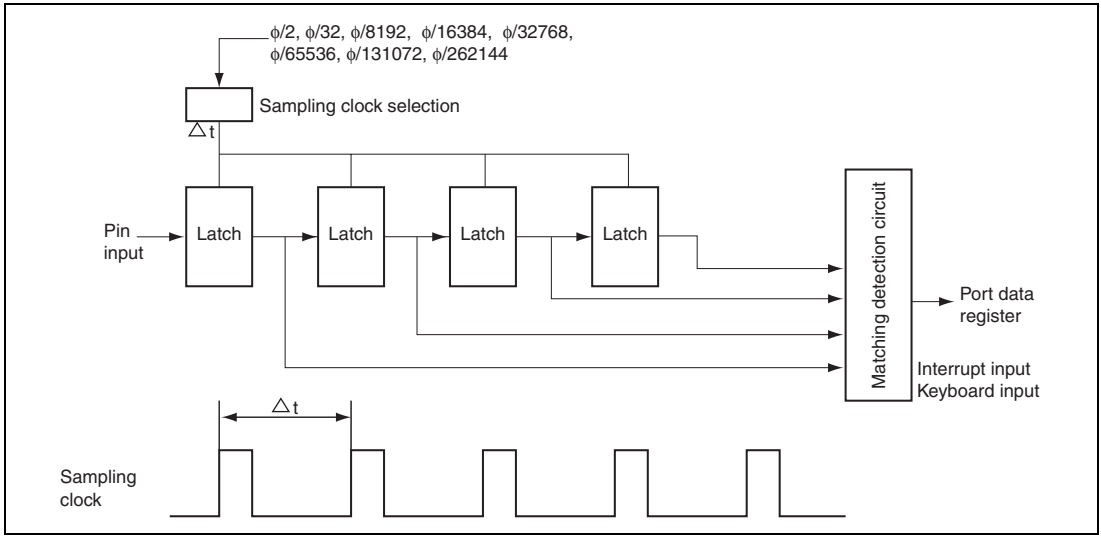

Figure 7.1 Noise Cancel Circuit

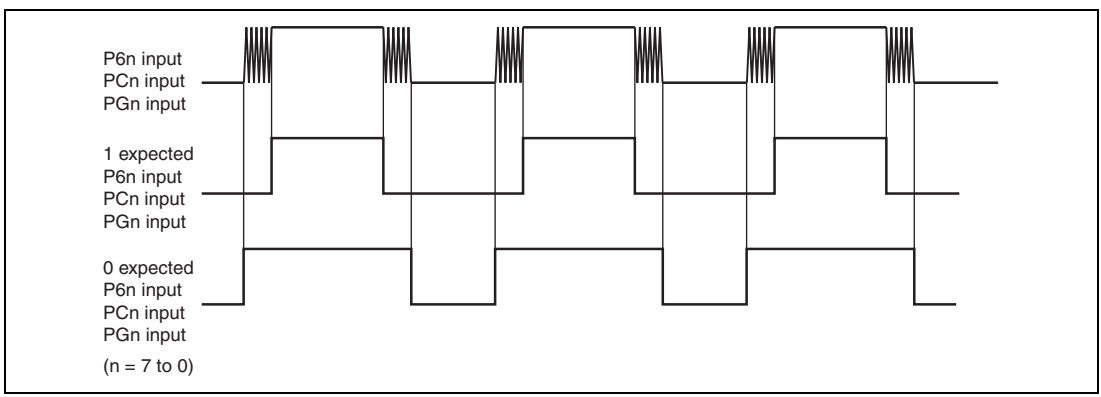

Figure 7.2 Schematic View of Noise Cancel Operation

8.3.1 PWM Control Register A (PWMCONA)

PWMCONA selects the PWM clock source.

Bit	Bit Name	Initial Value	R/W	Description
7, 6	CLK1, CLK0	All 0	R/W	Clock Select 1, 0 These bits select the PWM count clock source. CLK1 CLK0 0 0: Internal clock ϕ is selected 0 1: Internal clock ϕ/2 is selected 1 0: Internal clock ϕ/4 is selected 1 1: Internal clock ϕ/8 is selected
5 to 0	–	All 0	R	Reserved These bits are always read as 0 and cannot be modified.

8.3.2 PWM Control Register B (PWMCONB)

PWMCONB controls enabling and disabling of the PWM output and counter operation of each channel.

Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	All 0	R/W	Reserved The initial value should not be changed.
5	PWM5E	0	R/W	PWMU5 Output Enable 0: PWMU5 output and counter operation are disabled. 1: PWMU5 output and counter operation are enabled.

9.5 Operation

A PWM waveform like the one shown in figure 9.3 is output from the PWMX pin. DA13 to DA0 in DADR corresponds to the total width (T_L) of the low (0) pulses output in one conversion cycle (256 pulses when CFS = 0, 64 pulses when CFS = 1). When OS = 0, this waveform is directly output. When OS = 1, the output waveform is inverted, and DA13 to DA0 in DADR value corresponds to the total width (T_H) of the high (1) output pulses. Figures 9.4 and 9.5 show the types of waveform output available.

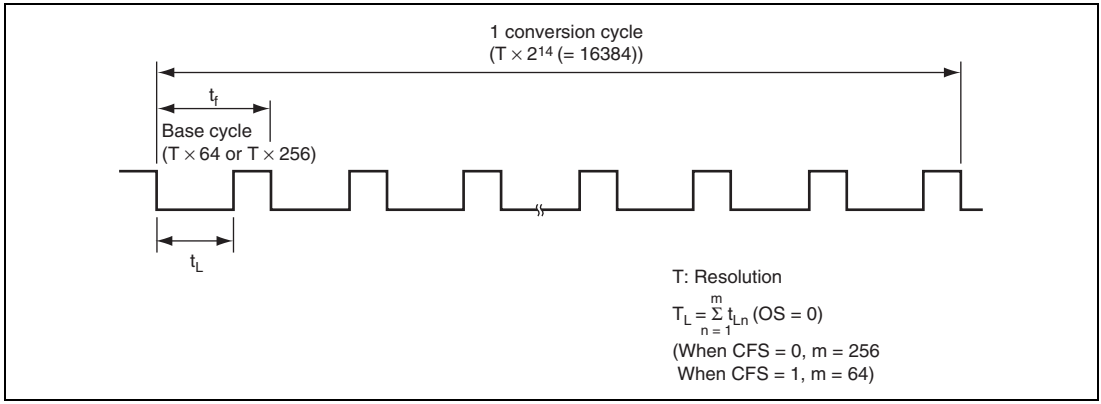

Figure 9.3 PWMX (D/A) Operation

Table 9.5 summarizes the relationships between the CKS and CFS bit settings and the resolution, base cycle, and conversion cycle. The PWM output remains fixed unless DA13 to DA0 in DADR contain at least a certain minimum value. The relationship between the OS bit and the output waveform is shown in figures 9.4 and 9.5.

Channel	Register Name	Abbreviation	R/W	Initial Value	Address	Data Bus Width
Channel 1	TCM timer counter_1	TCMCNT_1	R/W	H'0000	H'FBD0	16
	TCM cycle upper limit register_1	TCMMLCM_1	R/W	H'FFFF	H'FBD2	16
	TCM cycle lower limit register_1	TCMMINCM_1	R/W	H'0000	H'FBDC	16
	TCM input capture register_1	TCMICR_1	R	H'0000	H'FBD4	16
	TCM input capture buffer register_1	TCMICRF_1	R	H'0000	H'FBD6	16
	TCM status register_1	TCMCSR_1	R/W	H'00	H'FBD8	8
	TCM control register_1	TCMCR_1	R/W	H'00	H'FBD9	8
	TCM interrupt enable register_1	TCMIER_1	R/W	H'00	H'FBDA	8
Channel 2	TCM timer counter_2	TCMCNT_2	R/W	H'0000	H'FBE0	16
	TCM cycle upper limit register_2	TCMMLCM_2	R/W	H'FFFF	H'FBE2	16
	TCM cycle lower limit register_2	TCMMINCM_2	R/W	H'0000	H'FBEC	16
	TCM input capture register_2	TCMICR_2	R	H'0000	H'FBE4	16
	TCM input capture buffer register_2	TCMICRF_2	R	H'0000	H'FBE6	16
	TCM status register_2	TCMCSR_2	R/W	H'00	H'FBE8	8
	TCM control register_2	TCMCR_2	R/W	H'00	H'FBE9	8
	TCM interrupt enable register_2	TCMIER_2	R/W	H'00	H'FBEA	8
Channel 3	TCM timer counter_3	TCMCNT_3	R/W	H'0000	H'FBF0	16
	TCM cycle upper limit register_3	TCMMLCM_3	R/W	H'FFFF	H'FBF2	16
	TCM cycle lower limit register_3	TCMMINCM_3	R/W	H'0000	H'FBFC	16
	TCM input capture register_3	TCMICR_3	R	H'0000	H'FBF4	16
	TCM input capture buffer register_3	TCMICRF_3	R	H'0000	H'FBF6	16
	TCM status register_3	TCMCSR_3	R/W	H'00	H'FBF8	8
	TCM control register_3	TCMCR_3	R/W	H'00	H'FBF9	8
	TCM interrupt enable register_3	TCMIER_3	R/W	H'00	H'FBFA	8

20.3.19 Host Interface Select Register (HISEL)

HISEL selects the function of bits 7 to 4 in STR3 and selects the output of the host interrupt request signal of each frame.

Bit	Bit Name	Initial Value	R/W		Description
			Slave	Host	
7	SELSTR3	0	R/W	—	Status Register 3 Selection Selects the function of bits 7 to 4 in STR3 in combination with the TWRE bit in LADR3L. For details of STR3, see section 20.3.12, Status Registers 1 to 4 (STR1 to STR4). 0: Bits 7 to 4 in STR3 indicate processing status of the LPC interface. 1: [When TWRE = 1] Bits 7 to 4 in STR3 indicate processing status of the LPC interface. [When TWRE = 0] Bits 7 to 4 in STR3 are readable/writable bits which user can use as necessary
6	SELIRQ11	0	R/W	—	Host IRQ Interrupt Select These bits select the state of the output on the SERIRQ pins. 0: [When host interrupt request is cleared] SERIRQ pin output is in the Hi-Z state [When host interrupt request is set] SERIRQ pin output is low 1: [When host interrupt request is cleared] SERIRQ pin output is low [When host interrupt request is set] SERIRQ pin output is in the Hi-Z state.
5	SELIRQ10	0	R/W	—	
4	SELIRQ9	0	R/W	—	
3	SELIRQ6	0	R/W	—	
2	SELSMI	0	R/W	—	
1	SELIRQ12	1	R/W	—	
0	SELIRQ1	1	R/W	—	

21.3.3 FSI Byte Count Register (FSIBNR)

The FSIBNR sets the number of bytes to be transmitted or received by the FSI. This register should not be set in the processing other than FSICMDI and FSIWI interrupt processing.

Bit	Bit Name	Initial Value	R/W EC	R/W Host	Description
7 to 4	TBN3	0	R/W	—	Transmit Byte Count 3-0
	TBN2	0			These bits specify the number of data bytes to be transmitted. The TBN value is decremented each time one byte of FSI data transmission is completed. When the FSI transmission ends, TBN is cleared to B'0000.
	TBN1	0			
	TBN0	0			
					0000: Transmits no data
					0001: Transmits one byte of data
					0010: Transmits two bytes of data
					0011: Transmits three bytes of data
					0100: Transmits four bytes of data
					0101: Transmits five bytes of data
					0110: Transmits six bytes of data
					0111: Transmits seven bytes of data
					1000: Transmits eight bytes of data
					1001 to 1111: Setting prohibited
					If transmission of nine bytes or more is specified, data in FSITDR7 is transmitted.
3	—	0	R/W	—	Reserved
					The initial value should not be modified.

(b) Programming

FPFR indicates the return value of the programming result.

Bit	Bit Name	Initial Value	R/W	Description
7	—	—	—	Unused Returns 0.
6	MD	—	R/W	Programming Mode Related Setting Error Detect Detects the error protection state and returns the result. When the error protection state is entered, this bit is set to 1. Whether the error protection state is entered or not can be confirmed with the FLER bit in FCCS. For conditions to enter the error protection state see section 24.9.3, Error Protection. 0: Normal operation (FLER = 0) 1: Error protection state, and programming cannot be performed (FLER = 1)
5	EE	—	R/W	Programming Execution Error Detect Writes 1 to this bit when the specified data could not be written because the user MAT was not erased. If this bit is set to 1, there is a high possibility that the user MAT has been written to partially. In this case, after removing the error factor, erase the user MAT. Also an attempt to write the user MAT when the FMATS value is H'AA and the user boot MAT is selected leads to a programming execution error. In that case, both the user MAT and user boot MAT are not rewritten. Writing to the user boot MAT must be performed in boot mode or programmer mode. 0: Programming has ended normally 1: Programming has ended abnormally (programming result is not guaranteed)
4	FK	—	R/W	Flash Key Register Error Detect Checks the FKEY value (H'5A) before programming starts, and returns the result. 0: FKEY setting is normal (H'5A) 1: FKEY setting is abnormal (value other than H'5A)
3	—	—	—	Unused Returns 0.

Lower Address	Register Abbreviation	Register Selection Condition	Module
H'F944	P9PIN (Read)	PORTS = 1	PORT
H'F946	P9PCR		
H'F950	PADDR		
H'F951	PBDDR		
H'F952	PAODR		
H'F953	PBODR		
H'F954	PAPIN (Read)		
H'F955	PBPIN (Read)		
H'F957	PBPCR		
H'F960	PCDDR		
H'F961	PDDDR		
H'F962	PCODR		
H'F963	PDODR		
H'F964	PCPIN (Read)		
H'F965	PDPIN (Read)		
H'F966	PCPCR		
H'F967	PDPCR		
H'F968	PCNOCR		
H'F969	PDNOCR		
H'F96A	PCNCE		
H'F96C	PCNCMC		
H'F96E	PCNCCS		
H'F971	PFDDR		
H'F973	PFODR		
H'F974	PEPIN (Read)		
H'F975	PFPIN (Read)		
H'F977	PFPCR		
H'F979	PFNOCR		
H'F980	PGDDR		
H'F981	PHDDR		
H'F982	PGODR		

Module	Register Abbreviation	Number of Bits	Address	Data Bus Width	Access States
PORT	P2DR	8	H'FFB3 (PORTS = 0)	8	2
PORT	P3DDR	8	H'FFB4 (PORTS = 0)	8	2
PORT	P4DDR	8	H'FFB5 (PORTS = 0)	8	2
PORT	P3DR	8	H'FFB6 (PORTS = 0)	8	2
PORT	P4DR	8	H'FFB7 (PORTS = 0)	8	2
PORT	P5DDR	8	H'FFB8 (PORTS = 0)	8	2
PORT	P6DDR	8	H'FFB9 (PORTS = 0)	8	2
PORT	P5DR	8	H'FFBA (PORTS = 0)	8	2
PORT	P6DR	8	H'FFBB (PORTS = 0)	8	2
PORT	PBODR	8	H'FFBC (PORTS = 0)	8	2
PORT	P8DDR	8	H'FFBD (Write) (PORTS = 0)	8	2
PORT	PBPIN	8	H'FFBD (Read) (PORTS = 0)	8	2
PORT	P7PIN	8	H'FFBE (Read) (PORTS = 0)	8	2
PORT	PBDDR	8	H'FFBE (Write) (PORTS = 0)	8	2
PORT	P8DR	8	H'FFBF (PORTS = 0)	8	2
PORT	P9DDR	8	H'FFC0 (PORTS = 0)	8	2
PORT	P9DR	8	H'FFC1 (PORTS = 0)	8	2
PORT	KMPCR	8	H'FFF2 (RELOCATE = 0) (PORTS = 0)	8	2

Module	Register Abbreviation	Number of Bits	Address	Data Bus Width	Access States
CIR	DT1MIN	8	H'FA4E	8	2
CIR	DT1MAX	8	H'FA4F	8	2
CIR	RMIN	8	H'FA50	8	2
CIR	RMAX	8	H'FA51	8	2
PWMU_A	PWMREG0	8	H'FD00	8	2
PWMU_A	PWMPRE0	8	H'FD01	8	2
PWMU_A	PWMREG1	8	H'FD02	8	2
PWMU_A	PWMPRE1	8	H'FD03	8	2
PWMU_A	PWMREG2	8	H'FD04	8	2
PWMU_A	PWMPRE2	8	H'FD05	8	2
PWMU_A	PWMREG3	8	H'FD06	8	2
PWMU_A	PWMPRE3	8	H'FD07	8	2
PWMU_A	PWMREG4	8	H'FD08	8	2
PWMU_A	PWMPRE4	8	H'FD09	8	2
PWMU_A	PWMREG5	8	H'FD0A	8	2
PWMU_A	PWMPRE5	8	H'FD0B	8	2
PWMU_A	PWMCONA	8	H'FD0C	8	2
PWMU_A	PWMCONB	8	H'FD0D	8	2
PWMU_A	PWMCONC	8	H'FD0E	8	2
PWMU_A	PWMCOND	8	H'FD0F	8	2
PWMU_B	PWMREG0	8	H'FD10	8	2
PWMU_B	PWMPRE0	8	H'FD11	8	2
PWMU_B	PWMREG1	8	H'FD12	8	2
PWMU_B	PWMPRE1	8	H'FD13	8	2
PWMU_B	PWMREG2	8	H'FD14	8	2
PWMU_B	PWMPRE2	8	H'FD15	8	2
PWMU_B	PWMREG3	8	H'FD16	8	2
PWMU_B	PWMPRE3	8	H'FD17	8	2
PWMU_B	PWMREG4	8	H'FD18	8	2
PWMU_B	PWMPRE4	8	H'FD19	8	2
PWMU_B	PWMREG5	8	H'FD1A	8	2
PWMU_B	PWMPRE5	8	H'FD1B	8	2

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