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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2600
Core Size	16-Bit
Speed	20MHz
Connectivity	FIFO, I²C, LPC, SCI, SmartCard
Peripherals	POR, PWM, WDT
Number of I/O	112
Program Memory Size	160KB (160K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	144-TQFP
Supplier Device Package	144-TQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2117rvt20ihv

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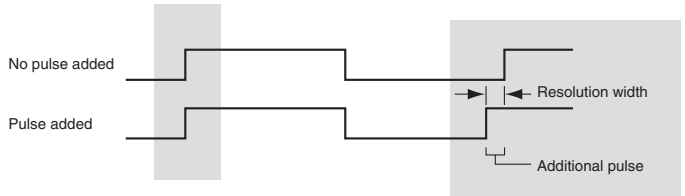
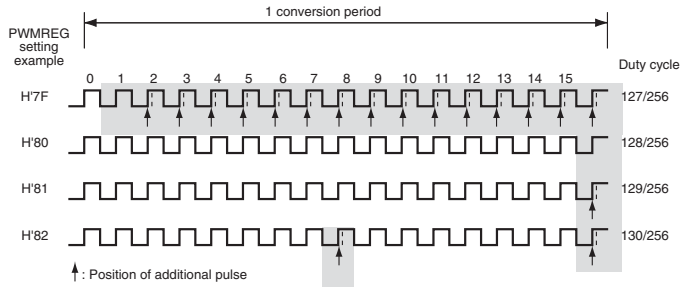
Item	Page	Revision (See Manual for Details)
8.4.2 Pulse Division Mode Figure 8.8 Example of Additional Pulse Timing (Upper 4 Bits in PWMREG = B'1000)	215	Figure amended 
Figure 8.9 Example of WMU Setting	216	Figure amended 
10.3.3 Timer I/O Control Register (TIOR) Table 10.13 TIORL_0 (channel 0)	253	Table amended **Bit 3 IOC3** **Bit 2 IOC2** **Bit 1 IOC1** **Bit 0 IOC0**
11.3.6 TCM Status Register (TCMCSR)	312	Table amended **Bit** **Bit Name** **Initial Value** **R/W** **Description** 0 0 R/W Reserved The initial value should not be changed.
14.3.2 Timer Control/Status Register (TCSR)	394	Table amended **Bit** **Bit Name** **Initial Value** **R/W** **Description** 4 0 R/W Reserved The initial value should not be changed.

8.3 Register Descriptions

The PWMU has the following registers.

Table 8.2 Register Configuration

Channel	Register Name	Abbreviation	R/W	Initial Value	Address	Data Bus Width
Channel A	PWM control register A_A (for clock control)	PWMCONA_A	R/W	H'00	H'FD0C	8
	PWM control register B_A (for output control)	PWMCONB_A	R/W	H'00	H'FD0D	8
	PWM control register C_A (for mode control)	PWMCONC_A	R/W	H'00	H'FD0E	8
	PWM control register D_A (for phase control)	PWMCOND_A	R/W	H'00	H'FD0F	8
	PWM prescaler register 0_A	PWMPRE0_A	R/W	H'00	H'FD01	8
	PWM prescaler register 1_A	PWMPRE1_A	R/W	H'00	H'FD03	8
	PWM prescaler register 2_A	PWMPRE2_A	R/W	H'00	H'FD05	8
	PWM prescaler register 3_A	PWMPRE3_A	R/W	H'00	H'FD07	8
	PWM prescaler register 4_A	PWMPRE4_A	R/W	H'00	H'FD09	8
	PWM prescaler register 5_A	PWMPRE5_A	R/W	H'00	H'FD0B	8
	PWM duty setting register 0_A	PWMREG0_A	R/W	H'00	H'FD00	8
	PWM duty setting register 1_A	PWMREG1_A	R/W	H'00	H'FD02	8
	PWM duty setting register 2_A	PWMREG2_A	R/W	H'00	H'FD04	8
	PWM duty setting register 3_A	PWMREG3_A	R/W	H'00	H'FD06	8
	PWM duty setting register 4_A	PWMREG4_A	R/W	H'00	H'FD08	8
	PWM duty setting register 5_A	PWMREG5_A	R/W	H'00	H'FD0A	8

11.6.5 Conflict between Edge Detection in Cycle Measurement Mode and Clearing of TCMMDS Bit in TCMCR

If the CST bit in TCMCR is set to 1 in cycle measurement mode, and the TCMMDS bit in TCMCR is cleared, but the selected edge from TCMCYI is detected at the same time, detection of the selected edge will cause the timer to continue to operate in cycle measurement mode. The timer will not make the transition to timer mode until the next detection of the selected edge. Thus, ensure that the CST bit is cleared to 0 in cycle measurement mode.

Figure 11.17 shows the timing of this conflict.

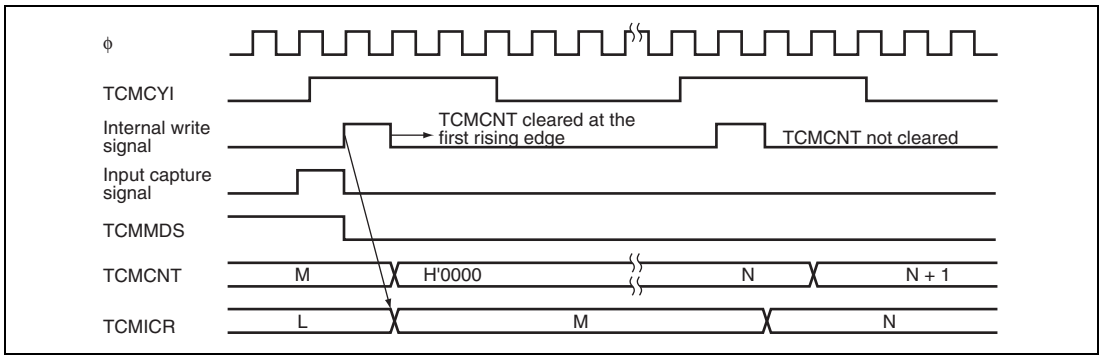


Figure 11.17 Conflict between Edge Detection and Clearing of TCMMDS (to Switch from Cycle Measurement Mode to Timer Mode)

11.6.6 Settings of TCMCKI and TCMMCI

TCMCKI and TCMMCI are multiplexed on the same pin of this LSI. Therefore, the selected external clock and the TCMMCI signal cannot be used at the same time. Do not make the settings CKS2 to CKS0 = B'111 and CMMS = B'1.

11.6.7 Setting for Module Stop Mode

The module-stop control register can be used to select either continuation or stoppage of TCM operation in module-stopped mode. The default setting is for TCM operation to stop. TCM registers become accessible on release from module stop mode. For details, see section 26, Power-Down Modes.

15.3 Register Descriptions

The SCI has the following registers for each channel. Some bits in the serial mode register (SMR), serial status register (SSR), and serial control register (SCR) have different functions in different modes — normal serial communication interface mode and smart card interface mode; therefore, the bits are described separately for each mode in the corresponding register sections.

Table 15.2 Register Configuration

Channel	Register Name	Abbreviation	R/W	Initial Value	Address	Data Bus Width
Channel 1	Serial mode register_1	SMR_1	R/W	H'00	H'FF88	8
	Bit rate register_1	BRR_1	R/W	H'FF	H'FF89	8
	Serial control register_1	SCR_1	R/W	H'00	H'FF8A	8
	Transmit data register_1	TDR_1	R/W	H'FF	H'FF8B	8
	Serial status register_1	SSR_1	R/W	H'84	H'FF8C	8
	Receive data register_1	RDR_1	R	H'00	H'FF8D	8
	Smart card mode register_1	SCMR_1	R/W	H'F2	H'FF8E	8
Channel 2	Serial mode register_2	SMR_2	R/W	H'00	H'FFA0	8
	Bit rate register_2	BRR_2	R/W	H'FF	H'FFA1	8
	Serial control register_2	SCR_2	R/W	H'00	H'FFA2	8
	Transmit data register_2	TDR_2	R/W	H'FF	H'FFA3	8
	Serial status register_2	SSR_2	R/W	H'84	H'FFA4	8
	Receive data register_2	RDR_2	R	H'00	H'FFA5	8
	Smart card mode register_2	SCMR_2	R/W	H'F2	H'FFA6	8

16.4.1 Determination of Signal Type by Low/High-Level Period

The signal type is determined by low/high-level period that is specified in the HHMIN, HHMAX, HLMIN, HLMAX, DT1MIN, DT1MAX, DT0MIN, DT0MAX, RMIN, and RMAX registers. Calculating formula for specified time, setting examples of each maximum/minimum value register during the specified time, and use for each register are described as follows. The symbols in table 16.4 correspond to the ones used in the figure 16.3 to figure 16.5.

$S.E = M (N + 1)/T$

S: Specified time of the NEC format

E: Error from the NEC format

T: Frequency of the reference clock (Hz) set by the CLK1 and CLK0 bits in CCR1 (ϕ, $\phi/2$, $\phi/4$, or ϕsub)

N: Setting value in BRR ($0 \leq N \leq 255$)

M: Value in the maximum/minimum value setting register

Section 17 Serial Communication Interface with FIFO (SCIF)

This LSI has single-channel serial communication interface with FIFO buffers (SCIF) that supports asynchronous serial communication.

The SCIF enables asynchronous serial communication with standard asynchronous communication LSIs such as a Universal Asynchronous Receiver/Transmitter (UART). The SCIF also has independent 16-stage FIFO buffers for transmission and reception to provide efficient high-speed continuous communication.

In addition, the SCIF can be connected to the LPC interface for direct control from the LPC host.

17.1 Features

- Full-duplex communication:
  The transmitter and receiver are independent, enabling transmission and reception to be executed simultaneously. Both the transmitter and receiver use 16-stage FIFO buffering, enabling continuous transmission and continuous reception of serial data.
- On-chip baud rate generator allows any bit rate to be selected
- Modem control function
- Data length: Selectable from 5, 6, 7, and 8 bits
- Parity: Selectable from even parity, odd parity, and no parity
- Stop bit length: Selectable from 1, 1.5, and 2 bits
- Receive error detection: Parity, overrun, and framing errors
- Break detection

17.3.7 Interrupt Identification Register (FIIR)

FIIR consists of bits that identify interrupt sources. For details, see table 17.4.

Bit	Bit Name	Initial Value	R/W	Description
7	FIFOE1	0	R	FIFO Enable 1, 0
6	FIFOE0	0	R	These bits indicate the transmit/receive FIFO setting. 00: Transmit/receive FIFOs disabled 11: Transmit/receive FIFOs enabled
5, 4	—	All 0	R	Reserved These bits are always read as 0 and cannot be modified.
3	INTID2	0	R	Interrupt ID2, ID1, ID0
2	INTID1	0	R	These bits Indicate the interrupt of the highest priority among the pending interrupts.
1	INTID0	0	R	000: Modem status 001: FTHR empty 010: Receive data ready 011: Receive line status 110: Character timeout (when the FIFO is enabled)
0	INTPEND	1	R	Interrupt Pending Indicates whether one or more interrupts are pending. 0: Interrupt pending 1: No interrupt pending

19.3.1 Keyboard Control Register 1 (KBCR1)

KBCR1 controls data transmission and interrupt, selects parity, and detects transmit error.

Bit	Bit Name	Initial Value	R/W	Description
7	KBTS	0	R/W	Transmit Start Selects start of data transmission or disables transmission. 0: Data transmission is disabled [Clearing conditions] • When 0 is written • When the KBTE is set to 1 • When the KBIOE is cleared to 0 1: Starts data transmission [Setting condition] When 1 is written after reading the KBTS = 0
6	PS	0	R/W	Transmit Parity Selection Selects even or odd parity. 0: Selects odd parity 1: Selects even parity
5	KCIE	0	R/W	First KCLK Falling Interrupt Enable Selects whether an interrupt at the first falling edge of KCLK is enabled or disabled. 0: Disables first KCLK falling interrupt 1: Enables first KCLK falling interrupt
4	KTIE	0	R/W	Transmit Completion Interrupt Enable Selects whether a transmit completion interrupt is enabled or disabled. 0: Disables transmit completion interrupt 1: Enables transmit completion interrupt
3	—	0	—	Reserved The initial value should not be changed.

20.4.5 LPC Interface Serialized Interrupt Operation (SERIRQ)

A host interrupt request can be issued from the LPC interface by means of the SERIRQ pin. In a host interrupt request via the SERIRQ pin, LCLK cycles are counted from the start frame of the serialized interrupt transfer cycle generated by the host or a peripheral function, and a request signal is generated by the frame corresponding to that interrupt. The timing is shown in figure 20.6.

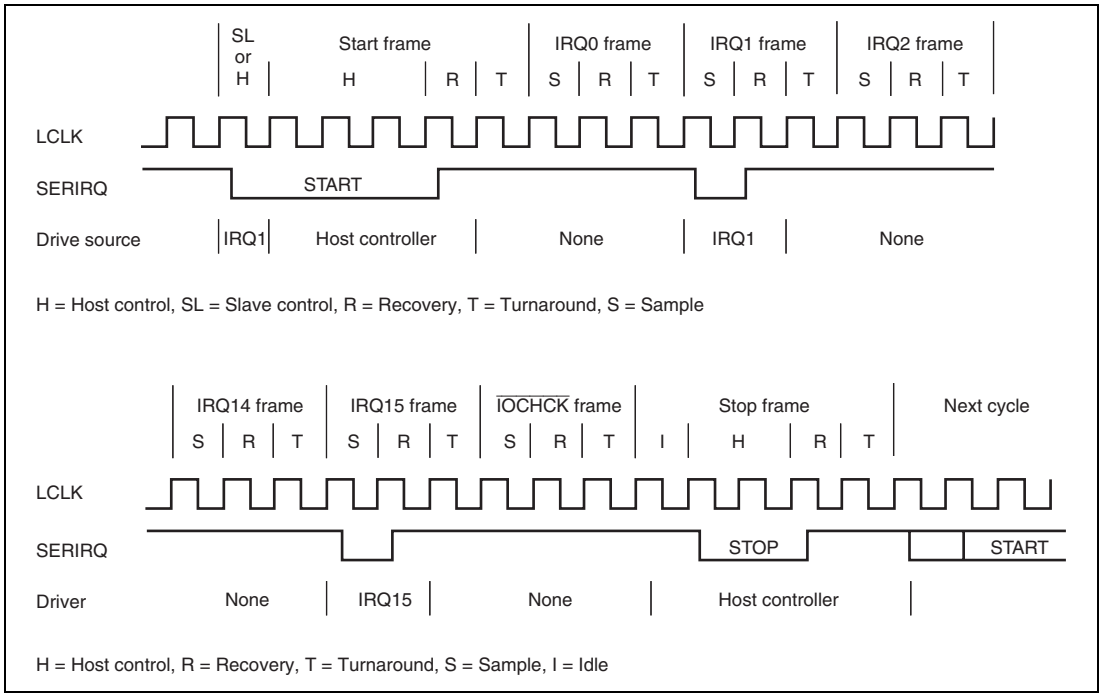


Figure 20.6 SERIRQ Timing

The serialized interrupt transfer cycle frame configuration is as follows. Two of the states comprising each frame are the recover state in which the SERIRQ signal is returned to the 1-level at the end of the frame, and the turnaround state in which the SERIRQ signal is not driven. The recover state must be driven by the host or slave that was driving the preceding state.

(2) Flash Pass and Fail Parameter (FPFR: General Register R0L of CPU)

FPFR indicates the return values of the initialization, programming, and erasure results. The meaning of the bits in FPFR varies depending on the processing.

(a) Initialization before programming/erasing

FPFR indicates the return value of the initialization result.

Bit	Bit Name	Initial Value	R/W	Description
7 to 2	—	—	—	Unused These bits return 0.
1	FQ	—	R/W	Frequency Error Detect Compares the specified CPU operating frequency with the operating frequencies supported by this LSI, and returns the result. 0: Setting of operating frequency is normal 1: Setting of operating frequency is abnormal
0	SF	—	R/W	Success/Fail Returns the initialization result. 0: Initialization has ended normally (no error) 1: Initialization has ended abnormally (error occurs)

(1) Serial Interface Setting by Host

The SCI_1 is set to asynchronous mode, and the serial transmit/receive format is set to 8-bit data, one stop bit, and no parity.

When a transition to boot mode is made, the boot program embedded in this LSI is initiated.

When the boot program is initiated, this LSI measures the low period of asynchronous serial communication data (H'00) transmitted consecutively by the host, calculates the bit rate, and adjusts the bit rate of the SCI_1 to match that of the host.

When bit rate adjustment is completed, this LSI transmits 1 byte of H'00 to the host as the bit adjustment end sign. When the host receives this bit adjustment end sign normally, it transmits 1 byte of H'55 to this LSI. When reception is not executed normally, initiate boot mode again. The bit rate may not be adjusted within the allowable range depending on the combination of the bit rate of the host and the system clock frequency of this LSI. Therefore, the transfer bit rate of the host and the system clock frequency of this LSI must be as shown in table 24.8.

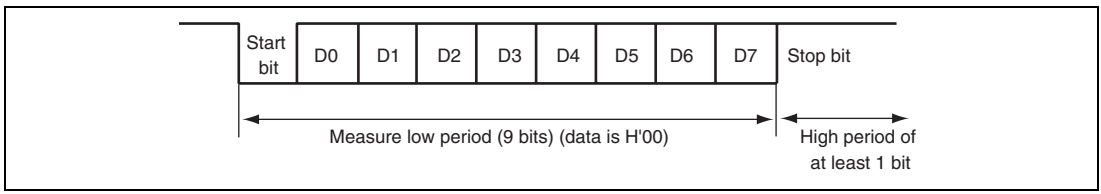


Figure 24.7 Automatic-Bit-Rate Adjustment Operation

Table 24.8 System Clock Frequency for Automatic-Bit-Rate Adjustment

Bit Rate of Host	System Clock Frequency of This LSI
9,600 bps	8 to 20 MHz
19,200 bps	8 to 20 MHz

(2) State Transition Diagram

The state transition after boot mode is initiated is shown in figure 24.8.

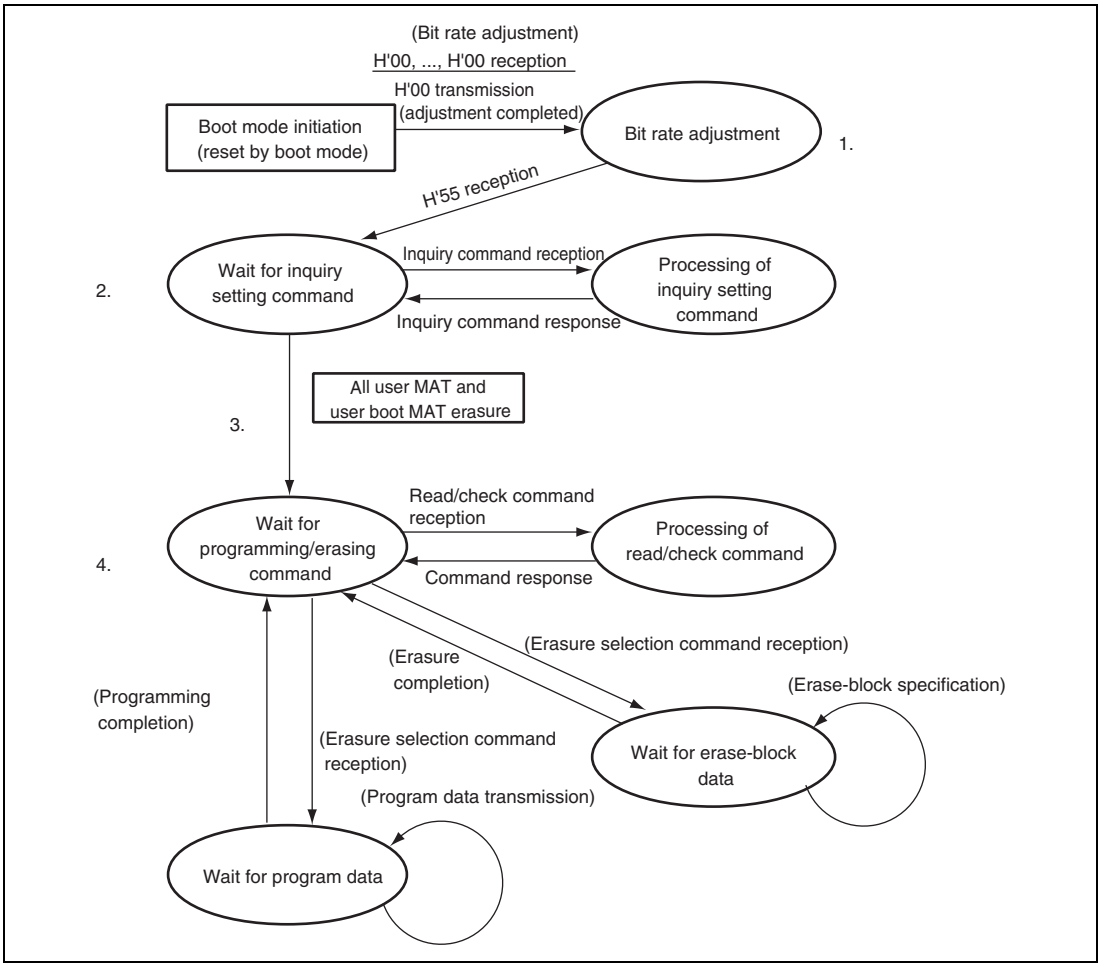


Figure 24.8 Boot Mode State Transition Diagram

In consideration of these conditions, the areas in which the program data can be stored and executed are determined by the combination of the processing contents, operating mode, and bank structure of the memory MATs, as shown in tables 24.9 to 24.13.

Table 24.9 Executable Memory MAT

	Operating Mode	
Processing Contents	**User Program Mode**	**User boot Mode***
Programming	See table 24.10.	See table 24.12
Erasing	See table 24.11.	See table 24.13

Note: * Programming/Erasing is possible to the User Mat.

Table 24.10 Usable Area for Programming in User Program Mode

	Storable/Executable Area		Selected MAT	
Item	**On-Chip RAM**	**User MAT**	**User MAT**	**Embedded Program Storage MAT**
Storage area for program data	O	×*	—	—
Operation for selecting on-chip program to be downloaded	O	O	O	
Operation for writing H'A5 to FKEY	O	O	O	
Execution of writing 1 to SCO bit in FCCS (download)	O	×		O
Operation for clearing FKEY	O	O	O	
Decision of download result	O	O	O	
Operation for download error	O	O	O	
Operation for setting initialization parameter	O	O	O	
Execution of initialization	O	×	O	
Decision of initialization result	O	O	O	
Operation for initialization error	O	O	O	
Operation for disabling interrupts	O	O	O	
Operation for writing H'5A to FKEY	O	O	O	
Operation for setting programming parameter	O	×	O	
Execution of programming	O	×	O	
Decision of programming result	O	×	O	
Operation for programming error	O	×	O	
Operation for clearing FKEY	O	×	O	

Note: * Transferring the program data to the on-chip RAM beforehand enables this area to be used.

Table 24.11 Usable Area for Erasure in User Program Mode

	Storable/Executable Area		Selected MAT	
Item	**On-Chip RAM**	**User MAT**	**User MAT**	**Embedded Program Storage MAT**
Operation for selecting on-chip program to be downloaded	O	O	O	
Operation for writing H'A5 to FKEY	O	O	O	
Execution of writing 1 to SCO bit in FCCS (download)	O	×		O
Operation for clearing FKEY	O	O	O	
Decision of download result	O	O	O	
Operation for download error	O	O	O	
Operation for setting initialization parameter	O	O	O	
Execution of initialization	O	×	O	
Decision of initialization result	O	O	O	
Operation for initialization error	O	O	O	
Operation for disabling interrupts	O	O	O	
Operation for writing H'5A to FKEY	O	O	O	
Operation for setting erasure parameter	O	×	O	
Execution of erasure	O	×	O	
Decision of erasure result	O	×	O	
Operation for erasure error	O	×	O	
Operation for clearing FKEY	O	×	O	

Register Name	Abbreviation	Number of bits	Address	Module	Data Width	Access States
SCIF address register H	SCIFADRH	8	H'FDC4	LPC	8	2
SCIF address register L	SCIFADRL	8	H'FDC5	LPC	8	2
LPC channel 4 address register H	LADR4H	8	H'FDD4	LPC	8	2
LPC channel 4 address register L	LADR4L	8	H'FDD5	LPC	8	2
Input data register 4	IDR4	8	H'FDD6	LPC	8	2
Output data register 4	ODR4	8	H'FDD7	LPC	8	2
Status register 4	STR4	8	H'FDD8	LPC	8	2
Host interface control register 4	HICR4	8	H'FDD9	LPC	8	2
SERIRQ control register 2	SIRQCR2	8	H'FDDA	LPC	8	2
SERIRQ control register 3	SIRQCR3	8	H'FDDB	LPC	8	2
Port 6 noise canceler enable register	P6NCE	8	H'FE00 (PORTS = 0)	PORT	8	2
Port 6 noise canceler decision control register	P6NCMC	8	H'FE01 (PORTS = 0)	PORT	8	2
Port 6 noise cancel cycle setting register	P6NCCS	8	H'FE02 (PORTS = 0)	PORT	8	2
Port C noise canceler enable register	PCNCE	8	H'FE03 (PORTS = 0)	PORT	8	2
Port C noise canceler decision control register	PCNCMC	8	H'FE04 (PORTS = 0)	PORT	8	2
Port C noise cancel cycle setting register	PCNCCS	8	H'FE05 (PORTS = 0)	PORT	8	2
Port G noise canceler enable register	PGNCE	8	H'FE06 (PORTS = 0)	PORT	8	2
Port G noise canceler decision control register	PGNCMC	8	H'FE07 (PORTS = 0)	PORT	8	2
Port G noise cancel cycle setting register	PGNCCS	8	H'FE08 (PORTS = 0)	PORT	8	2
Port H input data register	PHPIN	8	H'FE0C (Read) (PORTS = 0)	PORT	8	2
Port H data direction register	PHDDR	8	H'FE0C (Write) (PORTS = 0)	PORT	8	2
Port H output data register	PHODR	8	H'FE0D (PORTS = 0)	PORT	8	2
Port H Nch-OD control register	PHNOCR	8	H'FE0E (PORTS = 0)	PORT	8	2
Port control register 0	PTCNT0	8	H'FE10	PORT	8	2

Lower Address	Register Abbreviation	Register Selection Condition	Module
H'FC90	FSICR1	MSTP0 = 0	FSI
H'FC91	FSICR2	MSTPA2 = 0	
H'FC92	FSIBNR		
H'FC93	FSIINS		
H'FC94	FSIRDINS		
H'FC95	FSIPPINS		
H'FC96	FSISTR		
H'FC98	FSITDR0		
H'FC99	FSITDR1		
H'FC9A	FSITDR2		
H'FC9B	FSITDR3		
H'FC9C	FSITDR4		
H'FC9D	FSITDR5		
H'FC9E	FSITDR6		
H'FC9F	FSITDR7		
H'FCA0	FSIRDR		
H'FD00	PWMREG0_A	MSTPB0 = 0	PWMU_A
H'FD01	PWMPRE0_A		
H'FD02	PWMREG1_A		
H'FD03	PWMPRE1_A		
H'FD04	PWMREG2_A		
H'FD05	PWMPRE2_A		
H'FD06	PWMREG3_A		
H'FD07	PWMPRE3_A		
H'FD08	PWMREG4_A		
H'FD09	PWMPRE4_A		
H'FD0A	PWMREG5_A		
H'FD0B	PWMPRE5_A		
H'FD0C	PWMCONA_A		
H'FD0D	PWMCONB_A		
H'FD0E	PWMCONC_A		
H'FD0F	PWMCOND_A		

Module	Register Abbreviation	Number of Bits	Address	Data Bus Width	Access States
LPC	SCIFADRH	8	H'FDC4	8	2
LPC	SCIFADRL	8	H'FDC5	8	2
LPC	LADR4H	8	H'FDD4	8	2
LPC	LADR4L	8	H'FDD5	8	2
LPC	IDR4	8	H'FDD6	8	2
LPC	ODR4	8	H'FDD7	8	2
LPC	STR4	8	H'FDD8	8	2
LPC	HICR4	8	H'FDD9	8	2
LPC	SIRQCR2	8	H'FDDA	8	2
LPC	SIRQCR3	8	H'FDDB	8	2
LPC	TWR0MW	8	H'FE20	8	2
LPC	TWR0SW	8	H'FE20	8	2
LPC	TWR1	8	H'FE21	8	2
LPC	TWR2	8	H'FE22	8	2
LPC	TWR3	8	H'FE23	8	2
LPC	TWR4	8	H'FE24	8	2
LPC	TWR5	8	H'FE25	8	2
LPC	TWR6	8	H'FE26	8	2
LPC	TWR7	8	H'FE27	8	2
LPC	TWR8	8	H'FE28	8	2
LPC	TWR9	8	H'FE29	8	2
LPC	TWR10	8	H'FE2A	8	2
LPC	TWR11	8	H'FE2B	8	2
LPC	TWR12	8	H'FE2C	8	2
LPC	TWR13	8	H'FE2D	8	2
LPC	TWR14	8	H'FE2E	8	2
LPC	TWR15	8	H'FE2F	8	2
LPC	IDR3	8	H'FE30	8	2
LPC	ODR3	8	H'FE31	8	2
LPC	STR3	8	H'FE32	8	2
LPC	HICR5	8	H'FE33	8	2

Item		Symbol	Min.	Max.	Unit	Test Conditions
SCI	Input clock rise time	t_{SCKr}	—	1.5	t_{cyc}	Figure 28.20
	Input clock fall time	t_{SCKf}	—	1.5		
	Transmit data delay time (synchronous)	t_{TXD}	—	50	ns	Figure 28.21
	Receive data setup time (synchronous)	t_{RXS}	50	—		
	Receive data hold time (synchronous)	t_{RXH}	50	—		
FSI	Clock cycle	t_{CYC}	30	—	ns	Figure 28.22
	Clock pulse width (high)	t_{CKH}	13	—		
	Clock pulse width (low)	t_{CKL}	13	—		
	SS signal rise delay time	t_{SSH}	12	—		
	SS signal fall delay time	t_{SSL}	12	—		
	Transmit signal delay time	t_{TXD}	—	12		
	Receive signal setup time	t_{RXS}	5	—		
	Receive signal hold time	t_{RXH}	5	—		

Notes: 1. Applied only for the peripheral modules that are available during subclock operation.
2. Other than P52, P97, P86, P42, port A, port G, and port I.

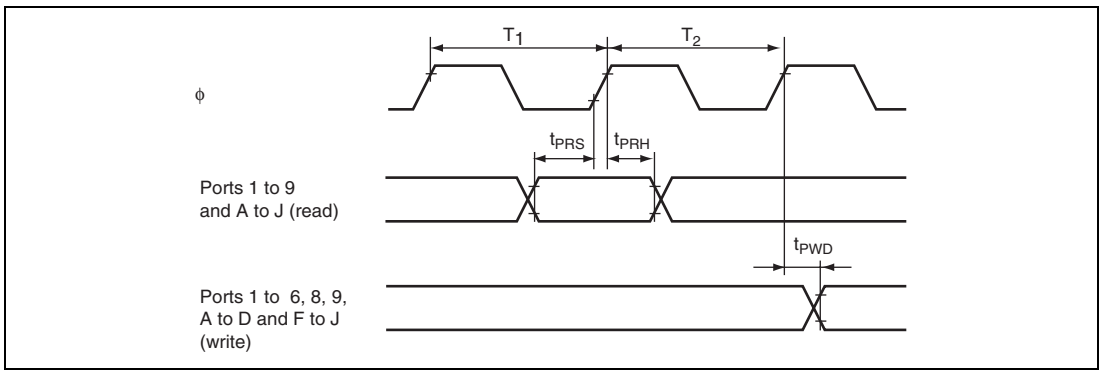


Figure 28.9 I/O Port Input/Output Timing

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