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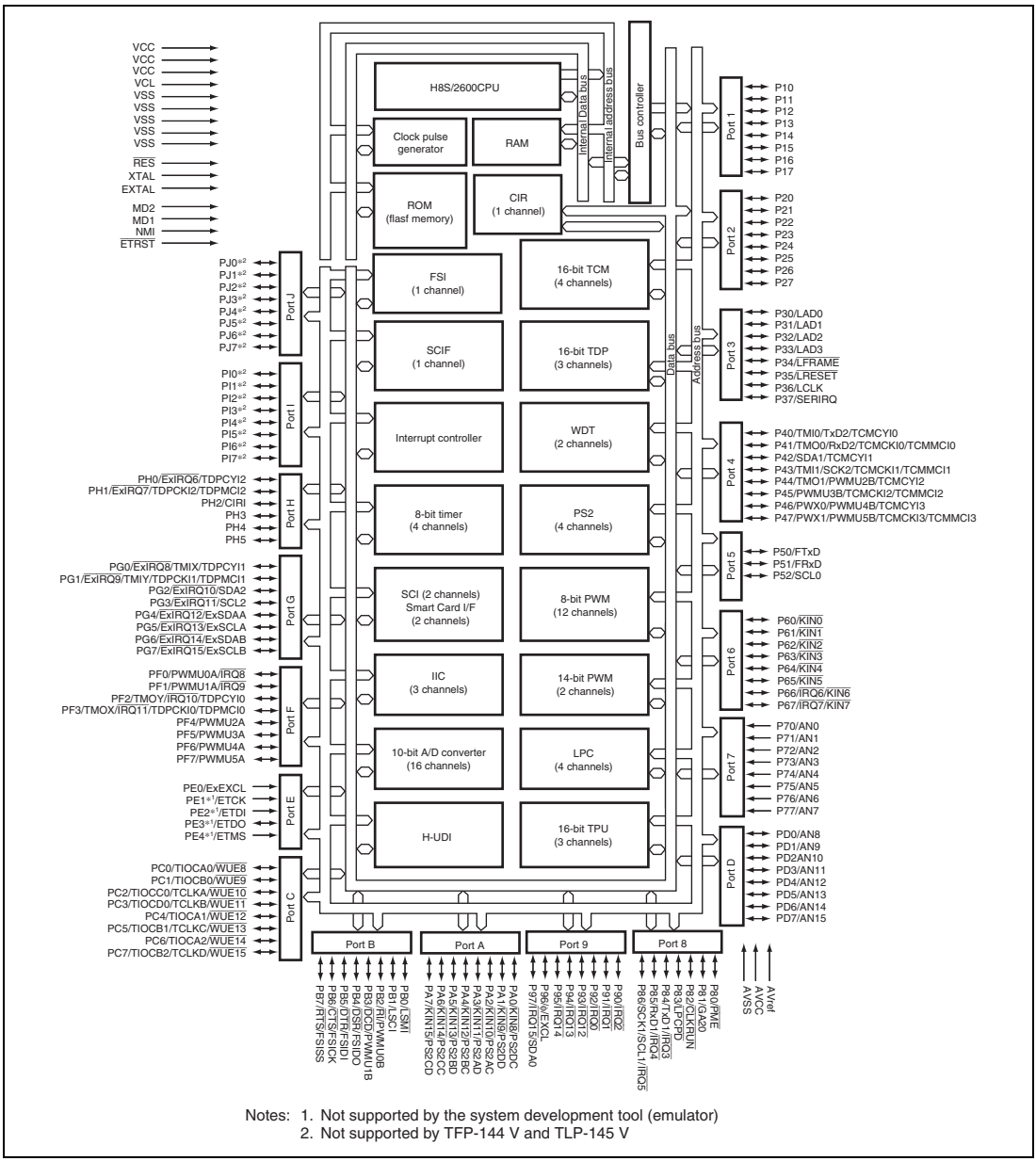
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8S/2600
Core Size	16-Bit
Speed	20MHz
Connectivity	FIFO, I²C, LPC, SCI, SmartCard
Peripherals	POR, PWM, WDT
Number of I/O	112
Program Memory Size	160KB (160K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	144-TQFP
Supplier Device Package	144-TQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2117rvt20v

1.3 Block Diagram



Notes: 1. Not supported by the system development tool (emulator)
2. Not supported by TFP-144 V and TLP-145 V

Figure 1.2 Internal Block Diagram

2.1.2 Differences from H8/300 CPU

In comparison to the H8/300 CPU, the H8S/2600 CPU has the following enhancements:

- More general registers and control registers
  - Eight 16-bit extended registers, and one 8-bit and two 32-bit control registers, have been added.
- Expanded address space
  - Normal mode supports the same 64-kbyte address space as the H8/300 CPU.
  - Advanced mode supports a maximum 16-Mbyte address space.
- Enhanced addressing
  - The addressing modes have been enhanced to make effective use of the 16-Mbyte address space.
- Enhanced instructions
  - Addressing modes of bit-manipulation instructions have been enhanced.
  - Signed multiply and divide instructions have been added.
  - A multiply-and-accumulate instruction has been added.
  - Two-bit shift instructions have been added.
  - Instructions for saving and restoring multiple registers have been added.
  - A test and set instruction has been added.
- Higher speed
  - Basic instructions execute twice as fast.

2.1.3 Differences from H8/300H CPU

In comparison to the H8/300H CPU, the H8S/2600 CPU has the following enhancements:

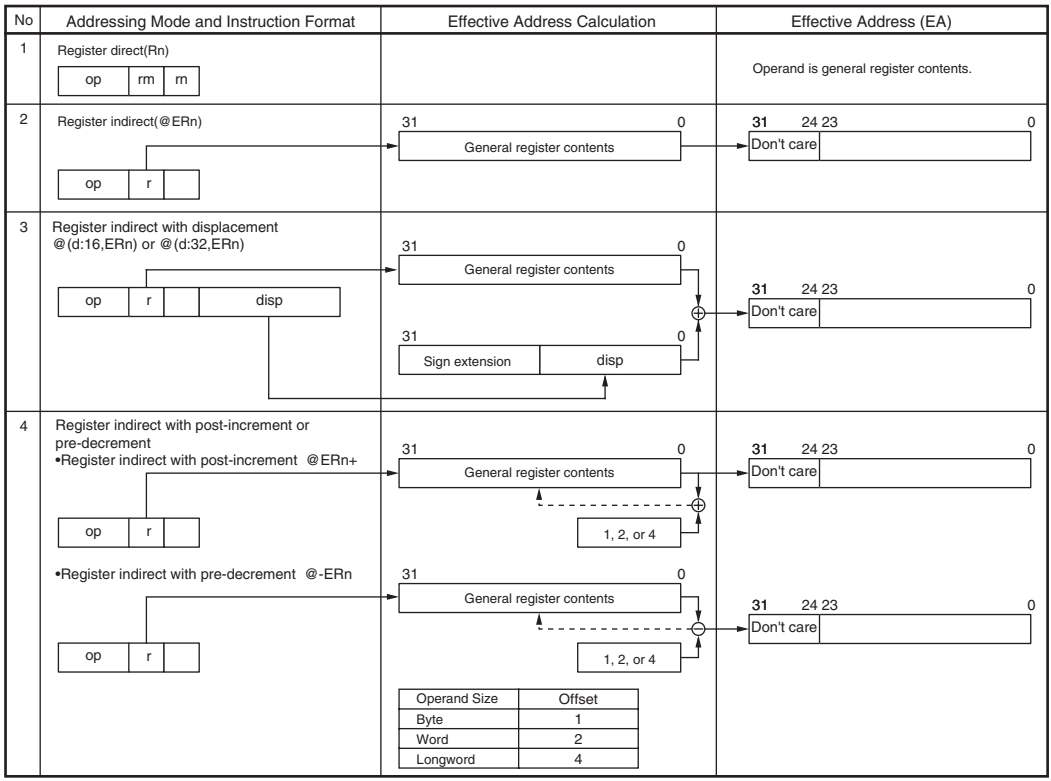
- More control registers
  - One 8-bit and two 32-bit control registers have been added.
- Enhanced instructions
  - Addressing modes of bit-manipulation instructions have been enhanced.
  - A multiply-and-accumulate instruction has been added.
  - Two-bit shift instructions have been added.
  - Instructions for saving and restoring multiple registers have been added.
  - A test and set instruction has been added.
- Higher speed
  - Basic instructions execute twice as fast.

2.7.9 Effective Address Calculation

Table 2.13 indicates how effective addresses are calculated in each addressing mode. In normal mode the upper 8 bits of the effective address are ignored in order to generate a 16-bit address.

Note: Normal mode is not available in this LSI.

Table 2.13 Effective Address Calculation (1)



Section 3 MCU Operating Modes

3.1 Operating Mode Selection

This LSI supports three operating modes (modes 2, 4, and 6). The operating mode is determined by the setting of the mode pins (MD2 and MD1). Table 3.1 shows the MCU operating mode selection.

Table 3.1 MCU Operating Mode Selection

MCU Operating Mode	MD2	MD1	MD0*	CPU Operating Mode	Description	On-Chip ROM
2	0	1	0	Advanced	Single-chip mode	Enabled
4	1	0	0	—	Flash memory programming/erasing	—
6	1	1	0	Emulation	On-chip emulation mode	Enabled

Note: * MD0 is not available as a pin and is internally fixed to 0.

Modes 2 is single-chip mode.

Modes 0, 1, 3, 5 and 7 are not available in this LSI. Modes 4 and 6 are operating modes for a special purpose. Thus, mode pins should be set to enable mode 2 in the normal program execution state. Mode pin settings should not be changed during operation. After a reset is canceled, the mode pin inputs should be latched by reading MDCR.

Mode 4 is a boot mode for programming or erasing the flash memory. For details, see section 24, Flash Memory.

Mode 6 is an on-chip emulation mode. In this mode, this LSI is controlled by an on-chip emulator (E10A) via the JTAG, thus enabling on-chip emulation.

Table 5.6 Interrupt Sources, Vector Addresses, and Interrupt Priorities (Extended Vector Mode)

Origin of Interrupt Source	Name	Vector Number	Vector Address: Advanced Mode	ICR	Priority
External pin	NMI	7	H'00001C	—	High
	IRQ0	16	H'000040	ICRA7	
	IRQ1	17	H'000044	ICRA6	
	IRQ2	18	H'000048	ICRA5	
	IRQ3	19	H'00004C		
	IRQ4	20	H'000050	ICRA4	
	IRQ5	21	H'000054		
	IRQ6	22	H'000058	ICRA3	
	IRQ7	23	H'00005C		
—	Reserved for system use	24	H'000060	—	
WDT_0	WOVI0 (Interval timer)	25	H'000064	ICRA1	
WDT_1	WOVI1 (Interval timer)	26	H'000068	ICRA0	
—	Address break	27	H'00006C	—	
A/D converter	ADI (A/D conversion end)	28	H'000070	ICRB7	
—	Reserved for system use	29	H'000074	—	
External pin	KIN7 to KIN0	30	H'000078	ICRD5	
	KIN15 to KIN8	31	H'00007C		
—	Reserved for system use	32	H'000080	—	
External pin	WUE15 to WUE8	33	H'000084	ICRD4	
TPU_0	TGI0A (TGR0A input capture/compare match)	34	H'000088	ICRD3	
	TGI0B (TGR0B input capture/compare match)	35	H'00008C		
	TGI0C (TGR0C input capture/compare match)	36	H'000090		
	TGI0D (TGR0D input capture/compare match)	37	H'000094		
	TGI0V (Overflow 0)	38	H'000098		
TPU_1	TGI1A (TGR1A input capture/compare match)	39	H'00009C	ICRD2	
	TGI1B (TGR1B input capture/compare match)	40	H'0000A0		
	TGI1V (Overflow 1)	41	H'0000A4		
	TGI1U (Underflow 1)	42	H'0000A8		Low

7.1.5 Output Data Register (PnODR) (n = A to D and F to J)

ODR is a register that stores output data for ports. The upper two bits in PHODR are reserved.

Bit	Bit Name	Initial Value	R/W	Description
7	Pn7ODR	0	R/W	ODR stores the output data for the pins that are used as the general output port.
6	Pn6ODR	0	R/W	
5	Pn5ODR	0	R/W	
4	Pn4ODR	0	R/W	
3	Pn3ODR	0	R/W	
2	Pn2ODR	0	R/W	
1	Pn1ODR	0	R/W	
0	Pn0ODR	0	R/W	

7.1.6 Noise Canceler Enable Register (PnNCE) (n = 6, C, and G)

NCE enables or disables the noise cancel circuit at port n pins in bit units.

Bit	Bit Name	Initial Value	R/W	Description
7	Pn7NCE	0	R/W	Noise cancel circuit is enabled when a bit in this register is set to 1, and the pin setting state is fetched in P6DR or PnPIN in the sampling cycle set by the PnNCCS.
6	Pn6NCE	0	R/W	
5	Pn5NCE	0	R/W	
4	Pn4NCE	0	R/W	
3	Pn3NCE	0	R/W	
2	Pn2NCE	0	R/W	
1	Pn1NCE	0	R/W	
0	Pn0NCE	0	R/W	

Section 8 8-Bit PWM Timer (PWMU)

This LSI has two channels of 8-bit PWM timers, A and B (PWMU_A and PWMU_B). Each PWMU outputs 6 PWM waveforms. Each of the PWM channels of a PWMU can operate independently. A PWMU allows long-period PWM outputs for six channels in 8-bit single-pulse mode and for three channels in 16-bit single-pulse mode. In addition, PWM outputs at a high carrier frequency are available in 8-bit pulse division mode. Connecting a low-pass filter externally to the LSI allows the PWMU to be used as an 8-bit D/A converter.

8.1 Features

- Selectable from four types of counter input clock
  Selection of four internal clock signals (ϕ, ϕ/2, ϕ/4, and ϕ/8)
- Independent operation and variable cycle for each channel
  Cascaded connection of two channels is possible.
  Operation of channel 1 (higher order) and channel 0 (lower order) as a 16-bit single-pulse PWM timer
  Operation of channel 3 (higher order) and channel 2 (lower order) as a 16-bit single-pulse PWM timer
  Operation of channel 5 (higher order) and channel 4 (lower order) as a 16-bit single-pulse PWM timer
- 8-bit single pulse mode
  Operates at a maximum carrier frequency of 78.1 kHz (at 20 MHz operation)
  Pulse output settable with a duty cycle from 0/255 to 255/255
  PWM output enable/disable control, and selection of direct or inverted PWM output
- 16-bit single pulse mode
  Two channels are cascade-connected for operation in this mode.
  Operates at a maximum carrier frequency of 305.1 Hz (at 20 MHz operation)
  Pulse output settable with a duty cycle from 0/65535 to 65535/65535
  PWM output enable/disable control, and selection of direct or inverted PWM output
- 8-bit pulse division mode
  Operable at a maximum carrier frequency of 1.25 MHz (at 20 MHz operation)
  Pulse output settable with a duty cycle from 0/16 to 15/16
  PWM output enable/disable control, and selection of direct or inverted PWM output

(3) Input Capture Function

The TCNT value can be transferred to TGR on detection of the TIOC pin input edge. Rising edge, falling edge, or both edges can be selected as the detected edge.

(a) Example of input capture operation setting procedure

Figure 10.12 shows an example of the input capture operation setting procedure.

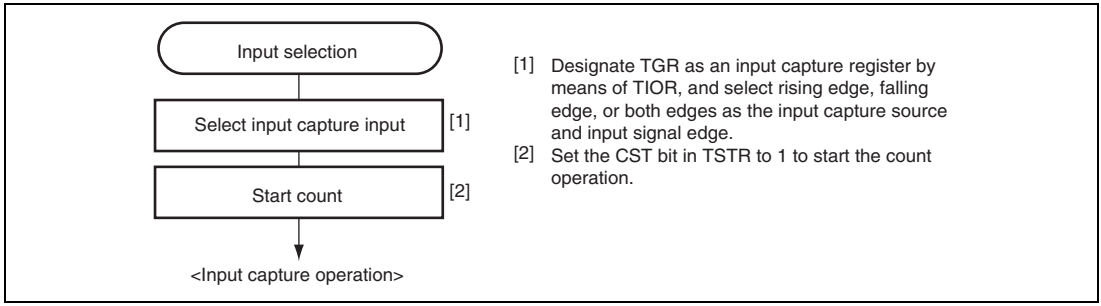


Figure 10.12 Example of Input Capture Operation Setting Procedure

(2) Examples of Buffer Operation

(a) When TGR is an output compare register

Figure 10.19 shows an operation example in which PWM mode 1 has been designated for channel 0, and buffer operation has been designated for TGRA and TGRC. The settings used in this example are TCNT clearing by compare match B, 1 output at compare match A, and 0 output at compare match B. As buffer operation has been set, when compare match A occurs the output changes and the value in buffer register TGRC is simultaneously transferred to timer general register TGRA. This operation is repeated each time compare match A occurs. For details of PWM modes, see section 10.5.4, PWM Modes.

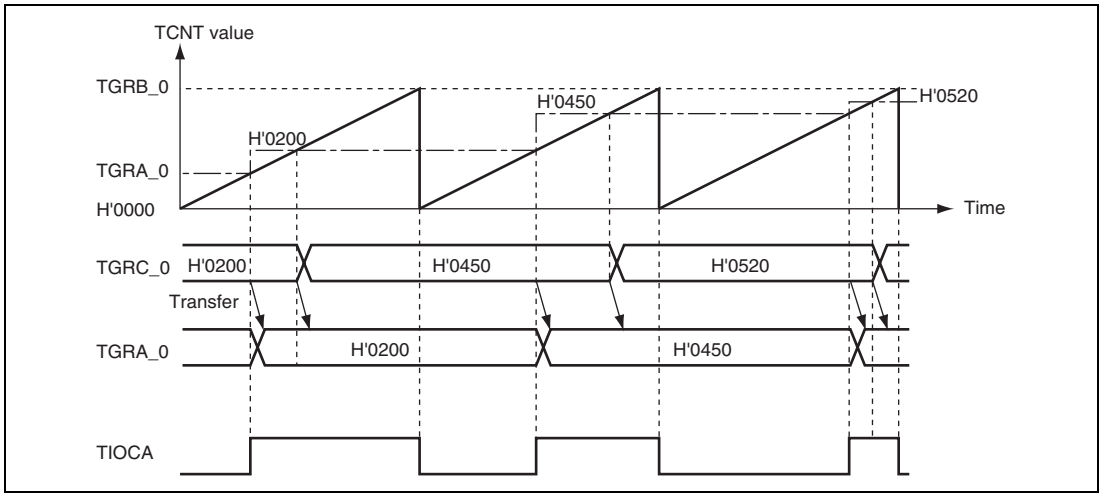


Figure 10.19 Example of Buffer Operation (1)

10.8.8 Conflict between TGR Write and Input Capture

If the input capture signal is generated in the T_2 state of a TGR write cycle, the input capture operation takes precedence and the write to TGR is not performed. Figure 10.49 shows the timing in this case.

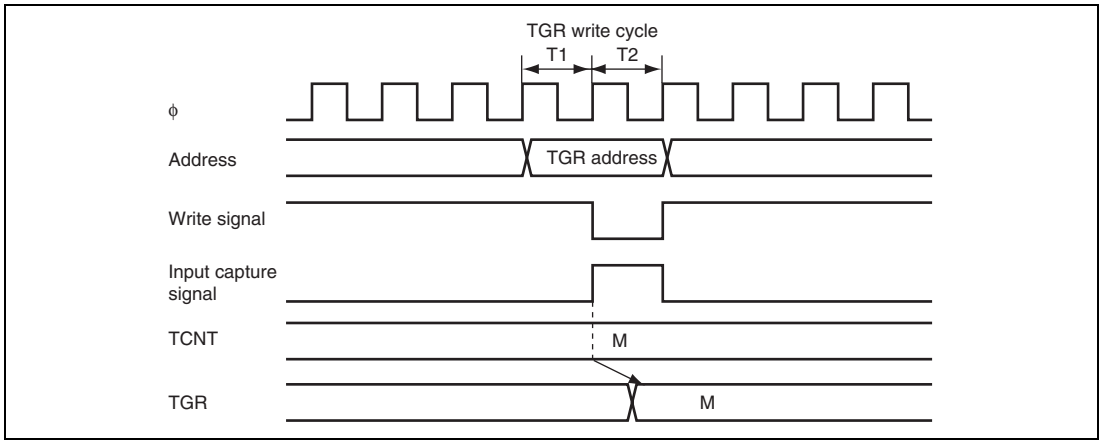


Figure 10.49 Conflict between TGR Write and Input Capture

Channel	Register Name	Abbreviation	R/W	Initial Value	Address	Data Bus Width
Channel 1	TCM timer counter_1	TCMCNT_1	R/W	H'0000	H'FBD0	16
	TCM cycle upper limit register_1	TCMMLCM_1	R/W	H'FFFF	H'FBD2	16
	TCM cycle lower limit register_1	TCMMINCM_1	R/W	H'0000	H'FBDC	16
	TCM input capture register_1	TCMICR_1	R	H'0000	H'FBD4	16
	TCM input capture buffer register_1	TCMICRF_1	R	H'0000	H'FBD6	16
	TCM status register_1	TCMCSR_1	R/W	H'00	H'FBD8	8
	TCM control register_1	TCMCR_1	R/W	H'00	H'FBD9	8
	TCM interrupt enable register_1	TCMIER_1	R/W	H'00	H'FBDA	8
Channel 2	TCM timer counter_2	TCMCNT_2	R/W	H'0000	H'FBE0	16
	TCM cycle upper limit register_2	TCMMLCM_2	R/W	H'FFFF	H'FBE2	16
	TCM cycle lower limit register_2	TCMMINCM_2	R/W	H'0000	H'FBEC	16
	TCM input capture register_2	TCMICR_2	R	H'0000	H'FBE4	16
	TCM input capture buffer register_2	TCMICRF_2	R	H'0000	H'FBE6	16
	TCM status register_2	TCMCSR_2	R/W	H'00	H'FBE8	8
	TCM control register_2	TCMCR_2	R/W	H'00	H'FBE9	8
	TCM interrupt enable register_2	TCMIER_2	R/W	H'00	H'FBEA	8
Channel 3	TCM timer counter_3	TCMCNT_3	R/W	H'0000	H'FBF0	16
	TCM cycle upper limit register_3	TCMMLCM_3	R/W	H'FFFF	H'FBF2	16
	TCM cycle lower limit register_3	TCMMINCM_3	R/W	H'0000	H'FBFC	16
	TCM input capture register_3	TCMICR_3	R	H'0000	H'FBF4	16
	TCM input capture buffer register_3	TCMICRF_3	R	H'0000	H'FBF6	16
	TCM status register_3	TCMCSR_3	R/W	H'00	H'FBF8	8
	TCM control register_3	TCMCR_3	R/W	H'00	H'FBF9	8
	TCM interrupt enable register_3	TCMIER_3	R/W	H'00	H'FBFA	8

Channel	Register Name	Abbreviation	R/W	Initial Value	Address	Data Bus Width
Channel 1	TDP timer counter_1	TDPCNT_1	R/W	H'0000	H'FB60	16
	TDP pulse width upper limit register_1	TDPWDMX_1	R/W	H'FFFF	H'FB62	16
	TDP pulse width lower limit register_1	TDPWDMN_1	R/W	H'0000	H'FB64	16
	TDP cycle upper limit register_1	TDPPDMX_1	R/W	H'FFFF	H'FB66	16
	TDP cycle lower limit register_1	TDPPDMN_1	R/W	H'0000	H'FB70	16
	TDP input capture register_1	TDPICR_1	R	H'0000	H'FB68	16
	TDP input capture buffer register_1	TDPICRF_1	R	H'0000	H'FB6A	16
	TDP status register_1	TDPCSR_1	R/W	H'00	H'FB6C	8
	TDP control register1_1	TDPCR1_1	R/W	H'00	H'FB6D	8
	TDP control register2_1	TDPCR2_1	R/W	H'00	H'FB6F	8
	TDP interrupt enable register_1	TDPIER_1	R/W	H'00	H'FB6E	8
Channel 2	TDP timer counter_2	TDPCNT_2	R/W	H'0000	H'FB80	16
	TDP pulse width upper limit register_2	TDPWDMX_2	R/W	H'FFFF	H'FB82	16
	TDP pulse width lower limit register_2	TDPWDMN_2	R/W	H'0000	H'FB84	16
	TDP cycle upper limit register_2	TDPPDMX_2	R/W	H'FFFF	H'FB86	16
	TDP cycle lower limit register_2	TDPPDMN_2	R/W	H'0000	H'FB90	16
	TDP input capture register_2	TDPICR_2	R	H'0000	H'FB88	16
	TDP input capture buffer register_2	TDPICRF_2	R	H'0000	H'FB8A	16
	TDP status register_2	TDPCSR_2	R/W	H'00	H'FB8C	8
	TDP control register 1_2	TDPCR1_2	R/W	H'00	H'FB8D	8
	TDP control register 2_2	TDPCR2_2	R/W	H'00	H'FB8F	8
	TDP interrupt enable register_2	TDPIER_2	R/W	H'00	H'FB8E	8

12.3.6 TDP Input Capture Register (TDPICR)

TDPICR is a 16-bit read-only register. In timer mode, the TDPCNT value is transferred to TDPICR on the edge selected by the IEDG bit in TDPCR1, and the ICPF flag in TDPCSR is set to 1. In cycle measurement mode, the TDPCNT value is transferred to TDPICR when the first edge of the measurement period is detected. At the same time, the ICPF flag in TDPCSR is set to 1. TDPICR must always be accessed in 16-bit units and cannot be accessed in 8-bit units. TDPICR is initialized to H'0000.

12.3.7 TDP Input Capture Buffer Register (TDPICRF)

TDPICRF is a 16-bit read-only register. TDPICRF can be used as a TDPICR buffer register. When input capture occurs, the TDPICR value is transferred to TDPICRF.

TDPICRF must always be accessed in 16-bit units and cannot be accessed in 8-bit units. TDPICRF is initialized to H'0000.

12.3.8 TDP Status Register (TDPCSR)

TDPCSR indicates the status flags and selects the external clock edge.

Bit	Bit Name	Initial Value	R/W	Description
7	OVF	0	R/(W)*	Timer Overflow This flag indicates a TDPCNT overflow. [Setting condition] • TDPCNT overflow (H'FFFF changes to H'0000) [Clearing condition] • Reading OVF when OVF = 1 and then writing 0 to OVF
6	TWDMXOVF	0	R/(W)*	Pulse Width Upper Limit Overflow This flag indicates that the waveform pulse width measured in cycle measurement mode has exceeded the upper limit specified in TDPWDMX. [Setting condition] • When TDPICR is greater than TDPWDMX [Clearing condition] • Reading TWDMXOVF when TWDMXOVF = 1 and then writing 0 to TWDMXOVF

13.9.6 Mode Setting with Cascaded Connection

If the 16-bit count mode and compare-match count mode are set simultaneously, the input clock pulses for TCNT_0 and TCNT_1, and TCNT_X and TCNT_Y are not generated, and thus the counters will stop operating. Simultaneous setting of these two modes should therefore be avoided.

13.9.7 Module Stop Mode Setting

TMR operation can be enabled or disabled using the module stop control register. The initial setting is for TMR operation to be halted. Register access is enabled by canceling the module stop mode. For details, see section 26, Power-Down Modes.

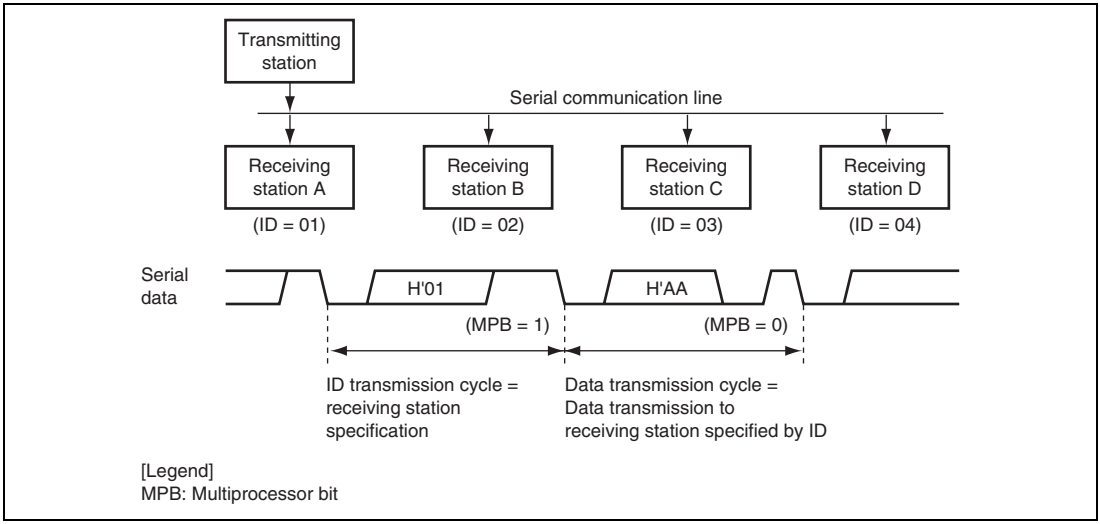


Figure 15.10 Example of Communication Using Multiprocessor Format (Transmission of Data H'AA to Receiving Station A)

Bit	Bit Name	Initial Value	R/W	Description
3	REND	0	R/W*	Reception End Flag [Setting condition] When the CIR has finished data reception. (When a stop is detected.) [Clearing condition] When writing 0 after reading REND = 1.
2	ABF	0	R/W*	Abort Flag An internal reset is generated when an abort (transfer format) is detected. [Setting condition] When data other than logic 0 or 1 is detected. [Clearing condition] When writing 0 after reading ABF = 1.
1	FRF	0	R/W*	Framing Error Flag [Setting condition] • When a stop is detected during data reception. • When the time period of a stop is too short. [Clearing condition] When writing 0 after reading FRF = 1.
0	HEADF	0	R/W*	Header Detection Flag [Setting condition] When a header is detected. [Clearing condition] When writing 0 after reading HEADF = 1.

Note: * Only 0 can be written to clear the flag.

Section 17 Serial Communication Interface with FIFO (SCIF)

This LSI has single-channel serial communication interface with FIFO buffers (SCIF) that supports asynchronous serial communication.

The SCIF enables asynchronous serial communication with standard asynchronous communication LSIs such as a Universal Asynchronous Receiver/Transmitter (UART). The SCIF also has independent 16-stage FIFO buffers for transmission and reception to provide efficient high-speed continuous communication.

In addition, the SCIF can be connected to the LPC interface for direct control from the LPC host.

17.1 Features

- Full-duplex communication:
  The transmitter and receiver are independent, enabling transmission and reception to be executed simultaneously. Both the transmitter and receiver use 16-stage FIFO buffering, enabling continuous transmission and continuous reception of serial data.
- On-chip baud rate generator allows any bit rate to be selected
- Modem control function
- Data length: Selectable from 5, 6, 7, and 8 bits
- Parity: Selectable from even parity, odd parity, and no parity
- Stop bit length: Selectable from 1, 1.5, and 2 bits
- Receive error detection: Parity, overrun, and framing errors
- Break detection

Table 20.5 Fast Gate A20 Output Signals

C/$\overline{D}$1	Data/Command	Internal CPU Interrupt Flag (IBF)	GA20 (P81)	Remarks
1	H'D1 command	0	Q	Turn-on sequence
0	1 data*[1]	0	1	
1	H'FF command	0	Q (1)	
1	H'D1 command	0	Q	Turn-off sequence
0	0 data*[2]	0	0	
1	H'FF command	0	Q (0)	
1	H'D1 command	0	Q	Turn-on sequence (abbreviated form)
0	1 data*[1]	0	1	
1/0	Command other than H'FF and H'D1	1	Q (1)	
1	H'D1 command	0	Q	Turn-off sequence (abbreviated form)
0	0 data*[2]	0	0	
1/0	Command other than H'FF and H'D1	1	Q (0)	
1	H'D1 command	0	Q	Cancelled sequence
1	Command other than H'D1	1	Q	
1	H'D1 command	0	Q	Retriggered sequence
1	H'D1 command	0	Q	
1	H'D1 command	0	Q	Consecutively executed sequences
0	Any data	0	1/0	
1	H'D1 command	0	Q (1/0)	

Notes: 1. Any data with bit 1 set to 1.
2. Any data with bit 1 cleared to 0.

Figure 20.5 shows the timing of the $\overline{\text{LPCPD}}$ and $\overline{\text{LRESET}}$ signals.

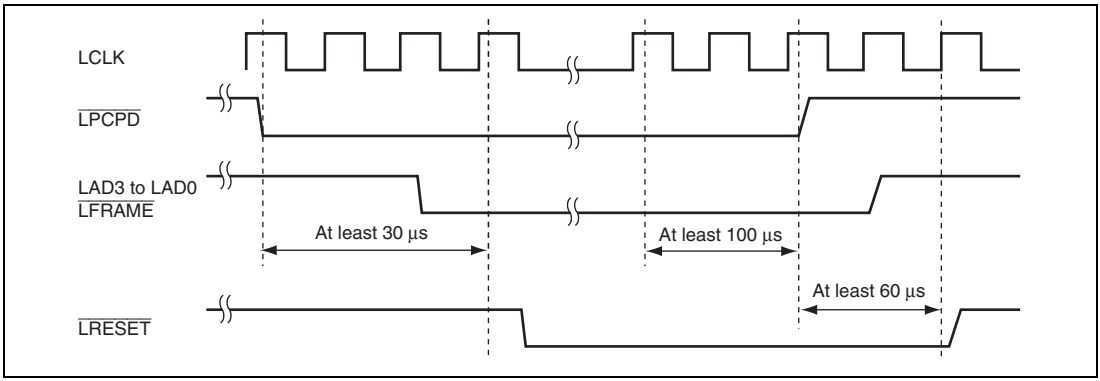


Figure 20.5 Power-Down State Termination Timing

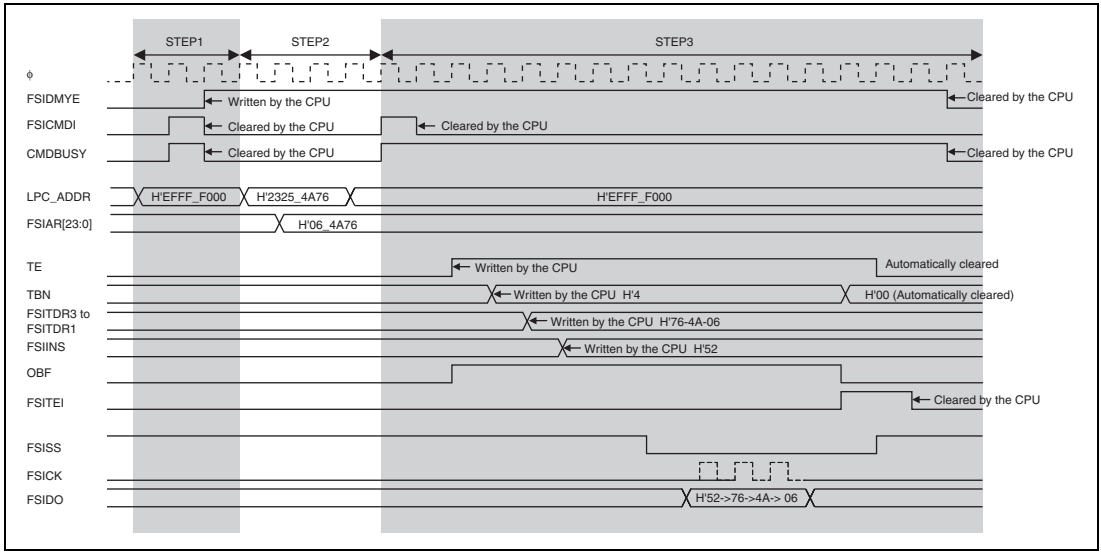


Figure 21.16 Execution Timing of SPI Flash Memory

Step 1:

1. Write an erasure setting command (Host).
2. Generate an FSICMDI interrupt request.
3. Set the FSIDMYE bit in FSILSTR1 to 1 and clear the FSICMDI and CMDBUSY bits in FSILSTR1 to 0.
4. Complete the interrupt processing.
5. Check that the FSIDMYE bit in FSILSTR1 is set to 1 and that the CMDBUSY and FSICMDI bits in FSILSTR1 are cleared to 0 (Host).

Step 2:

1. Perform a dummy write to the sector or block address to be erased (Host).
2. Store the SPI flash memory address and write data in the FSIAR register and FSIWDR register, respectively*.

Note: * Use the data stored in FSIWDR if necessary on the user side.

Step 3:

1. Write an erasure setting command (Host).
2. Generate an FSICMDI interrupt request.
3. Clear the FSICMDI bit in FSILSTR1 to 0.