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Understanding **Embedded - Microprocessors**

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MIPS-I
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	20MHz
Co-Processors/DSP	System Control; CP0
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 85°C (TC)
Security Features	-
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/idt79r3041-20j8

INTRODUCTION

The IDT RISController family is a series of high-performance 32-bit microprocessors featuring a high-level of integration, and targeted to high-performance but cost sensitive embedded processing applications. The RISController family is designed to bring the high-performance inherent in the MIPS RISC architecture into low-cost, simplified, power sensitive applications.

Thus, functional units have been integrated onto the CPU core in order to reduce the total system cost, rather than to increase the inherent performance of the integer engine. Nevertheless, the RISController family is able to offer 35MIPS of integer performance at 40MHz without requiring external SRAM or caches.

Further, the RISController family brings dramatic power reduction to these embedded applications, allowing the use of low-cost packaging. Thus, the RISController family allows customer applications to bring maximum performance at minimum cost.

The R3041 extends the range of price/performance achiev-able with the RISController family, by dramatically lowering the cost of using the MIPS architecture. The R3041 is designed to achieve minimal system and components cost, yet maintain the high-performance inherent in the MIPS architecture. The R3041 also maintains pin and software compatibility with the RISController and R3081.

The RISController family offers a variety of price/performance features in a pin-compatible, software compatible family. Table 1 provides an overview of the current members of the RISController family. Note that the R3051, R3052, and R3081 are also available in pin-compatible versions that include a full-function memory management unit, including 64-entry TLB. The R3051/2 and R3081 are described in separate manuals and data sheets.

Figure 1 shows a block level representation of the functional units within the R3041. The R3041 can be viewed as the embodiment of a discrete solution built around the R3000A. By integrating this functionality on a single chip, dramatic cost and power reductions are achieved.

An overview of these blocks is presented here, followed with detailed information on each block.

| Device Name	Instruction Cache	Data Cache	Floating Point	Bus Options
R3051	4kB	2kB	Software Emulation	Mux'ed A/D
R3052	8kB	2kB	Software Emulation	Mux'ed A/D
R3071 R3081	16kB or 8kB	4kB or 8kB	On-chip Hardware	1/2 frequency bus option
R3041	2kB	512B	Software Emulation Programmable timing support	8-, 16-, and 32-bit port width support

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Table 1. Pin-Compatible RISController Family

CPU Core

The CPU core is a full 32-bit RISC integer execution engine, capable of sustaining close to a single cycle execution rate. The CPU core contains a five stage pipeline, and 32 orthogonal 32-bit registers. The RISController family implements the MIPS-I Instruction Set Architecture (ISA). In fact, the execution engine of the R3041 is the same as the execution engine of the R3000A. Thus, the R3041 is binary compatible with those CPU engines, as well as compatible with other members of the RISController family.

The execution engine of the RISController family uses a five-stage pipeline to achieve close to single cycle execution. A new instruction can be started in every clock cycle; the execution engine actually processes five instructions concurrently (in various pipeline stages). The five parts of the pipeline are the Instruction Fetch, Read register, ALU execution, Memory, and Write Back stages. Figure 2 shows the concurrency achieved by the RISController family pipeline.
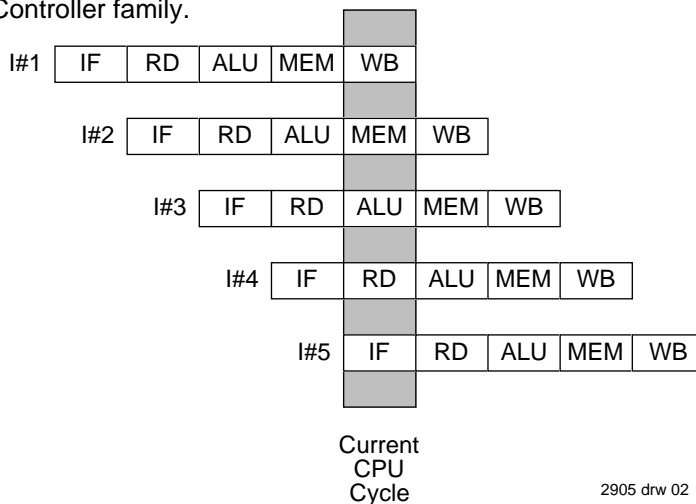
Figure 2. RISController Family 5-Stage Pipeline

System Control Co-Processor

The R3041 also integrates on-chip a System Control Co-processor, CP0. CP0 manages the exception handling capability of the R3041, the virtual to physical address mapping of the R3041, and the programmable bus interface capabilities of the R3041. These topics are discussed in subsequent sections.

The R3041 does not include the optional TLB found in other members of the RISController family, but instead performs the same virtual to physical address mapping of the base version of the RISController family. These devices still support distinct kernel and user mode operation, but do not require page management software or an on-chip TLB, leading to a simpler software model and a lower-cost processor.

The memory mapping used by these devices is illustrated in Figure 3. Note that the reserved address spaces shown are for compatibility with future family members; in the current family members, references to these addresses are translated in the same fashion as their respective segments, with no traps or exceptions taken.

When using the base versions of the architecture, the system designer can implement a distinction between the user tasks and the kernel tasks, without having to execute page management software. This distinction can take the form of physical memory protection, accomplished by ad-dress decoding, or in other system specific forms. In systems which do not wish to implement memory protection, and wish to have the kernel and user tasks operate out of a single unified memory space, upper address lines can be ignored by the address decoder, and thus all references will be seen in the lower gigabyte of the physical address space.

The R3041 adds additional resources into the on-chip CP0. These resources are detailed in the R3041 User's Manual. They allow kernel software to directly control activity of the processor internal resources and bus interface, and include:

- **Cache Configuration Register:** This register controls the data cache block size and miss refill algorithm.
- **Bus Control Register:** This register controls the behavior of the various bus interface signals.
- **Count and Compare Registers:** Together, these two registers implement a programmable 24-bit timer, which can be used for DRAM refresh or as a general purpose timer.
- **Port Size Control Register:** This register allows the kernel to indicate the port width of reads and writes to various sub-regions of the physical address space. Thus, the R3041 can interface directly with 8-, 16-, and 32-bit memory ports, including a mix of sizes, for both instruction and data references, without requiring additional external logic.
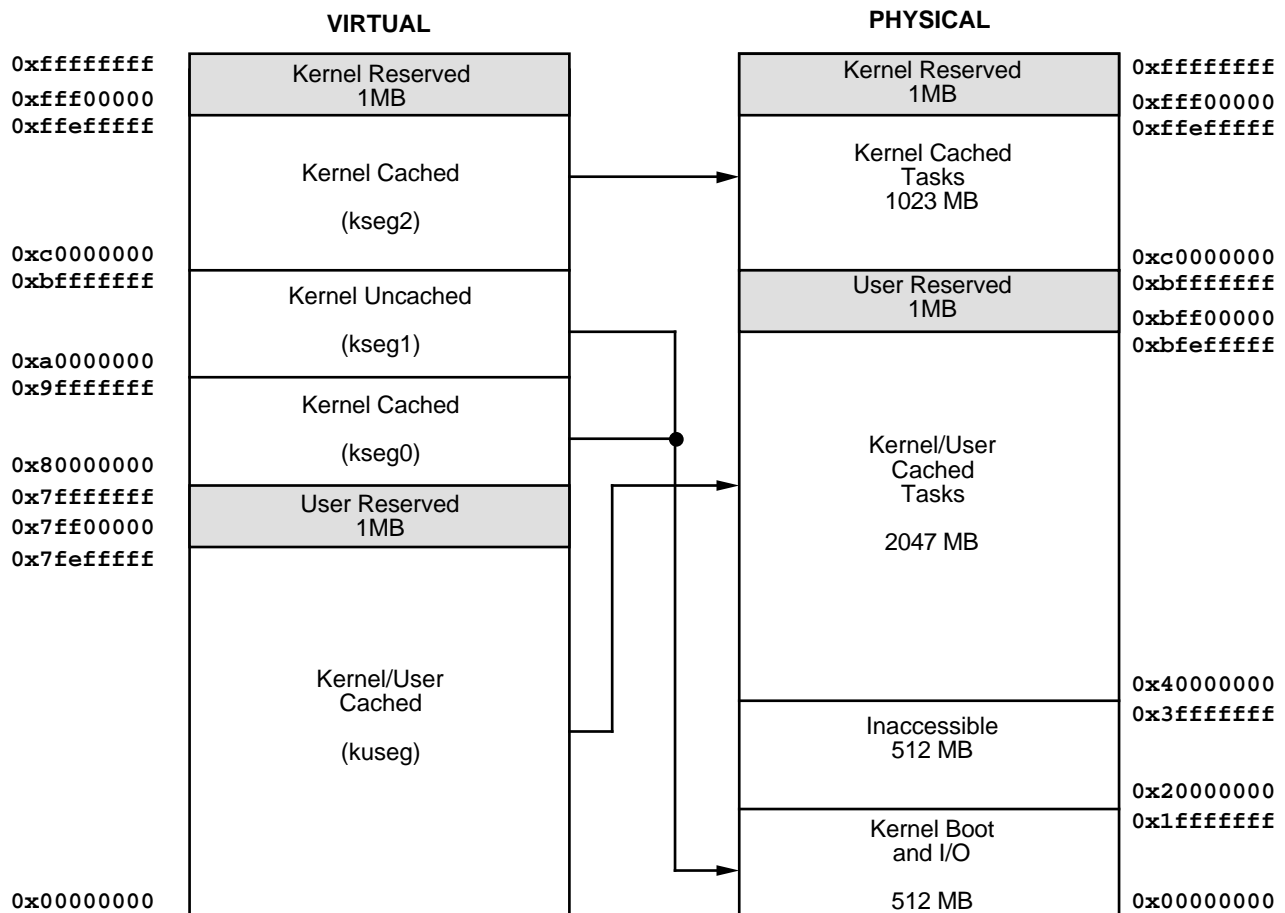
Figure 3. Virtual to Physical Mapping of Base Architecture Versions

R3041.

SYSTEM USAGE

The IDT RISController family is specifically designed to easily connect to low-cost memory systems. Typical low-cost memory systems use inexpensive EPROMs, DRAMs, and application specific peripherals.

Figure 4 shows some of the flexibility inherent in the R3041. In this example system, which is typical of a laser printer, a 32-bit PROM interface is used due to the size of the PDL interpreter. An embedded system can optionally use an 8-bit

boot PROM instead. A 16-bit font/program cartridge interface is provided for add-in cards. A 16-bit DRAM interface is used for a low-cost page frame buffer. In this system example, a field or manufacturing upgrade to a 32-bit page frame buffer is supported by the boot software and DRAM controller. Embedded systems may optionally substitute SRAMs for the DRAMs. Finally various 8/16/32-bit I/O ports such as RS-232/422, SCSI, and LAN as well as the laser printer engine interface are supported. Such a system features a very low entry price, with a range of field upgrade options including the ability to upgrade to a more powerful member of the RISController family.
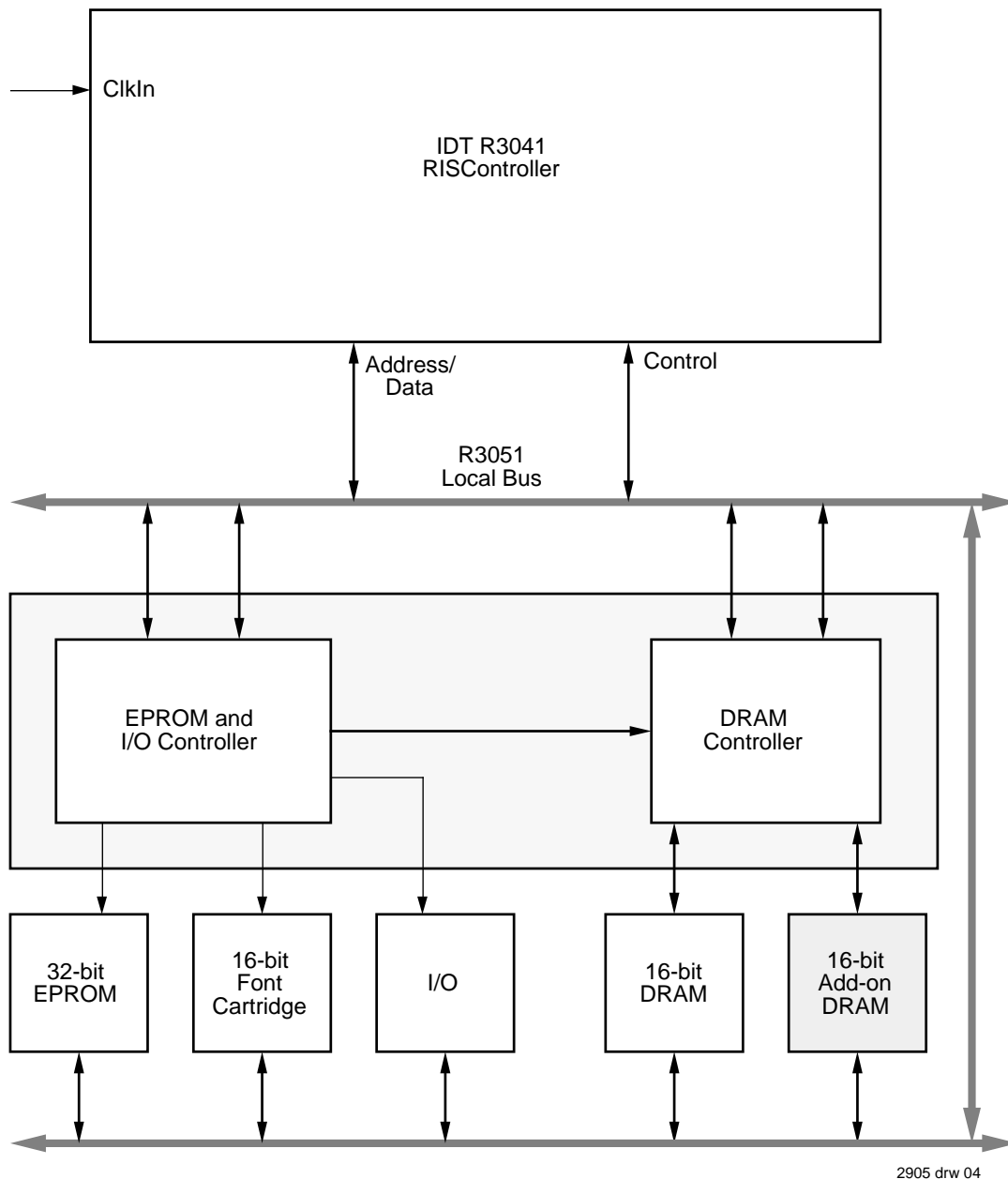

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Figure 4. Typical R3041-Based Application
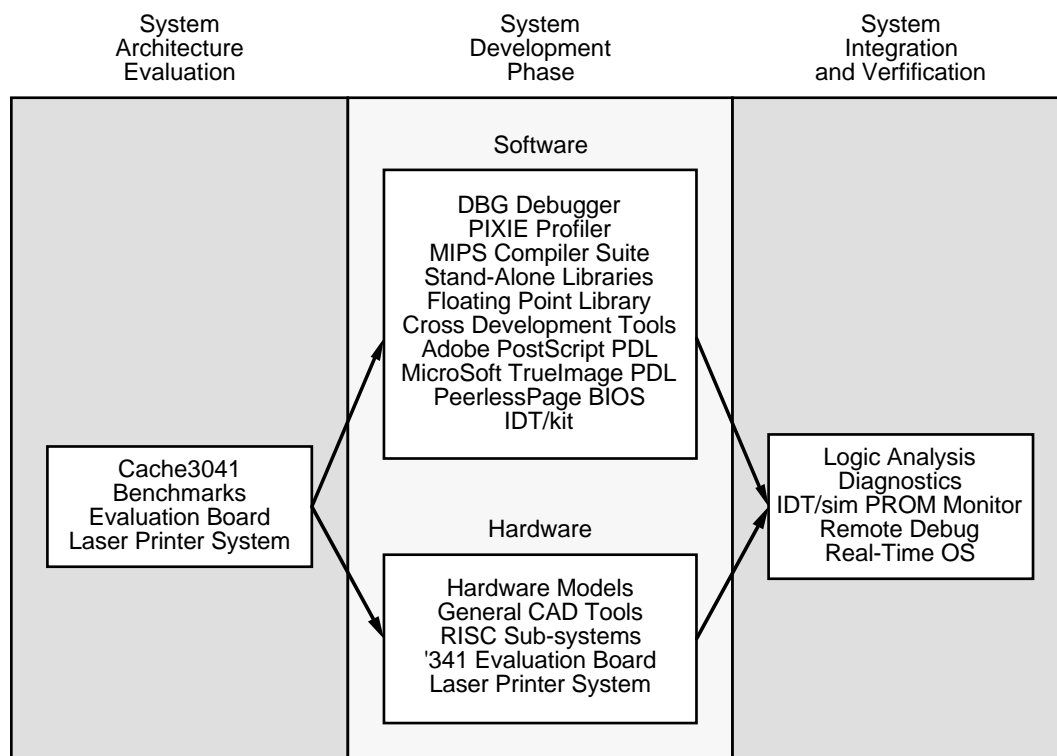
DEVELOPMENT SUPPORT

The IDT RISController family is supported by a rich set of development tools, ranging from system simulation tools through PROM monitor and debug support, applications software and utility libraries, logic analysis tools, and sub-system modules.

Figure 5 is an overview of the system development process typically used when developing R3041 applications. The RISController family is supported in all phases of project development. These tools allow timely, parallel development of hardware and software for RISController family based applications, and include tools such as:

• Optimizing compilers from MIPS Technology, the acknowl-edged leader in optimizing compiler technology.

• Cross development tools, available in a variety of development environments.

• The high-performance IDT floating point emulation library software.

• The IDT Evaluation Board, which includes RAM, EPROM, I/O, and the IDT PROM Monitor.

• IDT Laser Printer System boards, which directly drive a low-cost print engine, and runs Adobe PostScript™ Page Description Language

• Adobe PostScript Page Description Language running on the IDT RISController family.

• The IDT/sim™ PROM Monitor, which implements a full PROM monitor (diagnostics, remote debug support, peek/

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Figure 5. R3041 Development Environment

poke, etc.).
- IDT/kit™ (Kernel Integration Toolkit), providing library support and a frame work for the system run time environment.

PERFORMANCE OVERVIEW

The RISController family achieves a very high-level of performance. This performance is based on:

- **An efficient execution engine:** The CPU performs ALU operations and store operations in a single cycle, and has an effective load time of 1.3 cycles, and branch execution rate of 1.5 cycles (based on the ability of the compilers to avoid software interlocks). Thus, the R3041 achieves 20 MIPS performance at 25MHz when operating out of cache.
- **Large on-chip caches:** The RISController family contains caches which are substantially larger than those on the majority of embedded microprocessors. These large caches minimize the number of bus transactions required, and allow the RISController family to achieve actual sustained performance very close to its peak execution rate, even with low-cost memory systems.
- **Autonomous multiply and divide operations:** The RISController family features an on-chip integer multiplier/divide unit which is separate from the other ALU. This allows the R3041 to perform multiply or divide operations in parallel with other integer operations, using a single multiply or divide instruction rather than using "step" operations.
- **Integrated write buffer:** The R3041 features a four deep write buffer, which captures store target addresses and data at the processor execution rate and retires it to main memory at the slower main memory access rate. Use of on-chip write buffers eliminates the need for the processor to stall when performing store operations.
- **Burst read support:** The R3041 enables the system designer to utilize page mode, static column, or nibble mode RAMs when performing read operations to minimize the main memory read penalty and increase the effective cache hit rates.

The performance differences among the various RISController family members depends on the application software and the design of the memory system. Different family members feature different cache sizes, and the R3081 features a hardware floating point accelerator. Since all these devices can be used in a pin and software compatible fashion, the system designer has maximum freedom in trading between performance and cost. The memory simulation tools (e.g. Cache3041) allows the system designers to analyze and understand the performance differences among these de-vices in their application.

SELECTABLE FEATURES

The RISController family uses two methods to allow the system designer to configure bus interface operation options.
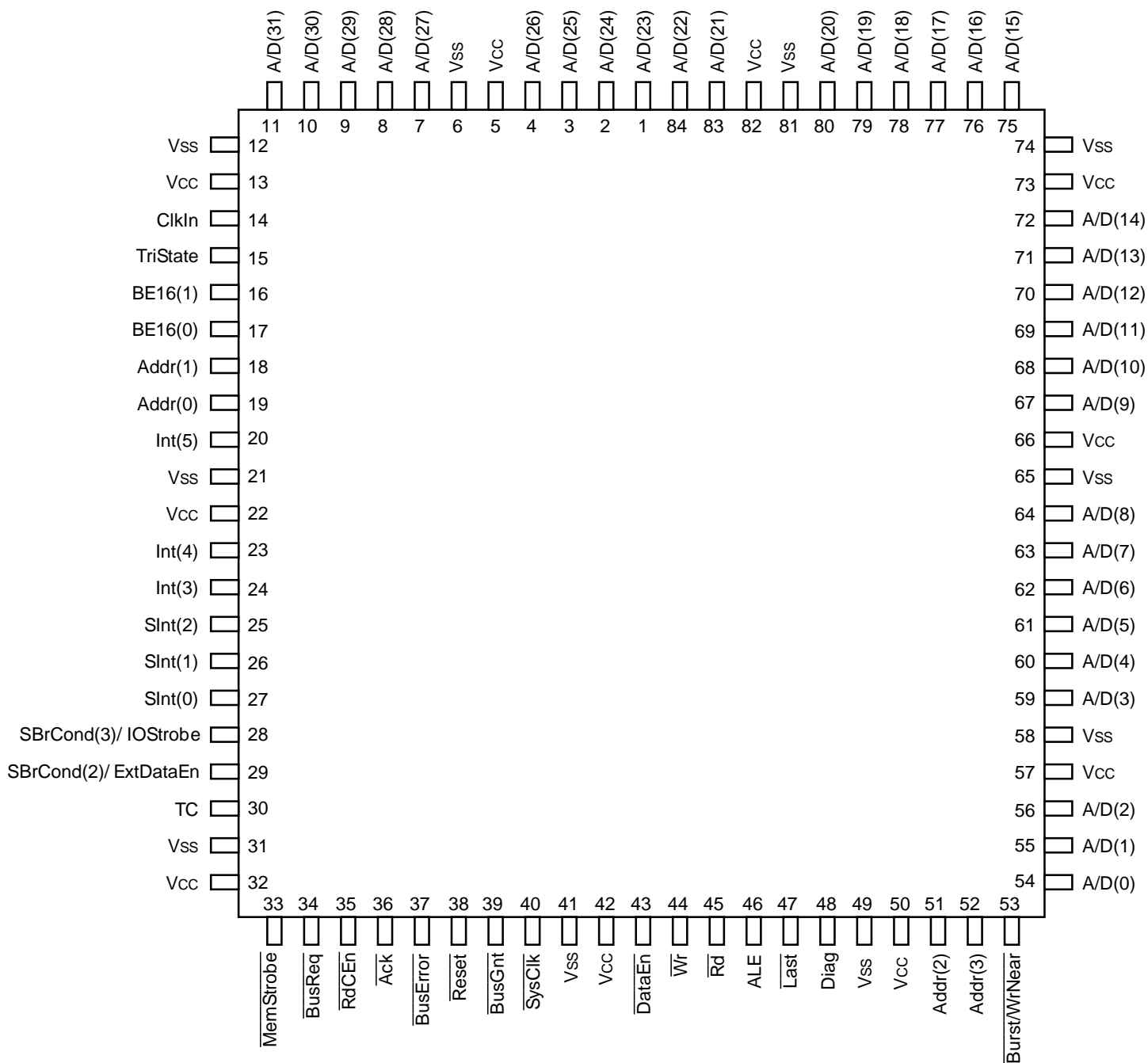
The first set of options are established via the Reset Configuration Mode inputs, sampled during the device reset. After reset, the Reset Mode inputs become regular input or output signals.

The second set of configuration options are contained in the System Control Co-Processor registers. These Co-processor registers configuration options are typically initialized with the boot PROM and can also be changed dynamically by the kernel software.

Selectable features include:

- **Big Endian vs. Little Endian operation**: The part can be configured to operate with either byte ordering convention, and in fact may also be dynamically switched between the two conventions. This facilitates the porting of applications from other processor architectures, and also permits inter-communication between various types of processors and databases.
- **Data Cache Refill of one or four words**: The memory system must be capable of performing 4 word transfers to satisfy instruction cache misses and 1 word transfers to satisfy uncached references. The data cache refill size option allows the system designers to choose between one and four word refill on data cache misses, depending on the performance each option brings to their application.
- **Bus Turn Around speed**: The R3041 allows the kernel to increase the amount of time between bus transactions when changes in direction of the A/D bus occur (e.g., at the end of reads followed by writes). This allows transceivers and buffers to be eliminated from the system.
- **Extended Address Hold Time**: The R3041 allows the system designer to increase the amount of hold time available for address latching, thus allowing slower speed (low cost) address latches, FPGAs and ASICs to be used.
- **Programmable control signals**: The R3041 allows the system designer to optimally configure various memory control signals to be active on reads only, writes only, or on both reads and writes. This allows the simplification of external logic, thus reducing system cost.

PIN CONFIGURATIONS

Top pins (left to right, pins 11–75):
A/D(31) 11, A/D(30) 10, A/D(29) 9, A/D(28) 8, A/D(27) 7, Vss 6, Vcc 5, A/D(26) 4, A/D(25) 3, A/D(24) 2, A/D(23) 1, A/D(22) 84, A/D(21) 83, Vcc 82, Vss 81, A/D(20) 80, A/D(19) 79, A/D(18) 78, A/D(17) 77, A/D(16) 76, A/D(15) 75

Left pins (top to bottom):
Pin	Signal
12	Vss
13	Vcc
14	ClkIn
15	TriState
16	BE16(1)
17	BE16(0)
18	Addr(1)
19	Addr(0)
20	Int(5)
21	Vss
22	Vcc
23	Int(4)
24	Int(3)
25	SInt(2)
26	SInt(1)
27	SInt(0)
28	SBrCond(3)/ IOStrobe
29	SBrCond(2)/ ExtDataEn
30	TC
31	Vss
32	Vcc

Right pins (top to bottom):
Pin	Signal
74	Vss
73	Vcc
72	A/D(14)
71	A/D(13)
70	A/D(12)
69	A/D(11)
68	A/D(10)
67	A/D(9)
66	Vcc
65	Vss
64	A/D(8)
63	A/D(7)
62	A/D(6)
61	A/D(5)
60	A/D(4)
59	A/D(3)
58	Vss
57	Vcc
56	A/D(2)
55	A/D(1)
54	A/D(0)

Bottom pins (left to right, pins 33–53):
33 MemStrobe, 34 BusReq, 35 RdCEn, 36 Ack, 37 BusError, 38 Reset, 39 BusGnt, 40 SysClk, 41 Vss, 42 Vcc, 43 DataEn, 44 Wr, 45 Rd, 46 ALE, 47 Last, 48 Diag, 49 Vss, 50 Vcc, 51 Addr(2), 52 Addr(3), 53 Burst/WrNear

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**84-Pin PLCC/
Top View
(Cavity Down)**

PIN DESCRIPTION

PIN NAME	I/O	DESCRIPTION
A/D(31:0)	I/O	**Address/Data:** A 32-bit time multiplexed bus which indicates the desired address for a bus transaction in one phase, and which is used to transmit data between the CPU and external memory resources during the rest of the transfer. Bus transactions on this bus are logically separated into two phases: during the first phase, information about the transfer is presented to the memory system to be captured using the ALE output. This information consists of: **Address(31:4):** The high-order address for the transfer is presented on A/D(31:4). $\overline{BE(3:0)}$: These strobes indicate which bytes of the 32-bit bus will be involved in the transfer, and are presented on A/D(3:0). $\overline{BE(3)}$ indicates that A/D(31:24) will be used, and $\overline{BE(0)}$ corresponds to A/D(7:0). These strobes are only valid for accesses to 32-bit wide memory ports. Note that $\overline{BE(3:0)}$ can be held in-active during reads by setting the appropriate bit of CP0; thus when latched, these signals can be directly used as Write Enable strobes. During the second phase, these signals are the data bus for the transaction. **Data(31:0):** During write cycles, the bus contains the data to be stored and is driven from the internal write buffer. On read cycles, the bus receives the data from the external resource, in either a single data transaction or in a burst of four words, and places it into the on-chip read buffer. The byte lanes used during the transfer are a function of the datum size, the memory port width, and the system byte-ordering.
Addr(3:0)	O	**Low Address (3:0)** A 4-bit bus which indicates which word/halfword/byte is currently expected by the processor. For 32-bit port widths, only Addr(3:2) is valid during the transfer; for 16-bit port widths, only Addr(3:1) are valid; for 8-bit port widths, all of Addr(3:0) are valid. These address lines always contain the address of the current datum to be transferred. In writes and single datum reads, the addresses initially output the specific target address, and will increment if the size of the datum is wider than the target memory port. For quad word reads, these outputs function as a counter starting at '0000', and incrementing according to the width of the memory port.
	I[1]	During $\overline{Reset}$, the Addr(3:0) pins act as Reset Configuration Mode bit inputs for the $\overline{BootProm16}$, $\overline{BootProm8}$, ReservedHigh, and $\overline{ExtAddrHold}$ options. The R3041 Addr(1:0) output pins are designated as the unconnected Rsvd(1:0) pins in the R3051 and R3081.
Diag	O	**Diagnostic Pin.** This output indicates whether the current bus read transaction is due to an on-chip cache miss and whether the read is an instruction or data. It is time multiplexed as described below: **Cached/$\overline{Uncached}$:** During the phase in which the A/D bus presents address information, this pin is an active high output which indicates whether or not the current read is a result of a cache miss. The value of this pin at this time other than in read cycles is undefined. **I/$\overline{D}$:** A high at this time indicates an instruction reference, and a low indicates a data reference. The value of this pin at this time other than in read cycles is undefined. The R3041 Diag output pin is designated as the Diag(1) output pin in the R3051 and R3081.
ALE	O	**Address Latch Enable:** Used to indicate that the A/D bus contains valid address information for the bus transaction. This signal is used by external logic to capture the address for the transfer, typically by using transparent latches.
$\overline{DataEn}$	O	**Data Enable:** This signal indicates that the A/D bus is no longer being driven by the processor during read cycles, and thus the external memory system may enable the drivers of the memory system onto this bus without having a bus conflict occur. During write cycles, or when no bus transaction is occurring, this signal is negated, thus disabling the external memory drivers.

NOTE: 2905 tbl 03

1. Reset Configuration Mode bit input when $\overline{Reset}$ is asserted, normal signal
   function when $\overline{Reset}$ is de-asserted.

PIN DESCRIPTION (Continued):

PIN NAME	I/O	DESCRIPTION
Burst/ WrNear	O	**Burst Transfer/Write Near:** On read transactions, the Burst signal indicates that the current bus read is requesting a block of four contiguous words from memory. This signal is asserted only in read cycles due to cache misses; it is asserted for all I-Cache miss read cycles, and for D-Cache miss read cycles if the 4-word data block refill option is selected in the CP0 Cache Config Register. On write transactions, the WrNear output tells the external memory system that the bus interface unit is performing back-to-back write transactions to an address within the same 256 byte page as the prior write transaction. This signal is useful in memory systems which employ page mode or static column DRAMs, and allows nearby writes to be retired quickly.
Rd	O	**Read:** An output which indicates that the current bus transaction is a read.
Wr	O	**Write:** An output which indicates that the current bus transaction is a write.
Ack	I	**Acknowledge:** An input which indicates to the device that the memory system has sufficiently processed the bus transaction. On write transactions, this signal indicates that the CPU may either progress to the next data item (for mini-burst writes of wide datums to narrow memories), or terminate the write cycle. On read transactions, this signal indicates that the memory system has sufficiently processed the read, and that the processor core may begin processing the data from this read transfer.
RdCEn	I	**Read Buffer Clock Enable:** An input which indicates to the device that the memory system has placed valid data on the A/D bus, and that the processor may move the data into the on-chip Read Buffer.
SysClk	O	**System Reference Clock:** An output from the CPU which reflects the timing of the internal processor "System" clock. This clock is used to control state transitions in the read buffer, write buffer, memory controller, and bus interface unit.
BusReq	I	**DMA Arbiter Bus Request:** An input to the device which requests that the CPU tri-state its bus interface signals so that they may be driven by an external master. The negation of this input relinquishes mastership back to the CPU.
BusGnt	O	**DMA Arbiter Bus Grant.** An output from the CPU used to acknowledge that a BusReq has been detected, and that the bus is relinquished to the external master. The R3041 adds an additional DMA protocol, under the control of CP0. If the DMA Protocol is enabled, the R3041 can request that the external master relinquish bus mastership back to the processor by negating the BusGnt output early, and waiting for the BusReq input to be negated.
SBrCond(3)/ IOStrobe	I/O	**Branch Condition Port/IO Strobe:** The use of this signal depends on the setting of various bits of the CP0 Bus Control register. If BrCond mode is selected, this input is logically connected to CpCond(3), and can be used by the branch on co-processor condition instructions as an input port. The SBrCond(3) input has special internal logic to synchronize the input, and thus may be driven by asynchronous agents. If this pin is selected to function as IOStrobe, it may be asserted as an output on reads, writes, or both, as programmed into CP0. This strobe asserts in the second clock cycle of a transfer, and thus can be used to strobe various control signals on the bus interface.
SBrCond(2)/ ExtDataEn	I/O	**Branch Condition Port/Extended Data Enable:** The use of this signal depends on the settings in the CP0 Bus Control register. If BrCond mode is selected, this input is logically connected to CpCond(2), and can be used by the branch on co-processor condition instructions as an input port. The SBrCond(2) input has special internal logic to synchronize the input, and thus may be driven by asynchronous agents. If this pin is selected to function as Extended Data Enable, it may be asserted as an output on reads, writes, or both, as programmed into CP0. This strobe can be used as an extended data enable strobe, in that it is held asserted for one-half clock cycle after the negation of Rd or Wr. This signal may typically be used as a write enable control line for transceivers, as a write line for I/O, or as an address mux select for DRAMs.
MemStrobe	O	**Memory Strobe:** This active low output pulses low for each data read or written, as configured in the CP0 Bus Control register. Thus, it can be used as a read strobe, write strobe, or both, for SRAM type memories or for I/O devices. The R3041 MemStrobe output pin is designated as the BrCond(0) input pin in the R3051 and R3081.

2905 tbl 04

PIN DESCRIPTION (Continued):

PIN NAME	I/O	DESCRIPTION
$\overline{BE16(1:0)}$	O	**Byte Enable Strobes for 16-bit Memory Port:** These active low outputs are the byte lane strobes for accesses to 16-bit wide memory ports; they are not necessarily valid for 8- or 32-bit wide ports. If $\overline{BE16(1)}$ is asserted, then the most significant byte (either D(31:24) or D(15:8), depending on system endianness) is going to be used in this transfer. If $\overline{BE16(0)}$ is asserted, the least significant byte (D(23:16) or D(7:0)) will be used. $\overline{BE16(1:0)}$ can be held inactive (masked) during read transfers, according to the programming of the CP0 Bus Control register.
	I[1]	During $\overline{Reset}$, the $\overline{BE16(1:0)}$ act as Reset Configuration Mode bit inputs for two ReservedHigh options. The $\overline{BE16(1:0)}$ output pins are designated as the unconnected Rsvd(3:2) pins in the R3051 and R3081.
$\overline{Last}$	O	**Last Datum in Mini-Burst:** This active low output indicates that this is the last datum transfer in a given transaction. It is asserted after the next to last $\overline{RdCEn}$ (reads) or $\overline{Ack}$ (writes), and is negated when $\overline{Rd}$ or $\overline{Wr}$ is negated. The $\overline{Last}$ output pin is designated in the R3051 and R3081 as the Diag(0) output pin.
$\overline{TC}$	O	**Terminal Count:** This is an active low output from the processor which indicates that the on-chip timer has reached its terminal count. It will remain low for either 1.5 clock cycles, or until software resets the timer, depending on the mode selected in the CP0 Bus Control register. Thus, the on-chip timer can function either as a free running timer for system functions such as DRAM refresh, or can operate as a software controlled time-slice timer, or real-time clock. The $\overline{TC}$ output pin is designated in the R3051 as the BrCond(1) input pin, and in the R3081 as the Run pin output.
$\overline{BusError}$	I	**Bus Error:** Input to the bus interface unit to terminate a bus transaction due to an external bus error. This signal is only sampled during read and write operations. If the bus transaction is a read operation, then the CPU will take a bus error exception.
$\overline{Int(5:3)}$ $\overline{SInt(2:0)}$	I	**Processor Interrupt:** During normal operation, these signals are logically the same as the $\overline{Int(5:0)}$ signals of the R3000A. During processor reset, these signals perform mode initialization of the CPU, but in a different (simpler) fashion than the interrupt signals on the original R3000A.
	I[1]	During $\overline{Reset}$, $\overline{Int(3)}$ and $\overline{SInt(0)}$ act as Reset Configuration Mode bit inputs for the AddrDisplayAndForceCacheMiss and BigEndian options. There are two types of interrupt inputs: the $\overline{SInt}$ inputs are internally synchronized by the processor, and may be driven by an asynchronous external agent. The direct interrupt inputs are not internally synchronized, and thus must be externally synchronized to the CPU. The direct interrupt inputs have one cycle lower latency than the synchronized interrupts.
ClkIn	I	**Master Clock Input:** This is a double frequency input used to control the timing of the CPU.
$\overline{Reset}$	I	**Master Processor Reset:** This signal initializes the CPU. Reset initialization mode selection is performed during the last cycle of $\overline{Reset}$.
$\overline{TriState}$	I	**Tri-State:** This input to the R3041 requests that the R3041 tri-state all of its outputs. In addition to those outputs tri-stated during DMA, tri-state will cause $\overline{SysClk}$, $\overline{TC}$, and $\overline{BusGnt}$ to tri-state. This signal is intended for use during board testing and emulation during debug and board manufacture. The $\overline{TriState}$ input pin is designated as the unconnected Rsvd(4)pin in the R3051 and R3081.
Vcc	I	**Power:** These inputs must be supplied with the rated supply voltage (VCC). All Vcc inputs must be connected to insure proper operation.
Vss	I	**Ground:** These inputs must be connected to ground (GND). All Vss inputs must be connected to insure proper operation.

2905 tbl 05

NOTE:
1. Reset Configuration Mode bit input when $\overline{Reset}$ is asserted, normal signal function when $\overline{Reset}$ is de-asserted.

AC ELECTRICAL CHARACTERISTICS RV3041 (CONT.)

Symbol	Signals	Description	16.67 MHz Min.	16.67 MHz Max.	20 MHz Min.	20 MHz Max.	25MHz Min.	25MHz Max.	33MHz Min.	33MHz Max.	Unit
t18	A/D	Tri-state from $\overline{\text{SysClk}}$	—	13	—	10	—	10	—	10	ns
t19	A/D	$\overline{\text{SysClk}}$ to data out	—	16	—	13	—	12	—	12	ns
t20	ClkIn	Pulse Width High	12	—	10	—	8	—	6.5	—	ns
t21	ClkIn	Pulse Width Low	12	—	10	—	8	—	6.5	—	ns
t22	ClkIn	Clock Period	30	250	25	250	20	250	15	250	ns
t23	$\overline{\text{Reset}}$	Pulse Width from Vcc valid	200	—	200	—	200	—	200	—	µs
t24	$\overline{\text{Reset}}$	Minimum Pulse Width	32	—	32	—	32	—	32	—	sys
t25	$\overline{\text{Reset}}$	Set-up to $\overline{\text{SysClk}}$ falling	8	—	6	—	5	—	5	—	ns
t26	$\overline{\text{Int}}$	Mode set-up to $\overline{\text{Reset}}$ rising	8	—	6	—	5	—	5	—	ns
t27	$\overline{\text{Int}}$	Mode hold from $\overline{\text{Reset}}$ rising	2.5	—	2.5	—	2.5	—	2.5	—	ns
t28	$\overline{\text{SInt}}$, SBrCond	Set-up to $\overline{\text{SysClk}}$ falling	8	—	6	—	5	—	5	—	ns
t29	$\overline{\text{SInt}}$, SBrCond	Hold from $\overline{\text{SysClk}}$ falling	4	—	3	—	3	—	3	—	ns
t30	$\overline{\text{Int}}$, BrCond	Set-up to $\overline{\text{SysClk}}$ falling	8	—	6	—	5	—	5	—	ns
t31	$\overline{\text{Int}}$, BrCond	Hold from $\overline{\text{SysClk}}$ falling	4	—	3	—	3	—	3	—	ns
tsys	$\overline{\text{SysClk}}$	Pulse Width	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	ns
t32	$\overline{\text{SysClk}}$	Clock High Time	t22 - 2	t22 + 2	t22 - 2	t22 + 2	t22 - 2	t22 + 2	t22 - 2	t22 + 2	ns
t33	$\overline{\text{SysClk}}$	Clock Low Time	t22 - 2	t22 + 2	t22 - 2	t22 + 2	t22 - 2	t22 + 2	t22 - 2	t22 + 2	ns
t45	$\overline{\text{ExtDataEn}}$	Tri-state from $\overline{\text{SysClk}}$ rising (after driven condition)	—	13	—	10	—	10	—	10	ns
t46	$\overline{\text{ExtDataEn}}$	Driven from $\overline{\text{SysClk}}$ falling (after driven condition)	—	13	—	10	—	10	—	10	ns
t47	$\overline{\text{IOStrobe}}$	Valid from $\overline{\text{SysClk}}$ falling	—	10	—	8	—	7	—	7	ns
t48	$\overline{\text{ExtDataEn}}$,	Asserted from $\overline{\text{SysClk}}$ rising	—	15	—	12	—	9	—	9	ns
t49	$\overline{\text{ExtDataEn}}$ $\overline{\text{DataEn}}$	Negated from $\overline{\text{SysClk}}$ rising	—	9	—	7	—	6	—	6	ns
t50	$\overline{\text{MemStrobe}}$	Asserted from $\overline{\text{SysClk}}$ rising	—	19	—	15	—	15	—	15	ns
t51	$\overline{\text{MemStrobe}}$	Negated from $\overline{\text{SysClk}}$ falling	—	19	—	15	—	15	—	15	ns
t52	$\overline{\text{MemStrobe}}$	Asserted from Addr(3:0) valid[4]	0	—	0	—	0	—	0	—	ns
tderate	All outputs	Timing deration for loading over 25pF[4, 5]	—	0.5	—	0.5	—	0.5	—	0.5	ns/ 25pF

2905 tbl 12

NOTES:
1. All timings referenced to 1.5 Volts, with a rise and fall time of less than 2.5ns.
2. All outputs tested with 25pF loading.
3. The AC values listed here reference timing diagrams contained in the R3041 Hardware User's Manual.
4. Guaranteed by design.
5. This parameter is used to derate the AC timings according to the loading of the system. This parameter provides a deration for loads over the specified test condition; that is, the deration factor is applied for each 25pF over the specified test load condition.
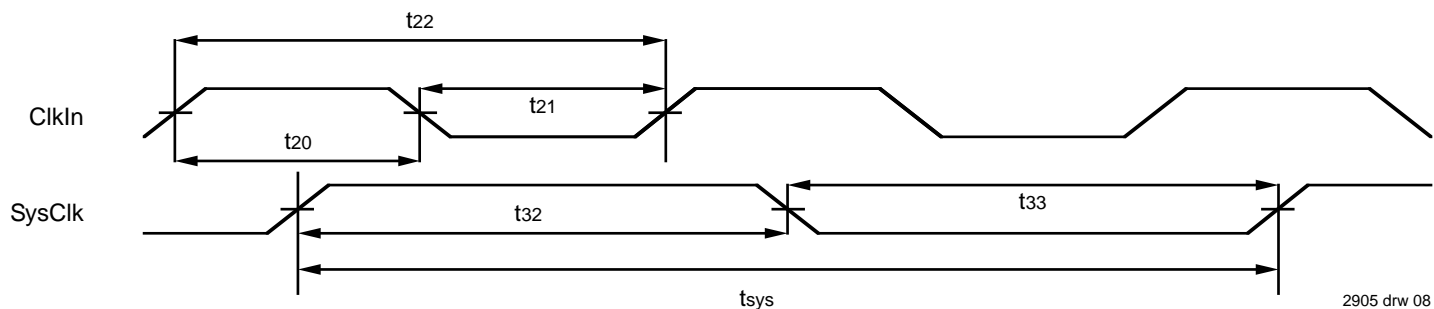6. Timings t34 - t44 are reserved for other RISController family members.

2905 drw 08
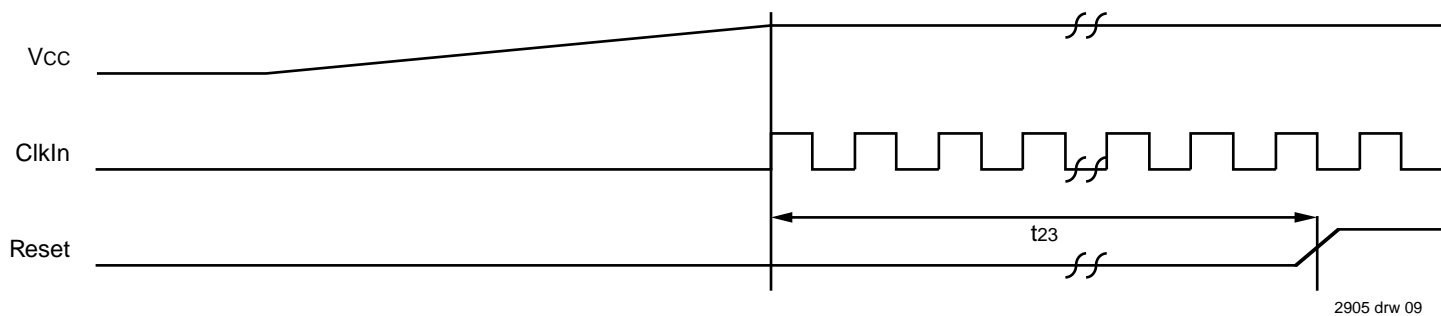
Figure 8. RISController Family Clocking

2905 drw 09

Figure 9. Power-On Reset Sequence

2905 drw 10
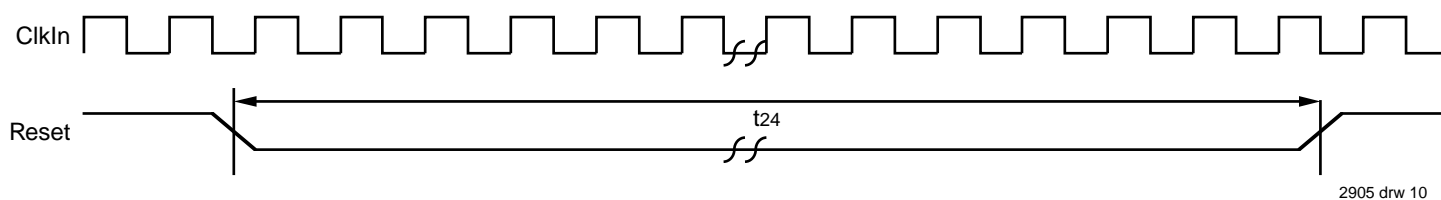
Figure 10(a). Warm Reset Sequence
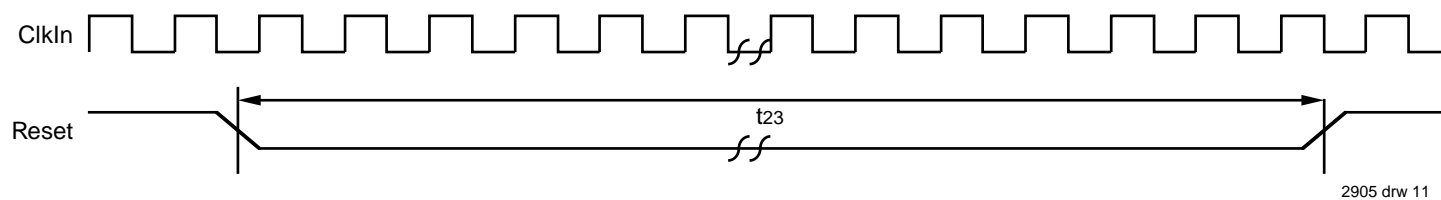

2905 drw 11

Figure 10(b). Warm Reset Sequence (Internal Pull-Ups Used)
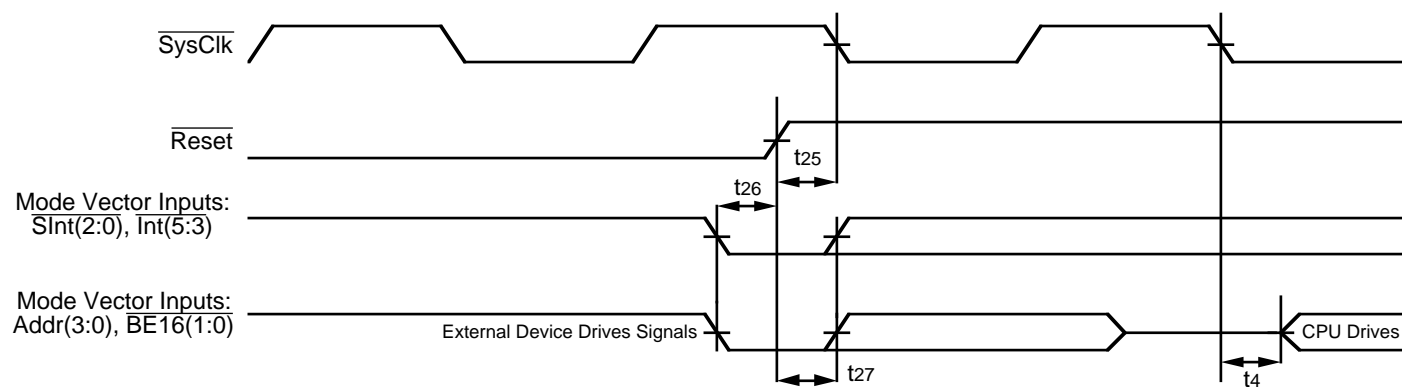

2905 drw 12

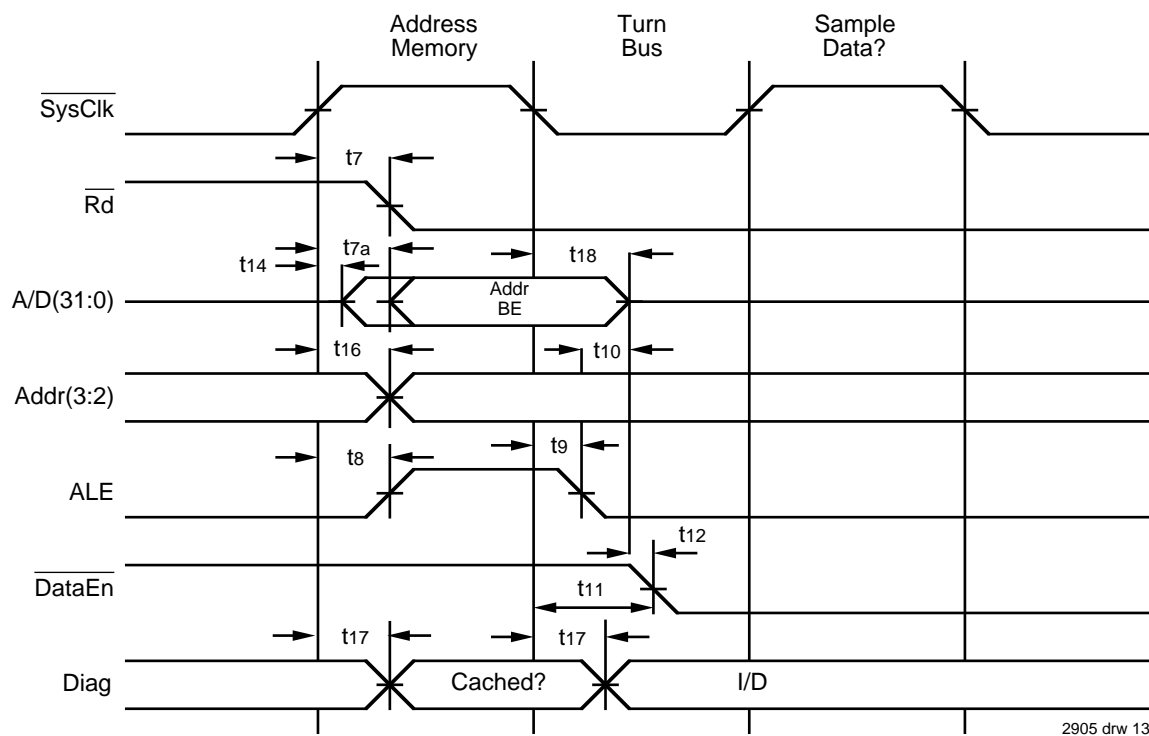**Figure 11. Mode Selection and Negation of Reset**

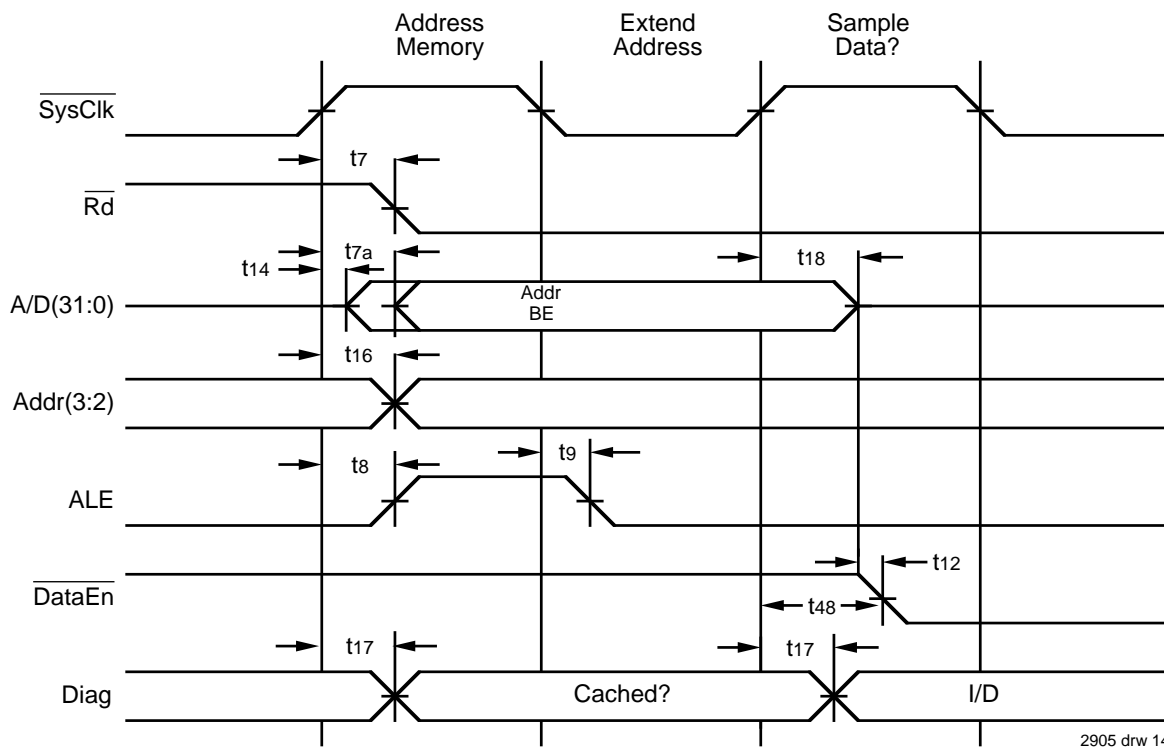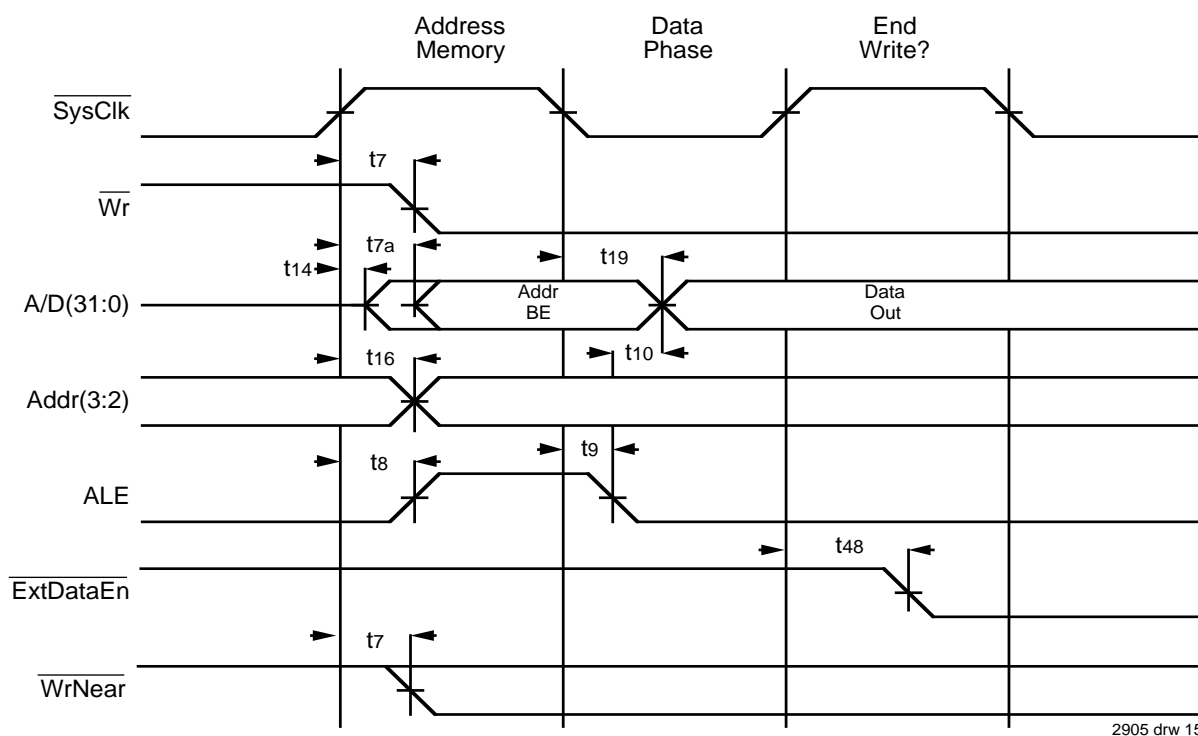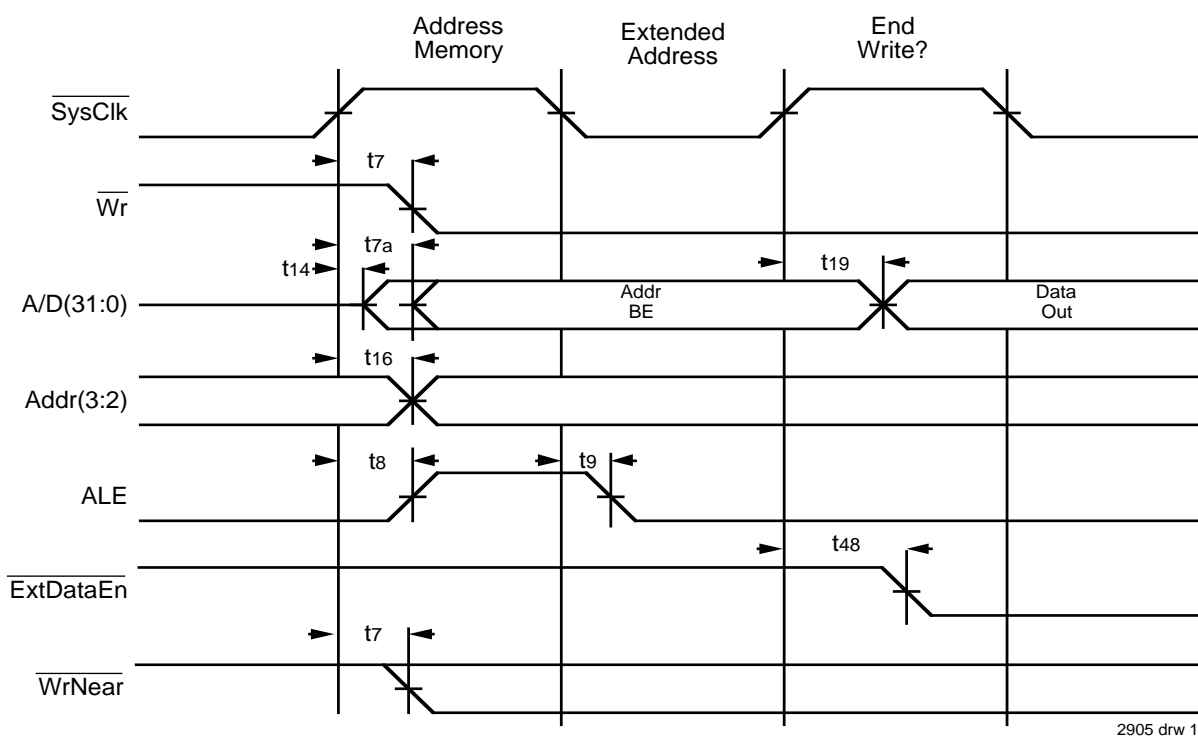**Figure 12(a). Start of Read Timing with Non-Extended Address Hold Option**

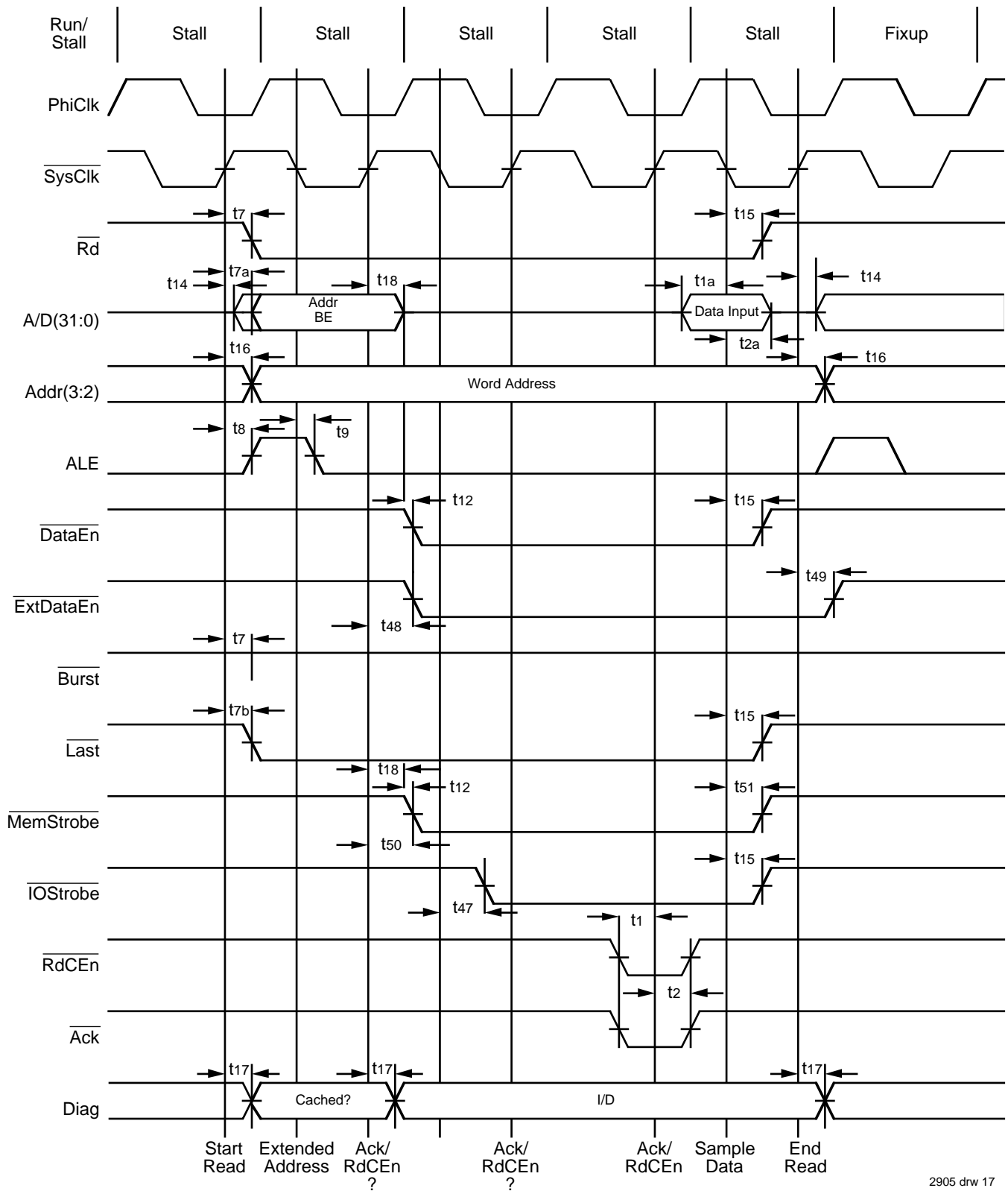**Figure 12(b). Start of Read Timing with Extended Address Hold Option**

Figure 12(c). Start of Write Timing with Non-Extended Address Hold Option

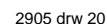**Figure 12(d). Start of Write Timing with Extended Address Hold Option**

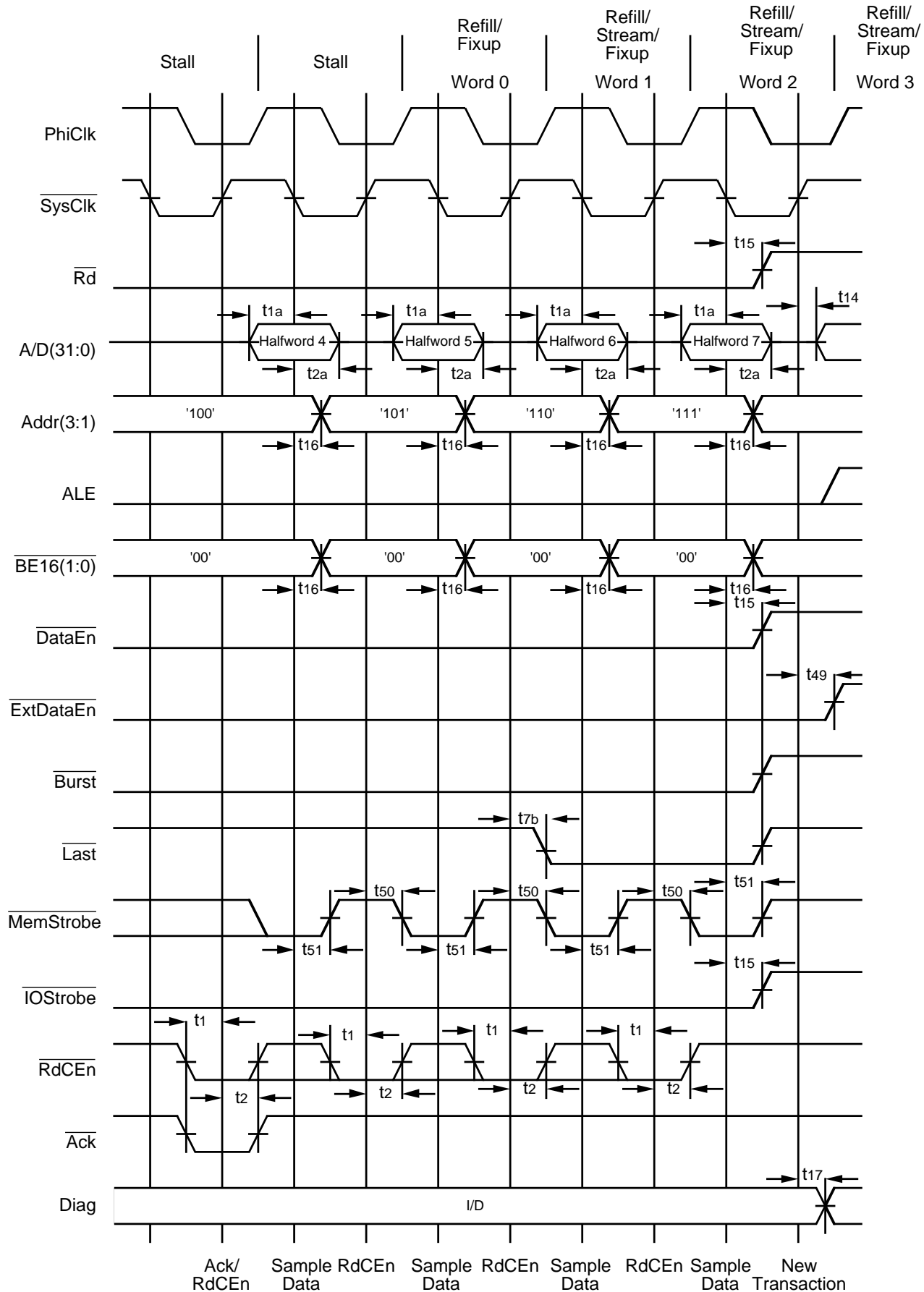**Figure 13. Single Datum Read**
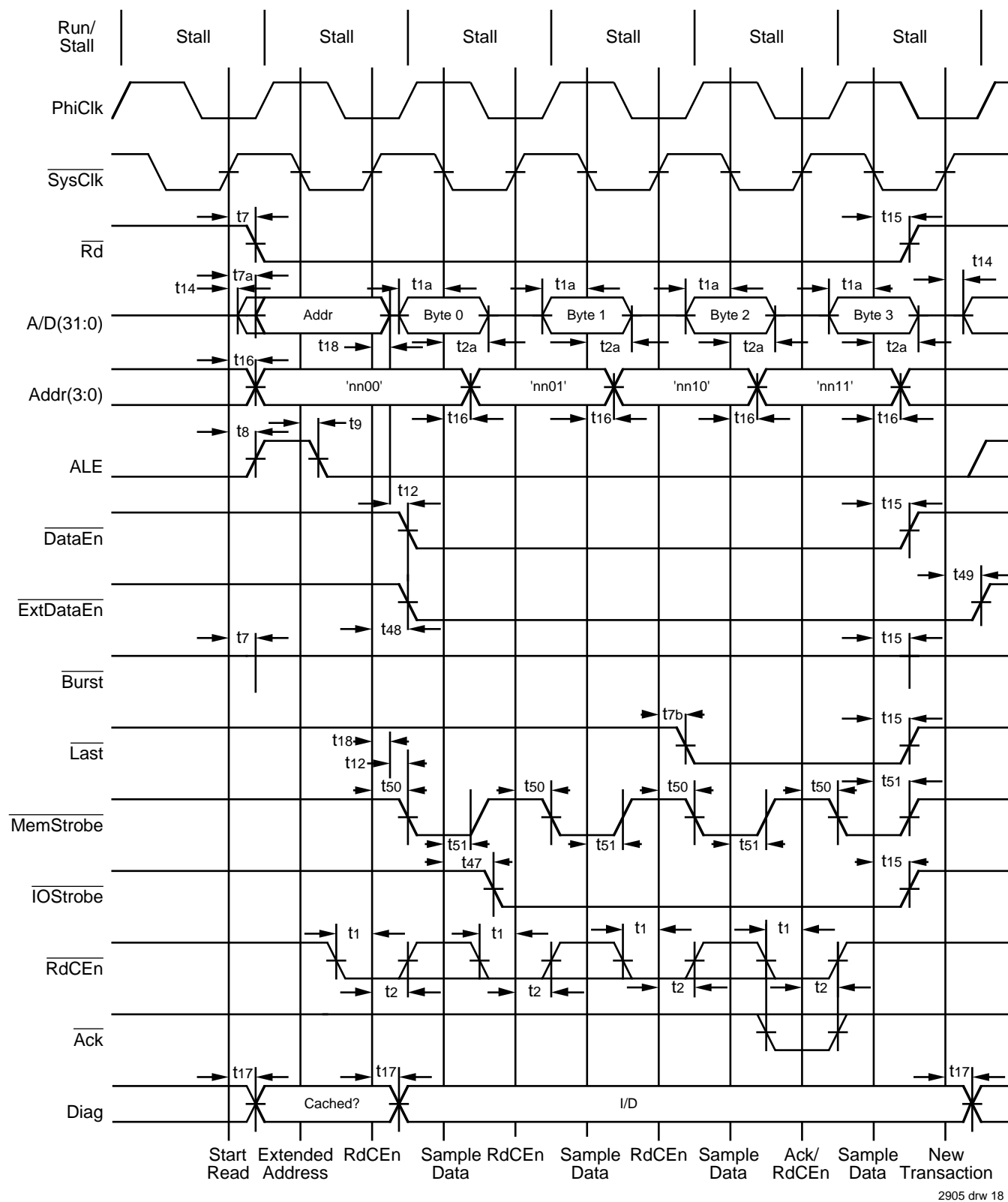
Figure 14. Mini-burst read of 32-bit datum from 8-bit wide memory port
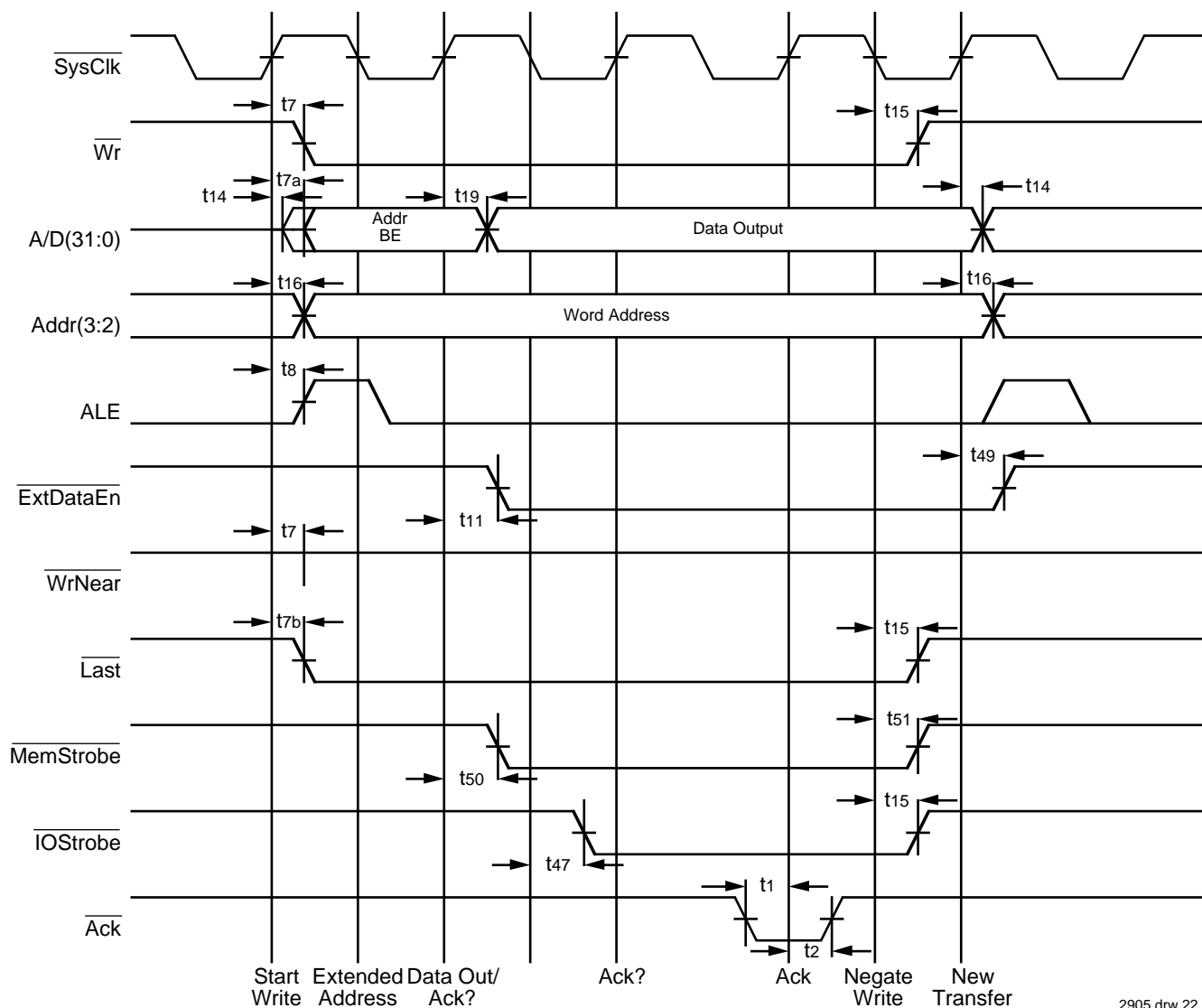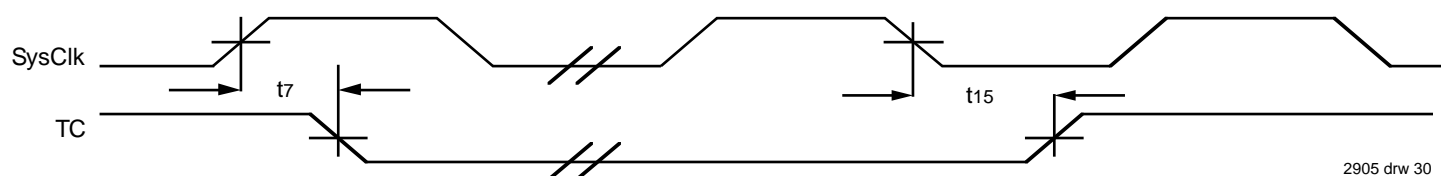
Figure 16(a). Quad Word Read to 16-bit wide Memory Port

2905 drw 20

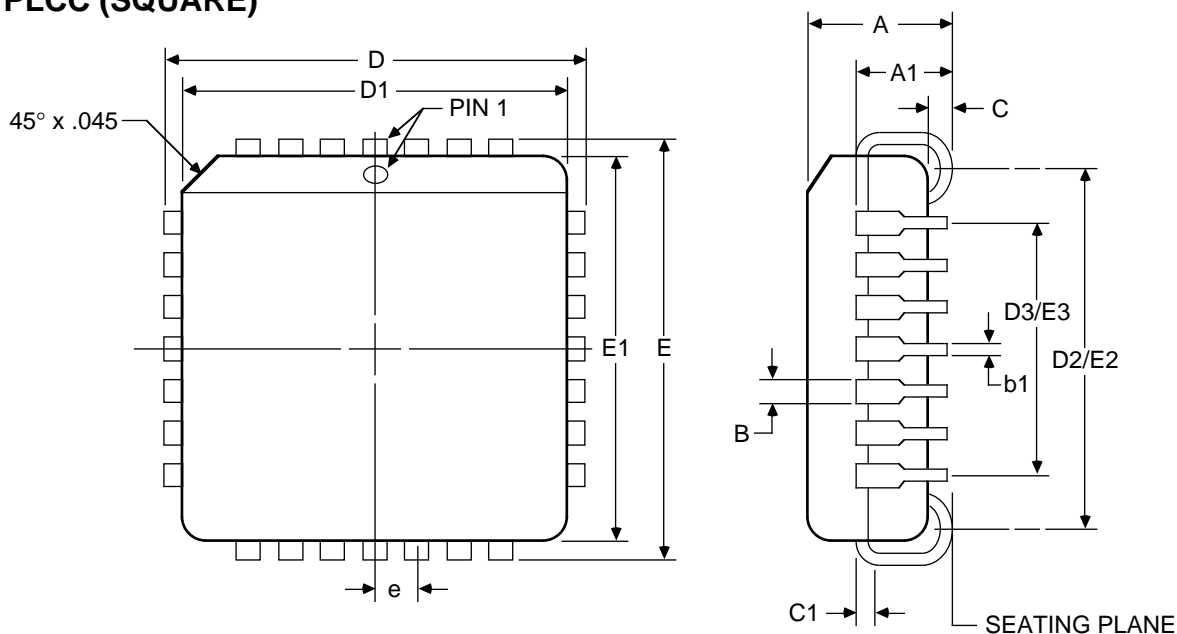**Figure 16(b). End of Quad Word read from 16-bit Wide Memory Port**

2905 drw 21

Figure 17. Basic Write to 32-bit Memory Port

2905 drw 22

2905 drw 30

Figure 25. $\overline{TC}$ Output

84 LEAD PLCC (SQUARE)

2905 drw 31

DWG #	J84-1	
# of Leads	84	
Symbol	Min.	Max.
A	165	.180
A1	.095	.115
B	.026	.032
b1	.013	.021
C	.020	.040
C1	.008	.012
D	1.185	1.195
D1	1.150	1.156
D2/E2	1.090	1.130
D3/E3	1.000 REF	
E	1.185	1.195
E1	1.150	1.156
e	.050 BSC	
ND/NE	21	

2905 tbl 13

NOTES:
1. All dimensions are in inches, unless otherwise noted.
2. BSC—Basic lead Spacing between Centers.
3. D & E do not include mold flash or protrutions.
4. Formed leads shall be planar with respect to one another and within .004" at the seating plane.
5. ND & NE represent the number of leads in the D & E directions respectively.
6. D1 & E1 should be measured from the bottom of the package.
7. PLCC is pin & form compatible with MQUAD; the MQUAD package is used in other RISController family members.

ORDERING INFORMATION

```
XXXXX    —    XX      X         X
```
Device Type   Speed   Package   Process/
                                 Temp. Range

Blank	Commercial Temperature Range
'J'	84-Pin PLCC
'PF'	100-Pin TQFP
'16'	16.67MHz
'20'	20.00MHz
'25'	25.00MHz
'33'	33.00MHz
79R3041	5.0V Integrated RISController for Low-Cost Systems
79RV3041	3.3V Integrated RISController for Low-Cost Systems
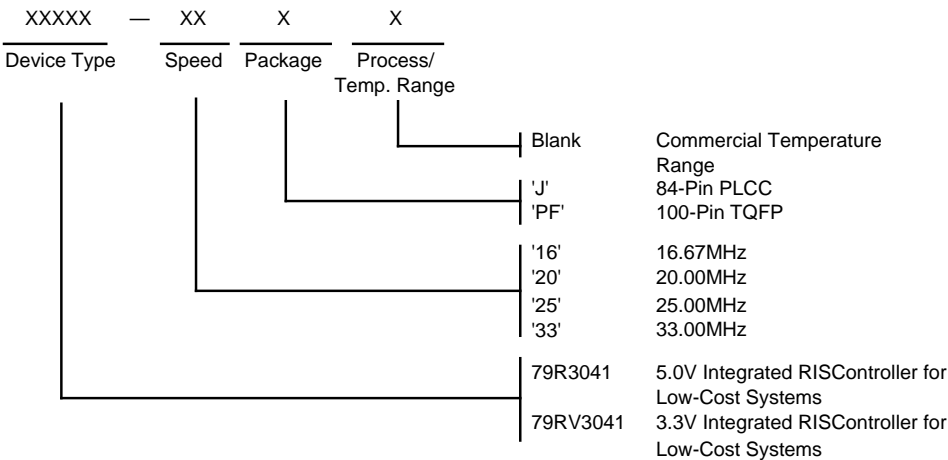
2905 drw 32

VALID COMBINATIONS

79R3041 - 16	TQFP, PLCC Package
79R3041 - 20	TQFP, PLCC Package
79R3041 - 25	TQFP, PLCC Package
79R3041 - 33	PLCC Package Only
79RV3041 - 16	TQFP, PLCC Package
79RV3041 - 20	TQFP, PLCC Package
79RV3041 - 25	TQFP, PLCC Package
79RV3041 - 33	TQFP, PLCC Package