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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MIPS-I
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	20MHz
Co-Processors/DSP	System Control; CP0
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 85°C (TC)
Security Features	-
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/idt79r3041-20pfg8

Clock Generation Unit

The R3041 is driven from a single 2x frequency input clock, capable of operating in a range of 40%-60% duty cycle. On-chip, the clock generator unit is responsible for managing the interaction of the CPU core, caches, and bus interface. The clock generator unit replaces the external delay line required in R3000A based applications.

Instruction Cache

The R3041 integrates 2kB of on-chip Instruction Cache, organized with a line size of 16 bytes (four 32-bit entries) a nd is direct mapped. This relatively large cache substantially contributes to the performance inherent in the R3041, and allows systems based on the R3041 to achieve high-performance even from low-cost memory systems. The cache is implemented as a direct mapped cache, and is capable of caching instructions from anywhere within the 4GB physical address space. The cache is implemented using physical addresses and physical tags (rather than virtual addresses or tags), and thus does not require flushing on context switch.

Data Cache

The R3041 incorporates an on-chip data cache of 512B, organized as a line size of 4 bytes (one word) and is direct mapped. This relatively large data cache contributes substantially to the performance inherent in the RISController family. As with the instruction cache, the data cache is implemented as a direct mapped physical address cache. The cache is capable of mapping any word within the 4GB physical address space.

The data cache is implemented as a write through cache, to insure that main memory is always consistent with the internal cache. In order to minimize processor stalls due to data write operations, the bus interface unit incorporates a 4-deep write buffer which captures address and data at the processor execution rate, allowing it to be retired to main memory at a much slower rate without impacting system performance.

Bus Interface Unit

The RISController family uses its large internal caches to provide the majority of the bandwidth requirements of the execution engine, and thus can utilize a simple bus interface connected to slow memory devices.

The RISController family bus interface utilizes a 32-bit address and data bus multiplexed onto a single set of pins. The bus interface unit also provides an ALE (Address Latch Enable) output signal to de-multiplex the A/D bus, and simple handshake signals to process CPU read and write requests. In addition to the read and write interface, the R3041 incorporates a DMA arbiter, to allow an external master to control the external bus.

The R3041 augments the basic RISController bus interface capability by adding the ability to directly interface with varying memory port widths, for instructions or data. For example, the R3041 can be used in a system with an 8-bit boot PROM, 16-bit font/program cartridges, and 32-bit main memory, transparently to software, and without requiring external data packing, rotation, and unpacking.

In addition, the R3041 incorporates the ability to change some of the interface timing of the bus. These features can be used to eliminate external data buffers and take advantage of lower speed and lower cost interface components.

One of the bus interface options is the Extended Address Hold mode which adds 1/2 clock of extra address hold time from ALE falling. This allows easier interfacing to FPGAs and ASICs.

The R3041 incorporates a 4-deep write buffer to decouple the speed of the execution engine from the speed of the memory system. The write buffers capture and FIFO processor address and data information in store operations, and present it to the bus interface as write transactions at the rate the memory system can accommodate. During main memory writes, the R3041 can break a large datum (e.g. 32-bit word) into a series of smaller transactions (e.g. bytes), according to the width of the memory port being written. This operation is transparent to the software which initiated the store, insuring that the same software can run in true 32-bit memory systems.

The RISController family read interface performs both single word reads and quad word reads. Single word reads work with a simple handshake, and quad word reads can either utilize the simple handshake (in lower performance, simple systems) or utilize a tighter timing mode when the memory system can burst data at the processor clock rate. Thus, the system designer can choose to use page or static column mode DRAMs (and possibly use interleaving, if desired, in high-performance systems), or even to use simpler SRAM techniques to reduce complexity.

In order to accommodate slower quad word reads, the RISController family incorporates a 4-deep read buffer FIFO, so that the external interface can queue up data within the processor before releasing it to perform a burst fill of the internal caches.

In addition, the R3041 can perform on-chip data packing when performing large datum reads (e.g., quad words) from narrower memory systems (e.g., 16-bits). Once again, this operation is transparent to the actual software, simplifying migration of software to higher performance (true 32-bit) systems, and simplifying field upgrades to wider memory. Since this capability works for either instruction or data reads, using 8-, 16-, or 32-bit boot PROMs is easily supported by the

DEVELOPMENT SUPPORT

The IDT RISController family is supported by a rich set of development tools, ranging from system simulation tools through PROM monitor and debug support, applications software and utility libraries, logic analysis tools, and sub-system modules.

Figure 5 is an overview of the system development process typically used when developing R3041 applications. The RISController family is supported in all phases of project development. These tools allow timely, parallel development of hardware and software for RISController family based applications, and include tools such as:

- Optimizing compilers from MIPS Technology, the acknowledged leader in optimizing compiler technology.
- Cross development tools, available in a variety of development environments.
- The high-performance IDT floating point emulation library software.
- The IDT Evaluation Board, which includes RAM, EPROM, I/O, and the IDT PROM Monitor.
- IDT Laser Printer System boards, which directly drive a low-cost print engine, and runs Adobe PostScript™ Page Description Language
- Adobe PostScript Page Description Language running on the IDT RISController family.
- The IDT/sim™ PROM Monitor, which implements a full PROM monitor (diagnostics, remote debug support, peek/

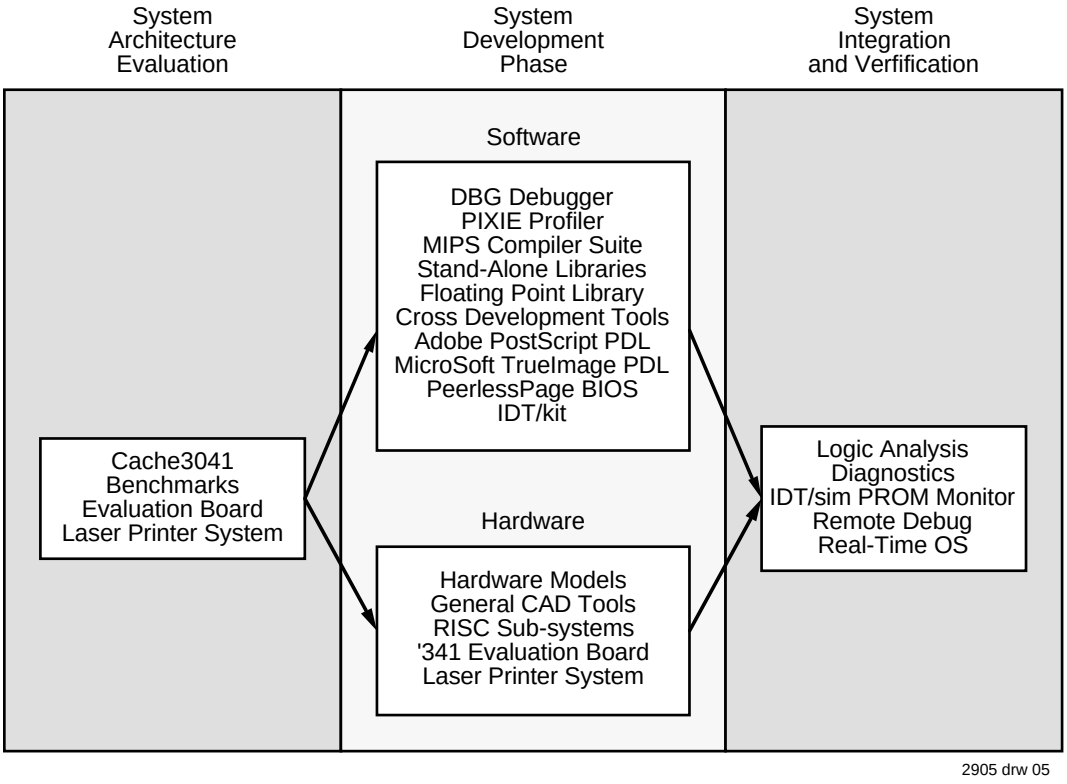


Figure 5. R3041 Development Environment

poke, etc.).
- IDT/kit™ (Kernel Integration Toolkit), providing library support and a frame work for the system run time environment.

PERFORMANCE OVERVIEW

The RISController family achieves a very high-level of performance. This performance is based on:

- **An efficient execution engine:** The CPU performs ALU operations and store operations in a single cycle, and has an effective load time of 1.3 cycles, and branch execution rate of 1.5 cycles (based on the ability of the compilers to avoid software interlocks). Thus, the R3041 achieves 20 MIPS performance at 25MHz when operating out of cache.
- **Large on-chip caches:** The RISController family contains caches which are substantially larger than those on the majority of embedded microprocessors. These large caches minimize the number of bus transactions required, and allow the RISController family to achieve actual sustained performance very close to its peak execution rate, even with low-cost memory systems.
- **Autonomous multiply and divide operations:** The RISController family features an on-chip integer multiplier/divide unit which is separate from the other ALU. This allows the R3041 to perform multiply or divide operations in parallel with other integer operations, using a single multiply or divide instruction rather than using “step” operations.
- **Integrated write buffer:** The R3041 features a four deep write buffer, which captures store target addresses and data at the processor execution rate and retires it to main memory at the slower main memory access rate. Use of on-chip write buffers eliminates the need for the processor to stall when performing store operations.
- **Burst read support:** The R3041 enables the system designer to utilize page mode, static column, or nibble mode RAMs when performing read operations to minimize the main memory read penalty and increase the effective cache hit rates.

The performance differences among the various RISController family members depends on the application software and the design of the memory system. Different family members feature different cache sizes, and the R3081 features a hardware floating point accelerator. Since all these devices can be used in a pin and software compatible fashion, the system designer has maximum freedom in trading between performance and cost. The memory simulation tools (e.g. Cache3041) allows the system designers to analyze and understand the performance differences among these devices in their application.

SELECTABLE FEATURES

The RISController family uses two methods to allow the system designer to configure bus interface operation options.

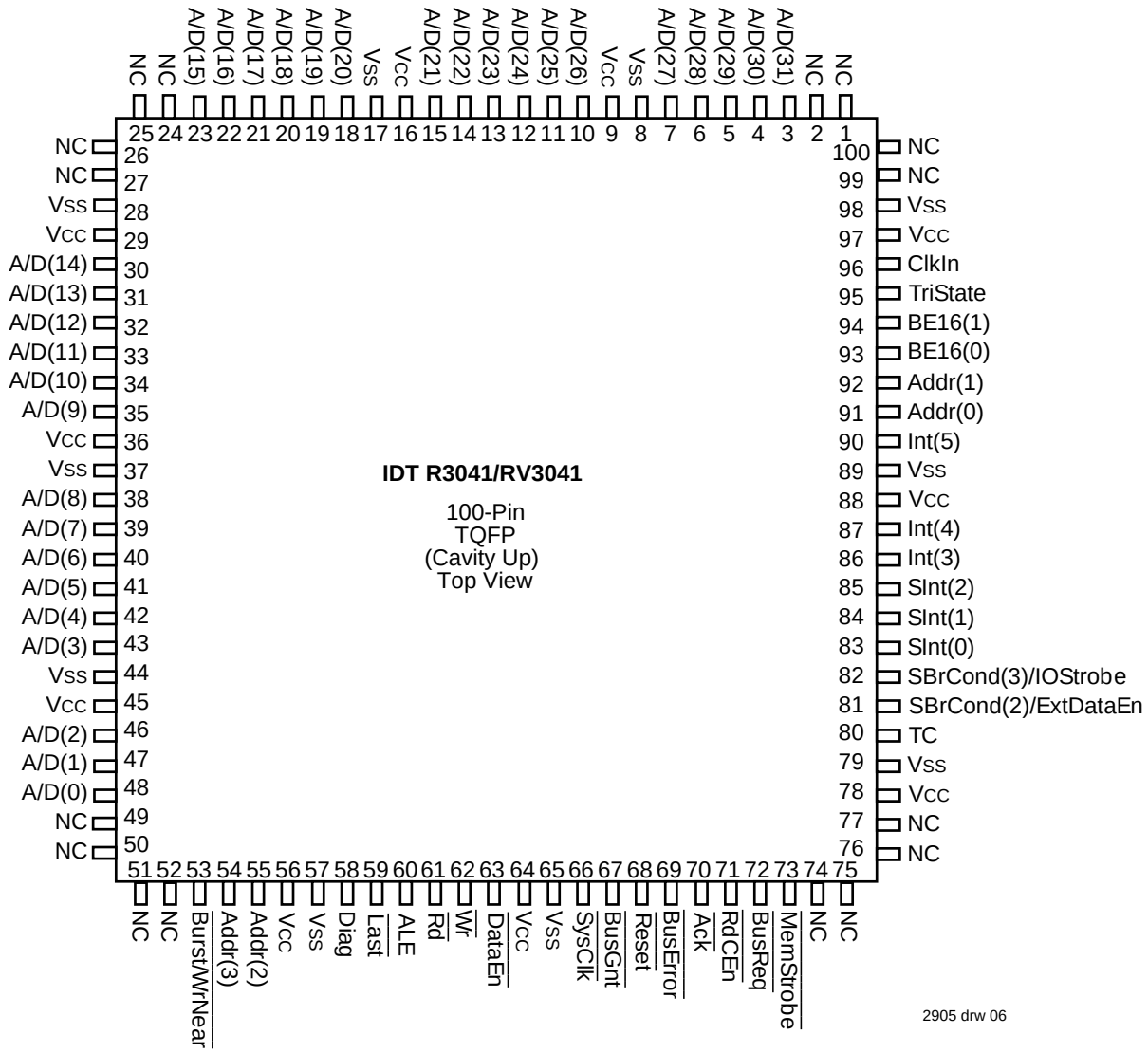
The first set of options are established via the Reset Configuration Mode inputs, sampled during the device reset. After reset, the Reset Mode inputs become regular input or output signals.

The second set of configuration options are contained in the System Control Co-Processor registers. These Co-processor registers configuration options are typically initialized with the boot PROM and can also be changed dynamically by the kernel software.

Selectable features include:

- **Big Endian vs. Little Endian operation**: The part can be configured to operate with either byte ordering convention, and in fact may also be dynamically switched between the two conventions. This facilitates the porting of applications from other processor architectures, and also permits intercommunication between various types of processors and databases.
- **Data Cache Refill of one or four words**: The memory system must be capable of performing 4 word transfers to satisfy instruction cache misses and 1 word transfers to satisfy uncached references. The data cache refill size option allows the system designers to choose between one and four word refill on data cache misses, depending on the performance each option brings to their application.
- **Bus Turn Around speed**: The R3041 allows the kernel to increase the amount of time between bus transactions when changes in direction of the A/D bus occur (e.g., at the end of reads followed by writes). This allows transceivers and buffers to be eliminated from the system.
- **Extended Address Hold Time**: The R3041 allows the system designer to increase the amount of hold time available for address latching, thus allowing slower speed (low cost) address latches, FPGAs and ASICs to be used.
- **Programmable control signals**: The R3041 allows the system designer to optimally configure various memory control signals to be active on reads only, writes only, or on both reads and writes. This allows the simplification of external logic, thus reducing system cost.

PIN CONFIGURATIONS



2905 drw 06

PIN DESCRIPTION (Continued):

PIN NAME	I/O	DESCRIPTION
$\overline{BE16(1:0)}$	O	**Byte Enable Strobes for 16-bit Memory Port:** These active low outputs are the byte lane strobes for accesses to 16-bit wide memory ports; they are not necessarily valid for 8- or 32-bit wide ports. If $\overline{BE16(1)}$ is asserted, then the most significant byte (either D(31:24) or D(15:8), depending on system endianness) is going to be used in this transfer. If $\overline{BE16(0)}$ is asserted, the least significant byte (D(23:16) or D(7:0)) will be used. $\overline{BE16(1:0)}$ can be held inactive (masked) during read transfers, according to the programming of the CP0 Bus Control register.
	I(1)	During $\overline{Reset}$, the $\overline{BE16(1:0)}$ act as Reset Configuration Mode bit inputs for two ReservedHigh options. The $\overline{BE16(1:0)}$ output pins are designated as the unconnected Rsvd(3:2) pins in the R3051 and R3081.
$\overline{Last}$	O	**Last Datum in Mini-Burst:** This active low output indicates that this is the last datum transfer in a given transaction. It is asserted after the next to last $\overline{RdCEn}$ (reads) or $\overline{Ack}$ (writes), and is negated when $\overline{Rd}$ or $\overline{Wr}$ is negated. The $\overline{Last}$ output pin is designated in the R3051 and R3081 as the Diag(0) output pin.
$\overline{TC}$	O	**Terminal Count:** This is an active low output from the processor which indicates that the on-chip timer has reached its terminal count. It will remain low for either 1.5 clock cycles, or until software resets the timer, depending on the mode selected in the CP0 Bus Control register. Thus, the on-chip timer can function either as a free running timer for system functions such as DRAM refresh, or can operate as a software controlled time-slice timer, or real-time clock. The $\overline{TC}$ output pin is designated in the R3051 as the BrCond(1) input pin, and in the R3081 as the Run pin output.
$\overline{BusError}$	I	**Bus Error:** Input to the bus interface unit to terminate a bus transaction due to an external bus error. This signal is only sampled during read and write operations. If the bus transaction is a read operation, then the CPU will take a bus error exception.
$\overline{Int(5:3)}$ $\overline{SInt(2:0)}$	I	**Processor Interrupt:** During normal operation, these signals are logically the same as the $\overline{Int}$(5:0) signals of the R3000A. During processor reset, these signals perform mode initialization of the CPU, but in a different (simpler) fashion than the interrupt signals on the original R3000A.
	I(1)	During $\overline{Reset}$, $\overline{Int(3)}$ and $\overline{SInt(0)}$ act as Reset Configuration Mode bit inputs for the AddrDisplayAndForceCacheMiss and BigEndian options. There are two types of interrupt inputs: the $\overline{SInt}$ inputs are internally synchronized by the processor, and may be driven by an asynchronous external agent. The direct interrupt inputs are not internally synchronized, and thus must be externally synchronized to the CPU. The direct interrupt inputs have one cycle lower latency than the synchronized interrupts.
ClkIn	I	**Master Clock Input:** This is a double frequency input used to control the timing of the CPU.
$\overline{Reset}$	I	**Master Processor Reset:** This signal initializes the CPU. Reset initialization mode selection is performed during the last cycle of $\overline{Reset}$.
$\overline{TriState}$	I	**Tri-State:** This input to the R3041 requests that the R3041 tri-state all of its outputs. In addition to those outputs tri-stated during DMA, tri-state will cause $\overline{SysClk}$, $\overline{TC}$, and $\overline{BusGnt}$ to tri-state. This signal is intended for use during board testing and emulation during debug and board manufacture. The $\overline{TriState}$ input pin is designated as the unconnected Rsvd(4)pin in the R3051 and R3081.
Vcc	I	**Power:** These inputs must be supplied with the rated supply voltage (VCC). All Vcc inputs must be connected to insure proper operation.
Vss	I	**Ground:** These inputs must be connected to ground (GND). All Vss inputs must be connected to insure proper operation.

2905 tbl 05

NOTE:
1. Reset Configuration Mode bit input when $\overline{Reset}$ is asserted, normal signal function when $\overline{Reset}$ is de-asserted.

ABSOLUTE MAXIMUM RATINGS(1, 3) R3041

Symbol	Rating	Commercial	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_C	Operating Case Temperature	0 to +85	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
V_{IN}	Input Voltage	–0.5 to +7.0	V

2905 tbl 06

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{IN} minimum = –3.0V for pulse width less than 15ns. V_{IN} should not exceed V_{CC} +0.5 Volts.
3. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

AC TEST CONDITIONS R3041

Symbol	Parameter	Min.	Max.	Unit
V_{IH}	Input HIGH Voltage	3.0	—	V
V_{IL}	Input LOW Voltage	—	0	V
V_{IHS}	Input HIGH Voltage	3.5	—	V
V_{ILS}	Input LOW Voltage	—	0	V

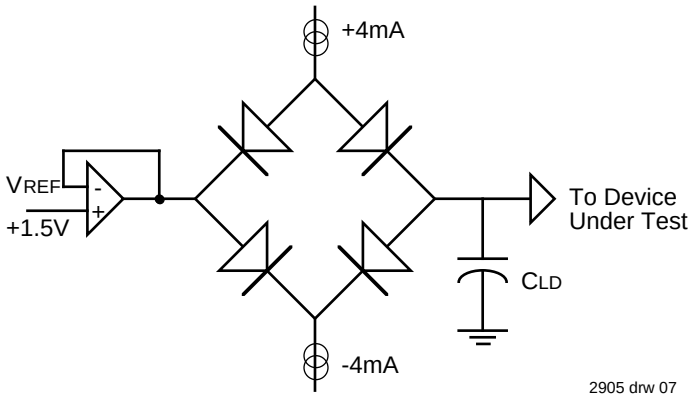
2905 tbl 08

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Commercial	0°C to +85°C (Case)	0V	5.0 ±5%

2905 tbl 07

OUTPUT LOADING FOR AC TESTING



2905 drw 07

Signal	Cld
All Signals	25 pF

2905 tbl 09

DC ELECTRICAL CHARACTERISTICS R3041 — (T_C = 0°C to +85°C, V_{CC} = +5.0V ±5%)

Symbol	Parameter	Test Conditions	16.67MHz		20MHz		25MHz		33MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4mA	3.5	—	3.5	—	3.5	—	3.5	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4mA	—	0.4	—	0.4	—	0.4	—	0.4	V
V_{IH}	Input HIGH Voltage(3)	—	2.0	—	2.0	—	2.0	—	2.0	—	V
V_{IL}	Input LOW Voltage(1)	—	—	0.8	—	0.8	—	0.8	—	0.8	V
V_{IHS}	Input HIGH Voltage(2,3)	—	3.0	—	3.0	—	3.0	—	3.0	—	V
V_{ILS}	Input LOW Voltage(1,2)	—	—	0.4	—	0.4	—	0.4	—	0.4	V
C_{IN}	Input Capacitance(4)	—	—	10	—	10	—	10	—	10	pF
C_{OUT}	Output Capacitance(4)	—	—	10	—	10	—	10	—	10	pF
I_{CC}	Operating Current	V_{CC} = 5V, T_C = 25°C	—	225	—	250	—	300	—	370	mA
I_{IH}	Input HIGH Leakage	V_{IH} = VCC	—	100	—	100	—	100	—	100	µA
I_{IL}	Input LOW Leakage	V_{IL} = GND	–100	—	–100	—	–100	—	–100	—	µA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	–100	100	–100	100	–100	100	–100	100	µA

2905 tbl 10

NOTES:
1. V_{IL} Min. = –3.0V for pulse width less than 15ns. V_{IL} should not fall below –0.5 volts for larger periods.
2. V_{IHS} and V_{ILS} apply to ClkIn and $\overline{\text{Reset}}$.
3. V_{IH} should not be held above V_{CC} + 0.5 volts.
4. Guaranteed by design.

AC ELECTRICAL CHARACTERISTICS R3041 (1, 2, 3)— (T_C = 0°C to +85°C, V_{CC} = +5.0V ±5%)

Symbol	Signals	Description	16.67MHz		20MHz		25MHz		33MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t1	$\overline{BusReq}$, $\overline{Ack}$, $\overline{BusError}$, $\overline{RdCEn}$	Set-up to $\overline{SysClk}$ rising	11	—	8	—	5.5	—	5.5	—	ns
t1a	A/D	Set-up to $\overline{SysClk}$ falling	12	—	9	—	7	—	7	—	ns
t2	$\overline{BusReq}$, $\overline{Ack}$, $\overline{BusError}$, $\overline{RdCEn}$	Hold from $\overline{SysClk}$ rising	4	—	3	—	2.5	—	2.5		ns
t2a	A/D	Hold from $\overline{SysClk}$ falling	2	—	2	—	1	—	1	—	ns
t3	A/D, Addr, Diag, ALE, $\overline{Wr}$ $\overline{Burst/WrNear}$, $\overline{Rd}$, $\overline{DataEn}$	Tri-state from SysClk rising (after driven condition)	—	13	—	10	—	10	—	10	ns
t4	A/D, Addr, Diag, ALE, $\overline{Wr}$ $\overline{Burst/WrNear}$, $\overline{Rd}$, $\overline{DataEn}$	Driven from $\overline{SysClk}$ falling (after tri-state condition)	—	13	—	10	—	10	—	10	ns
t5	$\overline{BusGnt}$	Asserted from $\overline{SysClk}$ rising	—	10	—	8	—	7	—	7	ns
t6	$\overline{BusGnt}$	Negated from $\overline{SysClk}$ falling	—	10	—	8	—	7	—	7	ns
t7	$\overline{Wr}$, $\overline{Rd}$, $\overline{Burst/WrNear}$, $\overline{TC}$	Valid from $\overline{SysClk}$ rising	—	8	—	6	—	5	—	5	ns
t7a	A/D	Valid from $\overline{SysClk}$ rising	—	12	—	9	—	8	—	8	ns
t7b	$\overline{Last}$	Valid from $\overline{SysClk}$ rising	—	12	—	9	—	8	—	8	ns
t8	ALE	Asserted from $\overline{SysClk}$ rising	—	5	—	4	—	4	—	4	ns
t9	ALE	Negated from $\overline{SysClk}$ falling	—	5	—	4	—	4	—	4	ns
t10	A/D	Hold from ALE negated	2	—	2	—	2	—	1.5		ns
t11	$\overline{DataEn}$	Asserted from $\overline{SysClk}$	—	19	—	15	—	15	—	15	ns
t12	$\overline{DataEn}$	Asserted from A/D tri-state(4)	0	—	0	—	0	—	0	—	ns
t14	A/D	Driven from $\overline{SysClk}$ rising(4)	0	—	0	—	0	—	0	—	ns
t15	$\overline{Wr}$, $\overline{Rd}$, $\overline{DataEn}$, $\overline{Burst/WrNear}$, $\overline{Last}$, $\overline{TC}$	Negated from $\overline{SysClk}$ falling	—	9	—	7	—	6	—	6	ns
t16	Addr(3:0), $\overline{BE\ 16(1:0)}$	Valid from $\overline{SysClk}$	—	11	—	8	—	7	—	7	ns
t17	Diag	Valid from $\overline{SysClk}$	—	15	—	12	—	11	—	11	ns
t18	A/D	Tri-state from $\overline{SysClk}$	—	13	—	10	—	10	—	10	ns
t19	A/D	$\overline{SysClk}$ to data out	—	16	—	13	—	12	—	12	ns
t20	ClkIn	Pulse Width High	12	—	10	—	8	—	6.5	—	ns
t21	ClkIn	Pulse Width Low	12	—	10	—	8	—	6.5	—	ns
t22	ClkIn	Clock Period	30	250	25	250	20	250	15	250	ns
t23	$\overline{Reset}$	Pulse Width from Vcc valid	200	—	200	—	200	—	200	—	µs
t24	$\overline{Reset}$	Minimum Pulse Width	32	—	32	—	32	—	32	—	sys
t25	$\overline{Reset}$	Set-up to $\overline{SysClk}$ falling	8	—	6	—	5	—	5	—	ns
t26	$\overline{Int}$	Mode set-up to $\overline{Reset}$ rising	8	—	6	—	5	—	5	—	ns
t27	$\overline{Int}$	Mode hold from $\overline{Reset}$ rising	2.5	—	2.5	—	2.5	—	2.5	—	ns
t28	$\overline{SInt}$, SBrCond	Set-up to $\overline{SysClk}$ falling	8	—	6	—	5	—	5	—	ns
t29	$\overline{SInt}$, SBrCond	Hold from $\overline{SysClk}$ falling	4	—	3	—	3	—	3	—	ns
t30	$\overline{Int}$, BrCond	Set-up to $\overline{SysClk}$ falling	8	—	6	—	5	—	5	—	ns
t31	$\overline{Int}$, BrCond	Hold from $\overline{SysClk}$ falling	4	—	3	—	3	—	3	—	ns
tsys	$\overline{SysClk}$	Pulse Width	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	ns
t32	$\overline{SysClk}$	Clock High Time	t22 - 2	t22 + 2	t22 - 2	t22 + 2	t22 - 2	t22 + 2	t22 - 2	t22 + 2	ns
t33	$\overline{SysClk}$	Clock Low Time	t22 - 2	t22 + 2	t22 - 2	t22 + 2	t22 - 2	t22 + 2	t22 - 2	t22 + 2	ns

2905 tbl 11

DC ELECTRICAL CHARACTERISTICS RV3041 — (T_C = 0°C to +85°C, V_{CC} = +3.3V ±5%)

Symbol	Parameter	Test Conditions	16.67MHz		20MHz		25MHz		33MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4mA	2.4	—	2.4	—	2.4	—	2.4	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4mA	—	0.4	—	0.4	—	0.4	—	0.4	V
V_{IH}	Input HIGH Voltage(3)	—	2.0	—	2.0	—	2.0	—	2.0	—	V
V_{IL}	Input LOW Voltage(1)	—	—	0.8	—	0.8	—	0.8	—	0.8	V
V_{IHS}	Input HIGH Voltage(2,3)	—	2.5	—	2.5	—	2.5	—	2.5	—	V
V_{ILS}	Input LOW Voltage(1,2)	—	—	0.4	—	0.4	—	0.4	—	0.4	V
C_{IN}	Input Capacitance(4)	—	—	10	—	10	—	10	—	10	pF
C_{OUT}	Output Capacitance(4)	—	—	10	—	10	—	10	—	10	pF
I_{CC}	Operating Current	V_{CC} = 3.3V, T_C = 25°C	—	130	—	150	—	180	—	225	mA
I_{IH}	Input HIGH Leakage	V_{IH} = VCC	—	100	—	100	—	100	—	100	mA
I_{IL}	Input LOW Leakage	V_{IL} = GND	–100	—	–100	—	–100	—	–100	—	mA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	–100	100	–100	100	–100	100	–100	100	mA

NOTES:

2905 tbl 10

1. V_{IL} Min. = –3.0V for pulse width less than 15ns. V_{IL} should not fall below –0.5 volts for larger periods.
2. V_{IHS} and V_{ILS} apply to ClkIn and $\overline{\text{Reset}}$.
3. V_{IH} should not be held above V_{CC} + 0.5 volts.
4. Guaranteed by design.

AC ELECTRICAL CHARACTERISTICS RV3041 (1, 2, 3)— (T_C = 0°C to +85°C, V_{CC} = +3.3V ±5%)

Symbol	Signals	Description	16.67MHz		20MHz		25MHz		33MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t1	$\overline{\text{BusReq}}$, $\overline{\text{Ack}}$, $\overline{\text{BusError}}$, $\overline{\text{RdCEn}}$	Set-up to $\overline{\text{SysClk}}$ rising	11	—	8	—	5.5	—	5.5	—	ns
t1a	A/D	Set-up to $\overline{\text{SysClk}}$ falling	12	—	9	—	7	—	7	—	ns
t2	$\overline{\text{BusReq}}$, $\overline{\text{Ack}}$, $\overline{\text{BusError}}$, $\overline{\text{RdCEn}}$	Hold from $\overline{\text{SysClk}}$ rising	4	—	3	—	2.5	—	2.5	—	ns
t2a	A/D	Hold from $\overline{\text{SysClk}}$ falling	2	—	2	—	1	—	1	—	ns
t3	A/D, Addr, Diag, ALE, $\overline{\text{Wr}}$ $\overline{\text{Burst/WrNear}}$, $\overline{\text{Rd}}$, $\overline{\text{DataEn}}$	Tri-state from $\overline{\text{SysClk}}$ rising (after driven condition)	—	13	—	10	—	10	—	10	ns
t4	A/D, Addr, Diag, ALE, $\overline{\text{Wr}}$ $\overline{\text{Burst/WrNear}}$, $\overline{\text{Rd}}$, $\overline{\text{DataEn}}$	Driven from $\overline{\text{SysClk}}$ falling (after tri-state condition)	—	13	—	10	—	10	—	10	ns
t5	$\overline{\text{BusGnt}}$	Asserted from $\overline{\text{SysClk}}$ rising	—	10	—	8	—	7	—	7	ns
t6	$\overline{\text{BusGnt}}$	Negated from $\overline{\text{SysClk}}$ falling	—	10	—	8	—	7	—	7	ns
t7	$\overline{\text{Wr}}$, $\overline{\text{Rd}}$, $\overline{\text{Burst/WrNear}}$, TC	Valid from $\overline{\text{SysClk}}$ rising	—	8	—	6	—	5	—	5	ns
t7a	A/D	Valid from $\overline{\text{SysClk}}$ rising	—	12	—	9	—	8	—	8	ns
t7b	Last	Valid from $\overline{\text{SysClk}}$ rising	—	12	—	9	—	8	—	8	ns
t8	ALE	Asserted from $\overline{\text{SysClk}}$ rising	—	5	—	4	—	4	—	4	ns
t9	ALE	Negated from $\overline{\text{SysClk}}$ falling	—	5	—	4	—	4	—	4	ns
t10	A/D	Hold from ALE negated	2	—	2	—	2	—	1.5		ns
t11	$\overline{\text{DataEn}}$	Asserted from $\overline{\text{SysClk}}$	—	19	—	15	—	15	—	15	ns
t12	$\overline{\text{DataEn}}$	Asserted from A/D tri-state(4)	0	—	0	—	0	—	0	—	ns
t14	A/D	Driven from $\overline{\text{SysClk}}$ rising(4)	0	—	0	—	0	—	0	—	ns
t15	$\overline{\text{Wr}}$, $\overline{\text{Rd}}$, $\overline{\text{DataEn}}$, $\overline{\text{Burst/WrNear}}$, Last, TC	Negated from $\overline{\text{SysClk}}$ falling	—	9	—	7	—	6	—	6	ns
t16	Addr(3:0), BE 16(1:0)	Valid from $\overline{\text{SysClk}}$	—	11	—	8	—	7	—	7	ns
t17	Diag	Valid from $\overline{\text{SysClk}}$	—	15	—	12	—	11	—	11	ns

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AC ELECTRICAL CHARACTERISTICS RV3041 (CONT.)

Symbol	Signals	Description	16.67 MHz		20 MHz		25MHz		33MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t18	A/D	Tri-state from $\overline{\text{SysClk}}$	—	13	—	10	—	10	—	10	ns
t19	A/D	$\overline{\text{SysClk}}$ to data out	—	16	—	13	—	12	—	12	ns
t20	ClkIn	Pulse Width High	12	—	10	—	8	—	6.5	—	ns
t21	ClkIn	Pulse Width Low	12	—	10	—	8	—	6.5	—	ns
t22	ClkIn	Clock Period	30	250	25	250	20	250	15	250	ns
t23	$\overline{\text{Reset}}$	Pulse Width from Vcc valid	200	—	200	—	200	—	200	—	µs
t24	$\overline{\text{Reset}}$	Minimum Pulse Width	32	—	32	—	32	—	32	—	sys
t25	$\overline{\text{Reset}}$	Set-up to $\overline{\text{SysClk}}$ falling	8	—	6	—	5	—	5	—	ns
t26	$\overline{\text{Int}}$	Mode set-up to $\overline{\text{Reset}}$ rising	8	—	6	—	5	—	5	—	ns
t27	$\overline{\text{Int}}$	Mode hold from $\overline{\text{Reset}}$ rising	2.5	—	2.5	—	2.5	—	2.5	—	ns
t28	$\overline{\text{SInt}}$, SBrCond	Set-up to $\overline{\text{SysClk}}$ falling	8	—	6	—	5	—	5	—	ns
t29	$\overline{\text{SInt}}$, SBrCond	Hold from $\overline{\text{SysClk}}$ falling	4	—	3	—	3	—	3	—	ns
t30	$\overline{\text{Int}}$, BrCond	Set-up to $\overline{\text{SysClk}}$ falling	8	—	6	—	5	—	5	—	ns
t31	$\overline{\text{Int}}$, BrCond	Hold from $\overline{\text{SysClk}}$ falling	4	—	3	—	3	—	3	—	ns
tsys	$\overline{\text{SysClk}}$	Pulse Width	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	ns
t32	$\overline{\text{SysClk}}$	Clock High Time	t22 - 2	t22 + 2	t22 - 2	t22 + 2	t22 - 2	t22 + 2	t22 - 2	t22 + 2	ns
t33	$\overline{\text{SysClk}}$	Clock Low Time	t22 - 2	t22 + 2	t22 - 2	t22 + 2	t22 - 2	t22 + 2	t22 - 2	t22 + 2	ns
t45	$\overline{\text{ExtDataEn}}$	Tri-state from $\overline{\text{SysClk}}$ rising (after driven condition)	—	13	—	10	—	10	—	10	ns
t46	$\overline{\text{ExtDataEn}}$	Driven from $\overline{\text{SysClk}}$ falling (after driven condition)	—	13	—	10	—	10	—	10	ns
t47	$\overline{\text{IOStrobe}}$	Valid from $\overline{\text{SysClk}}$ falling	—	10	—	8	—	7	—	7	ns
t48	$\overline{\text{ExtDataEn}}$,	Asserted from $\overline{\text{SysClk}}$ rising	—	15	—	12	—	9	—	9	ns
t49	$\overline{\text{ExtDataEn}}$ $\overline{\text{DataEn}}$	Negated from $\overline{\text{SysClk}}$ rising	—	9	—	7	—	6	—	6	ns
t50	$\overline{\text{MemStrobe}}$	Asserted from $\overline{\text{SysClk}}$ rising	—	19	—	15	—	15	—	15	ns
t51	$\overline{\text{MemStrobe}}$	Negated from $\overline{\text{SysClk}}$ falling	—	19	—	15	—	15	—	15	ns
t52	$\overline{\text{MemStrobe}}$	Asserted from Addr(3:0) valid(4)	0	—	0	—	0	—	0	—	ns
tderate	All outputs	Timing deration for loading over 25pF(4, 5)	—	0.5	—	0.5	—	0.5	—	0.5	ns/ 25pF

NOTES:

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1. All timings referenced to 1.5 Volts, with a rise and fall time of less than 2.5ns.
2. All outputs tested with 25pF loading.
3. The AC values listed here reference timing diagrams contained in the R3041 Hardware User's Manual.
4. Guaranteed by design.
5. This parameter is used to derate the AC timings according to the loading of the system. This parameter provides a deration for loads over the specified test condition; that is, the deration factor is applied for each 25pF over the specified test load condition.
6. Timings t34 - t44 are reserved for other RISController family members.

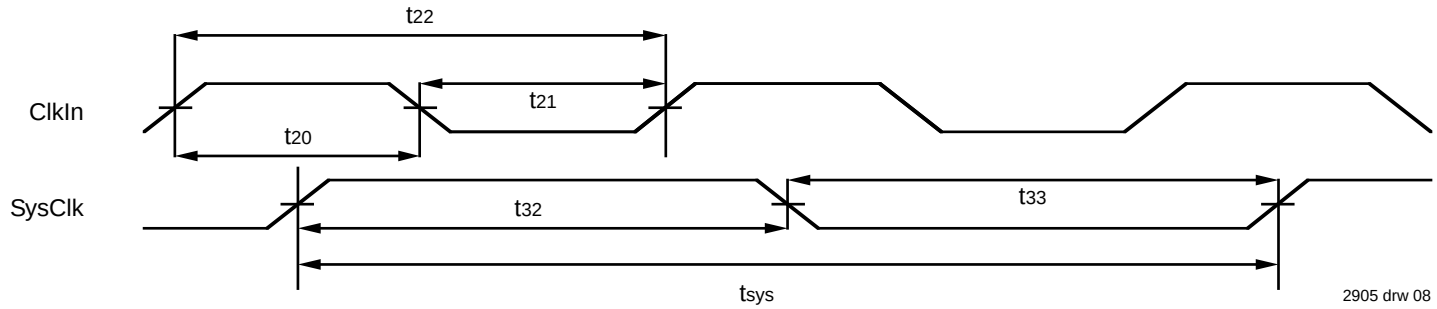


Figure 8. RISController Family Clocking

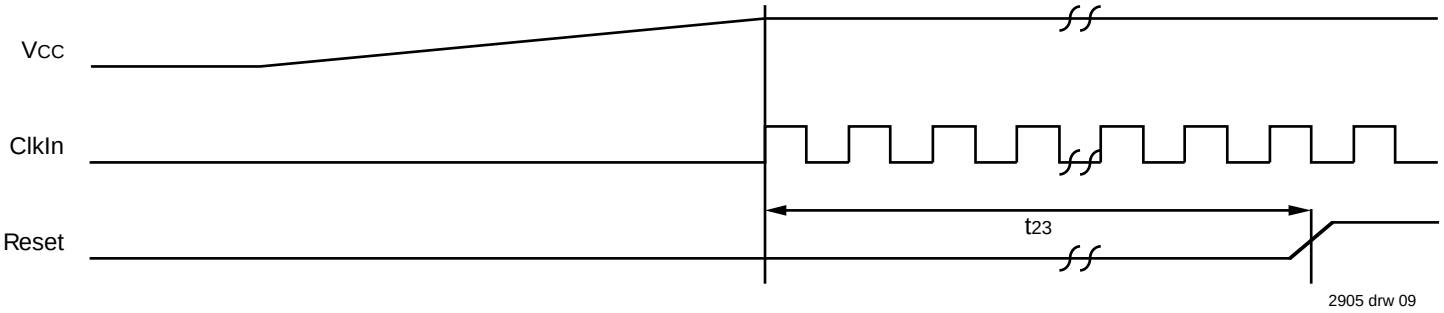


Figure 9. Power-On Reset Sequence

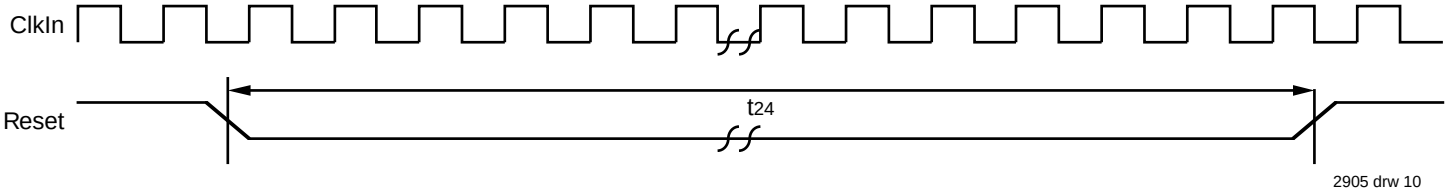


Figure 10(a). Warm Reset Sequence

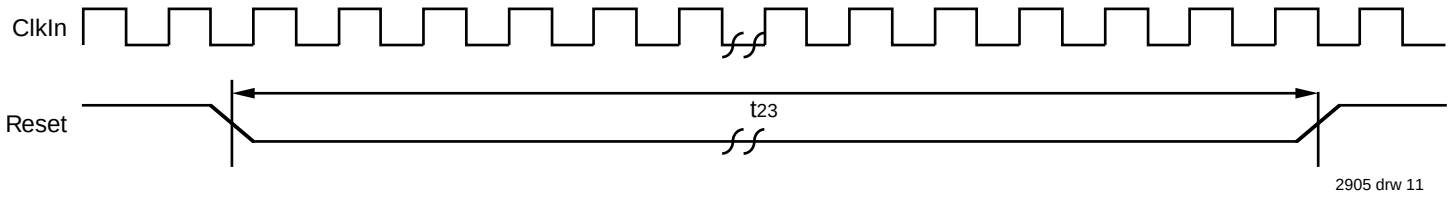


Figure 10(b). Warm Reset Sequence (Internal Pull-Ups Used)

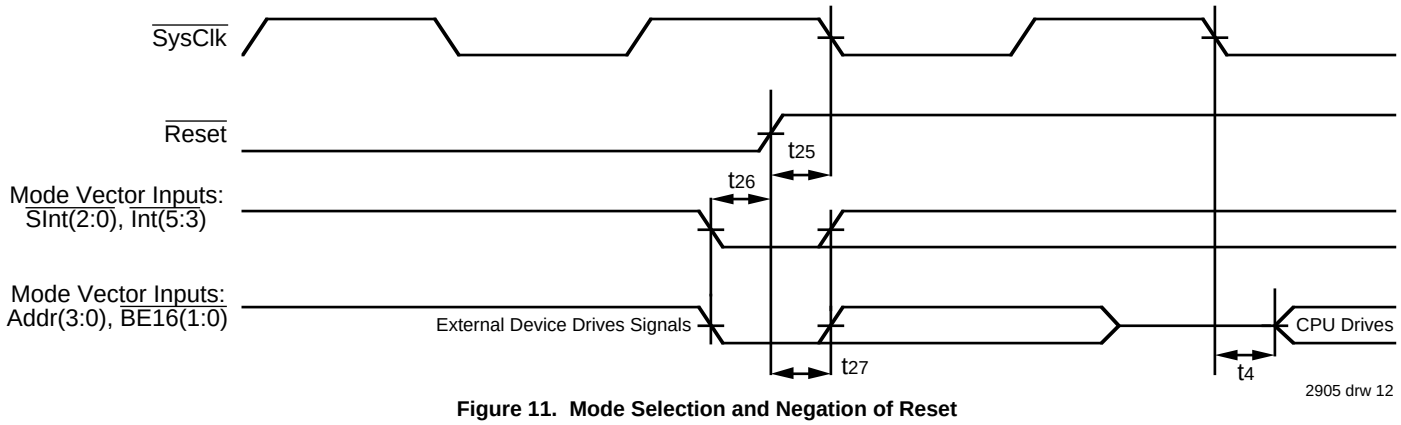


Figure 11. Mode Selection and Negation of Reset

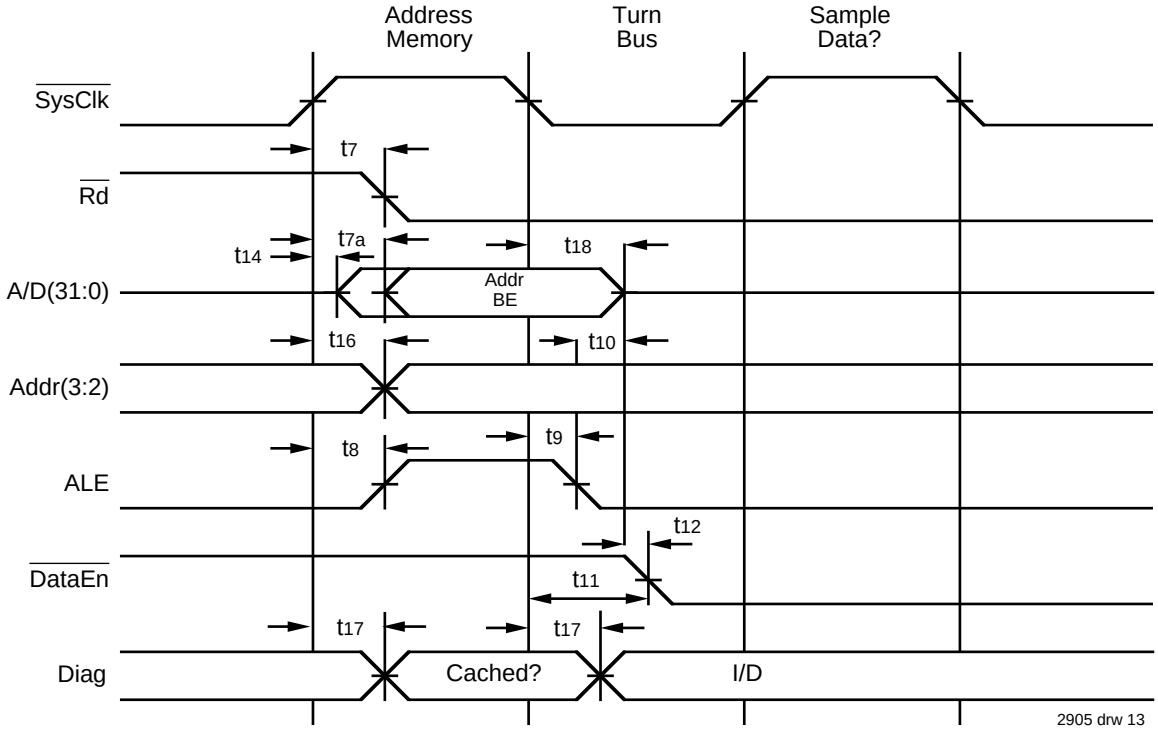


Figure 12(a). Start of Read Timing with Non-Extended Address Hold Option

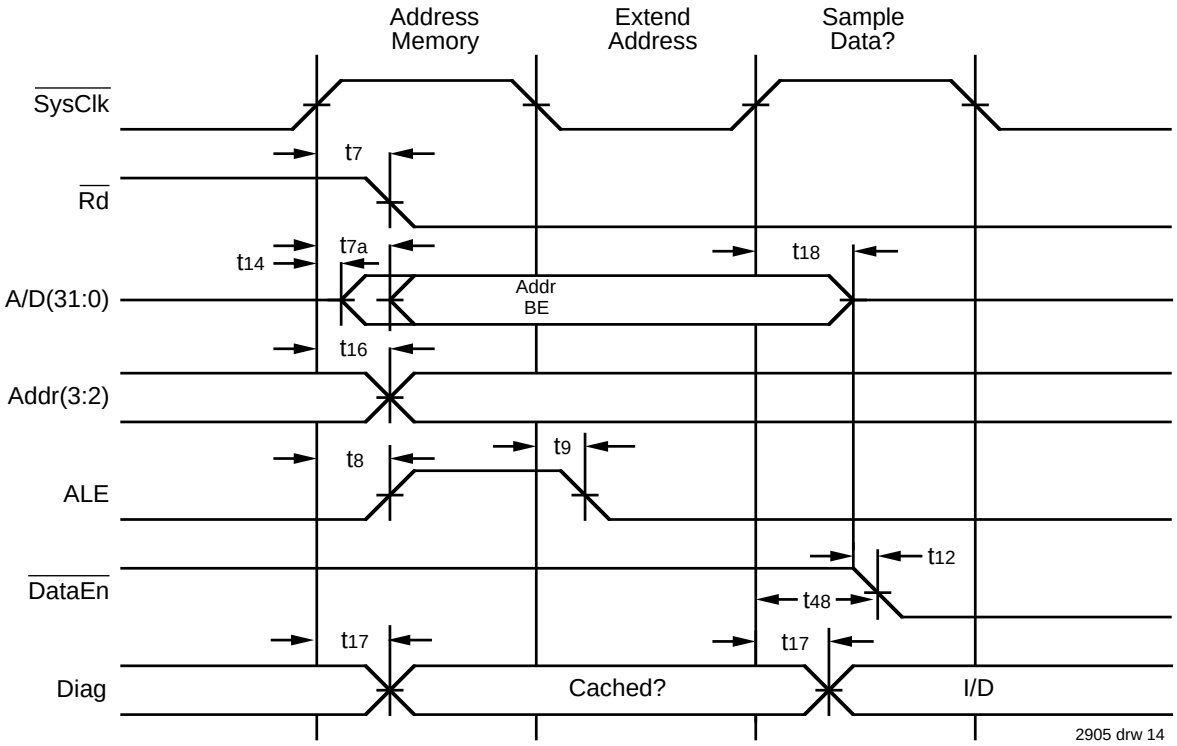


Figure 12(b). Start of Read Timing with Extended Address Hold Option

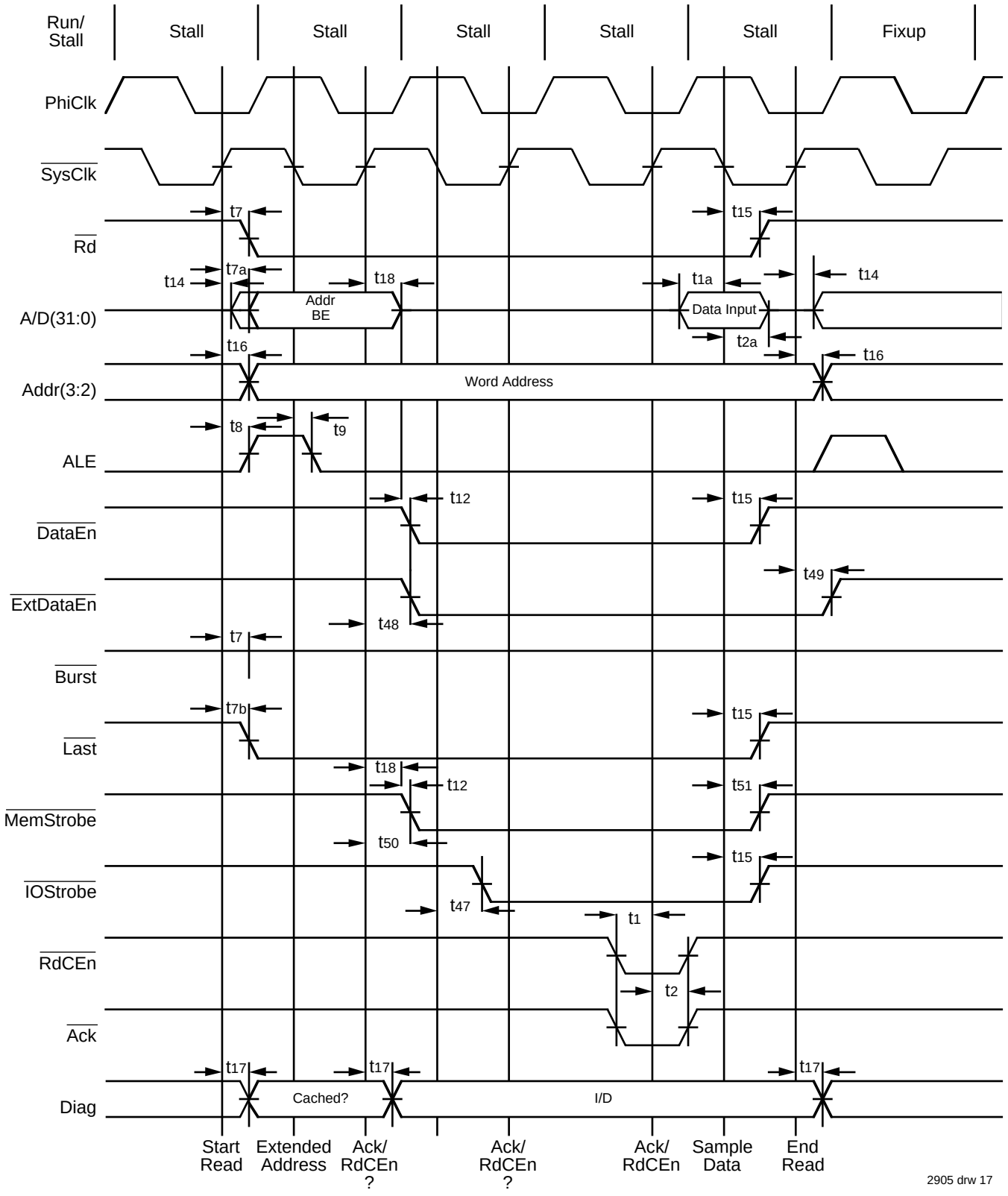


Figure 13. Single Datum Read

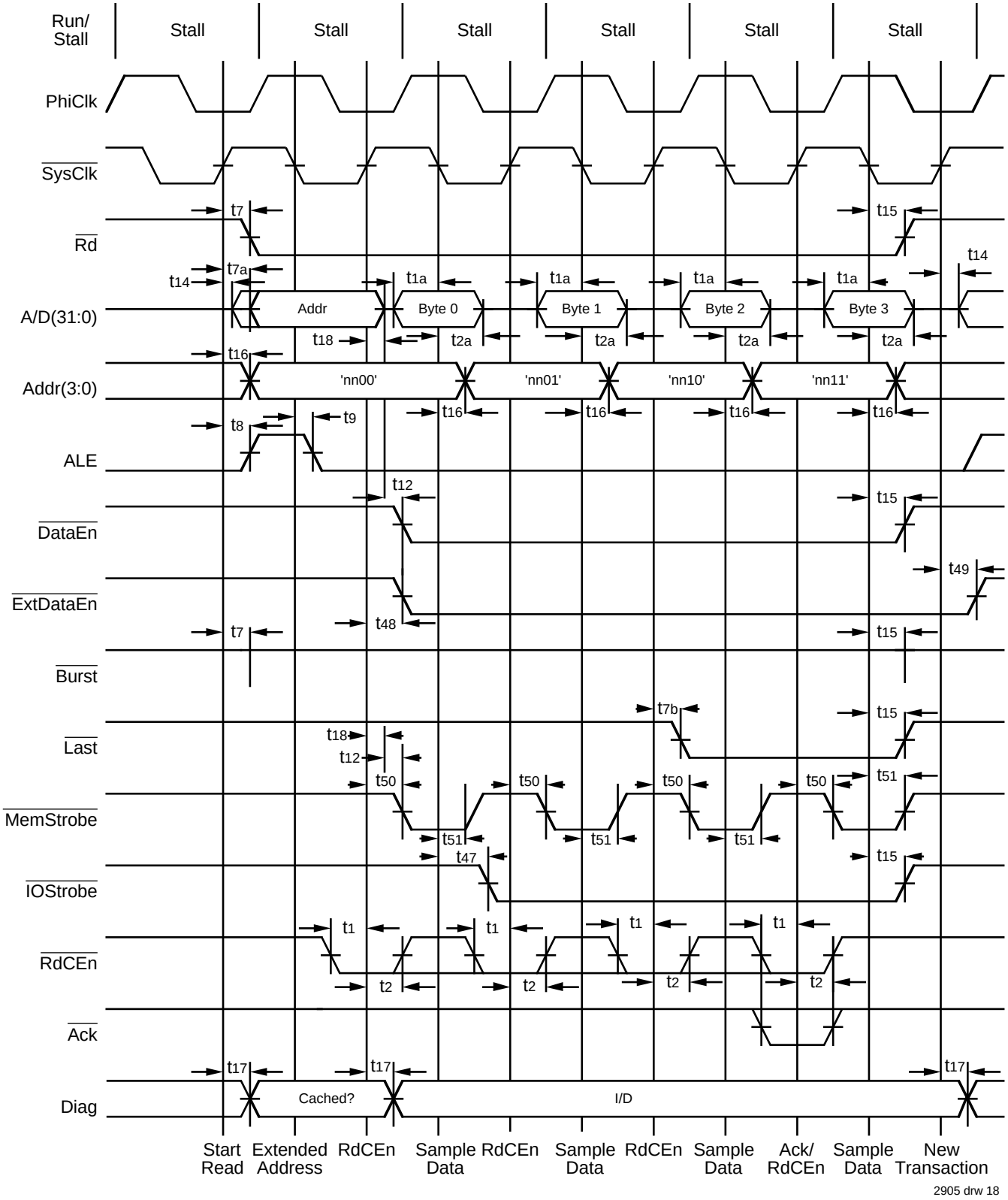


Figure 14. Mini-burst read of 32-bit datum from 8-bit wide memory port

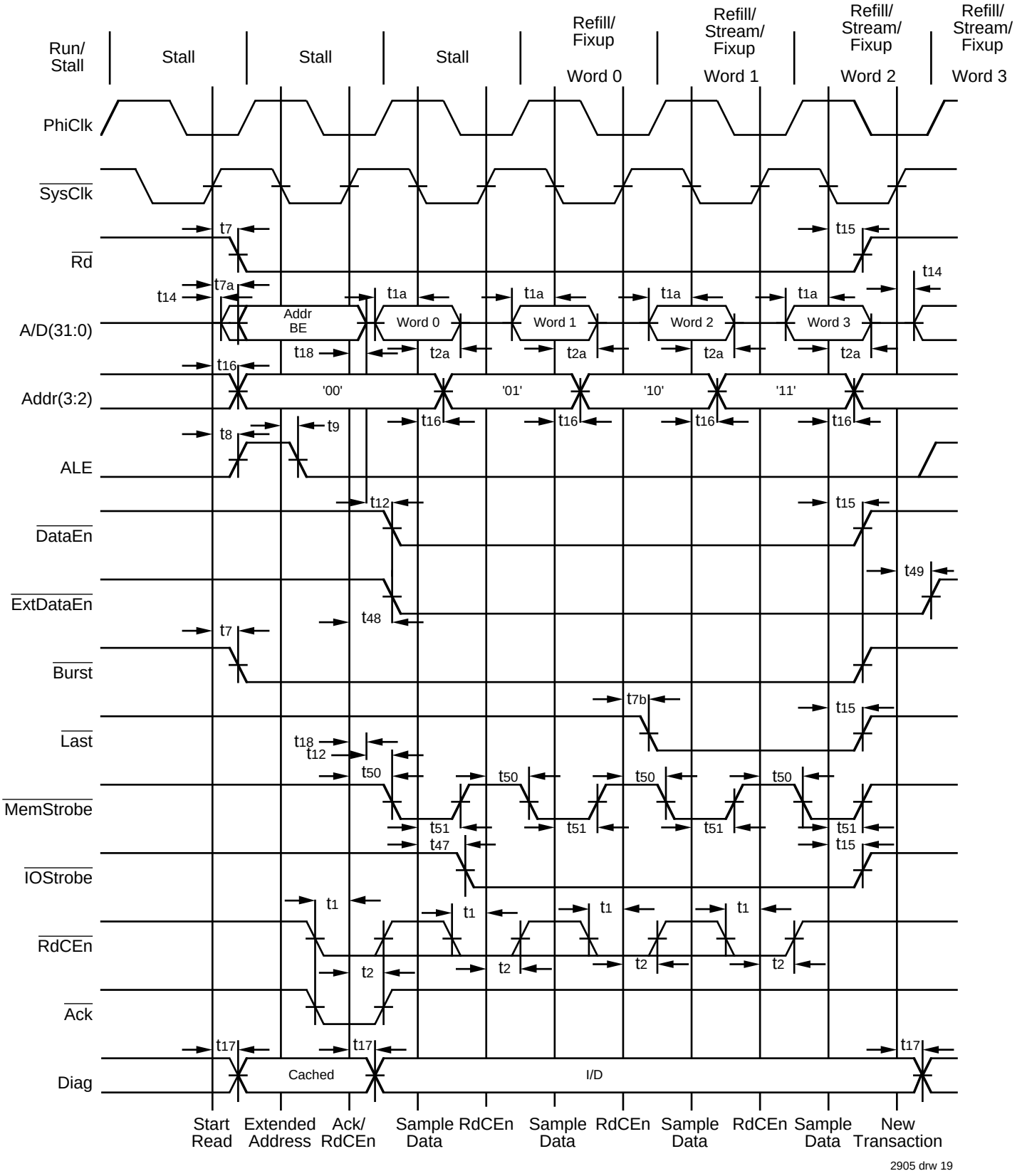


Figure 15. R3041 Quad Word Read

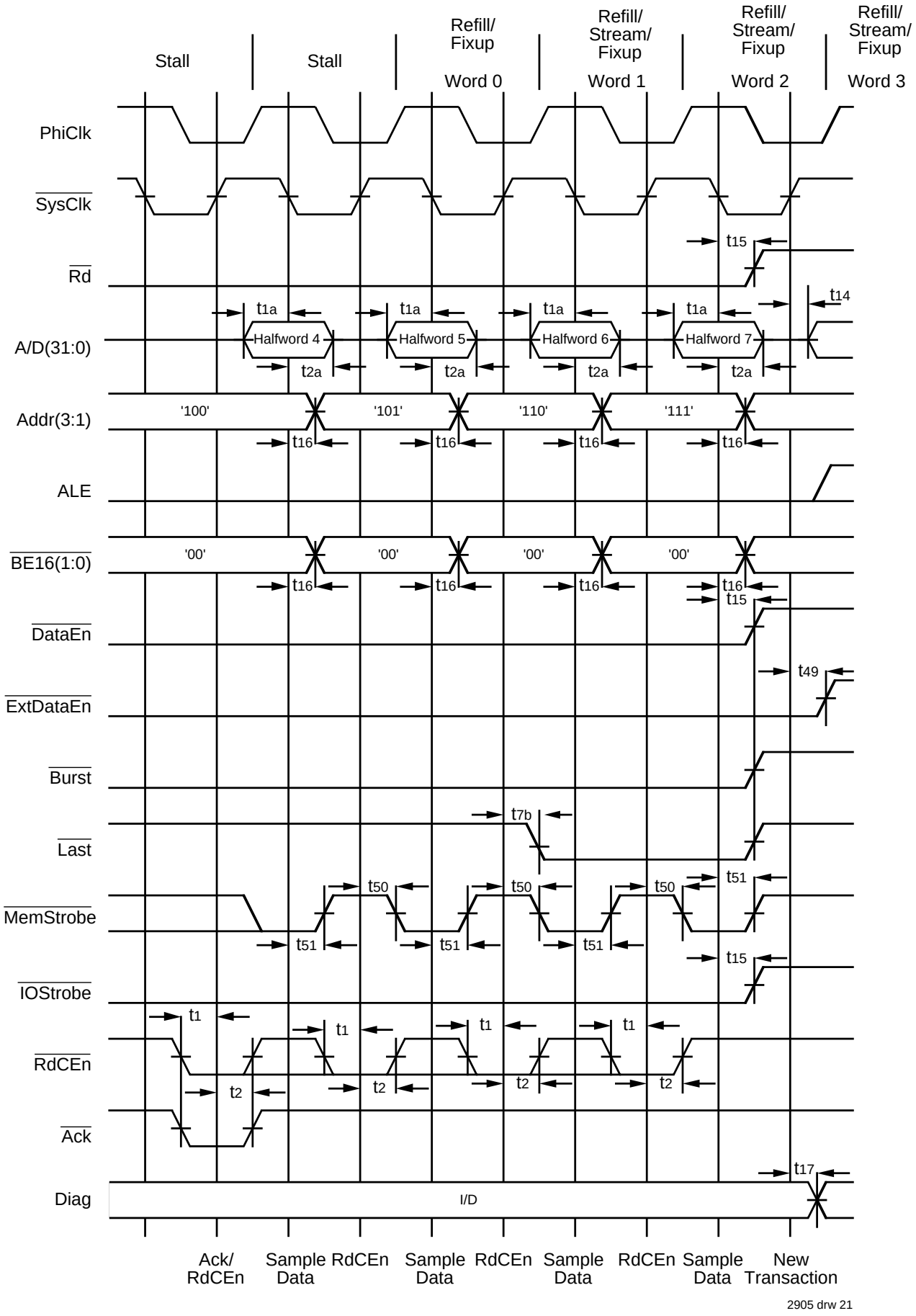


Figure 16(b). End of Quad Word read from 16-bit Wide Memory Port

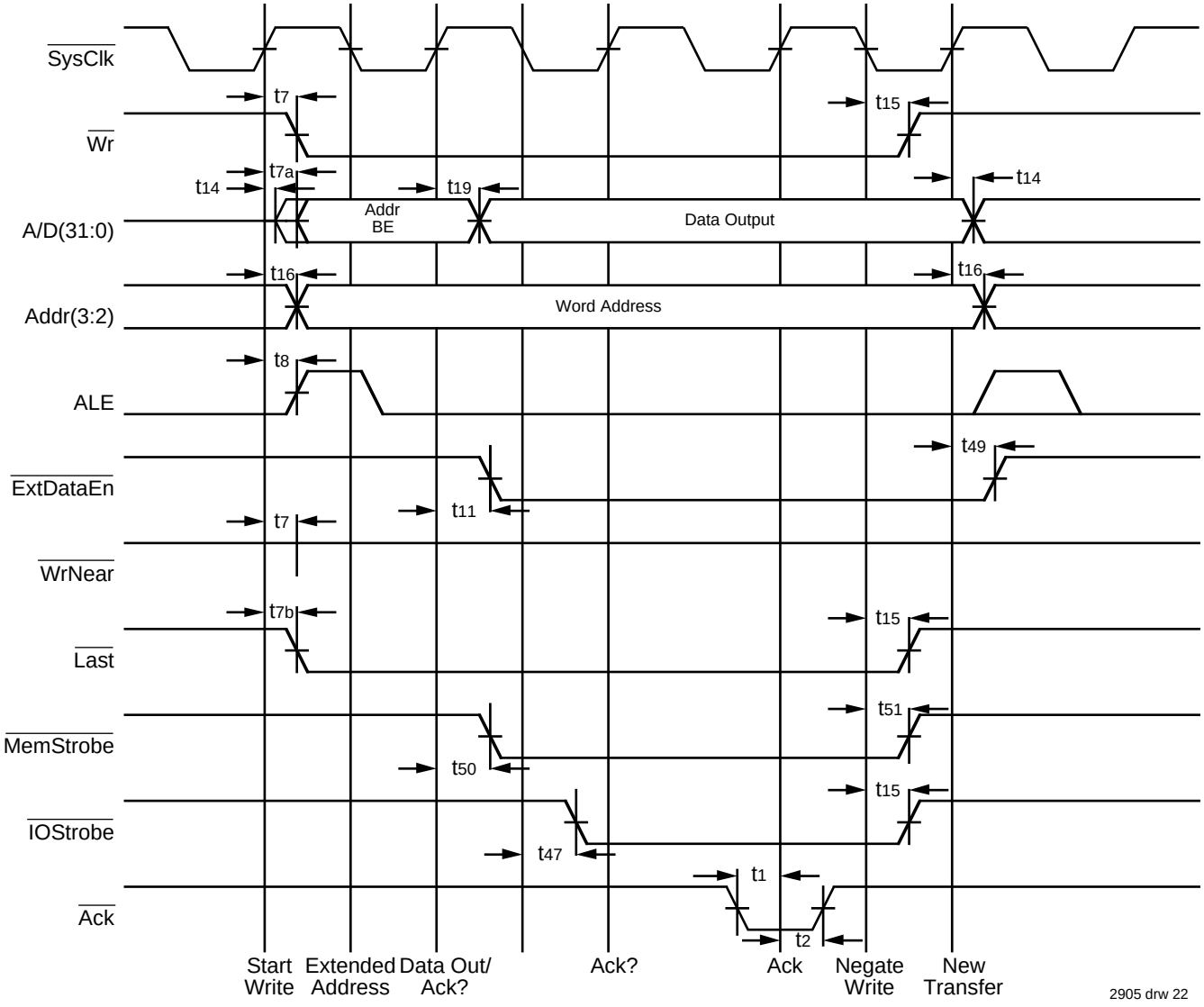


Figure 17. Basic Write to 32-bit Memory Port

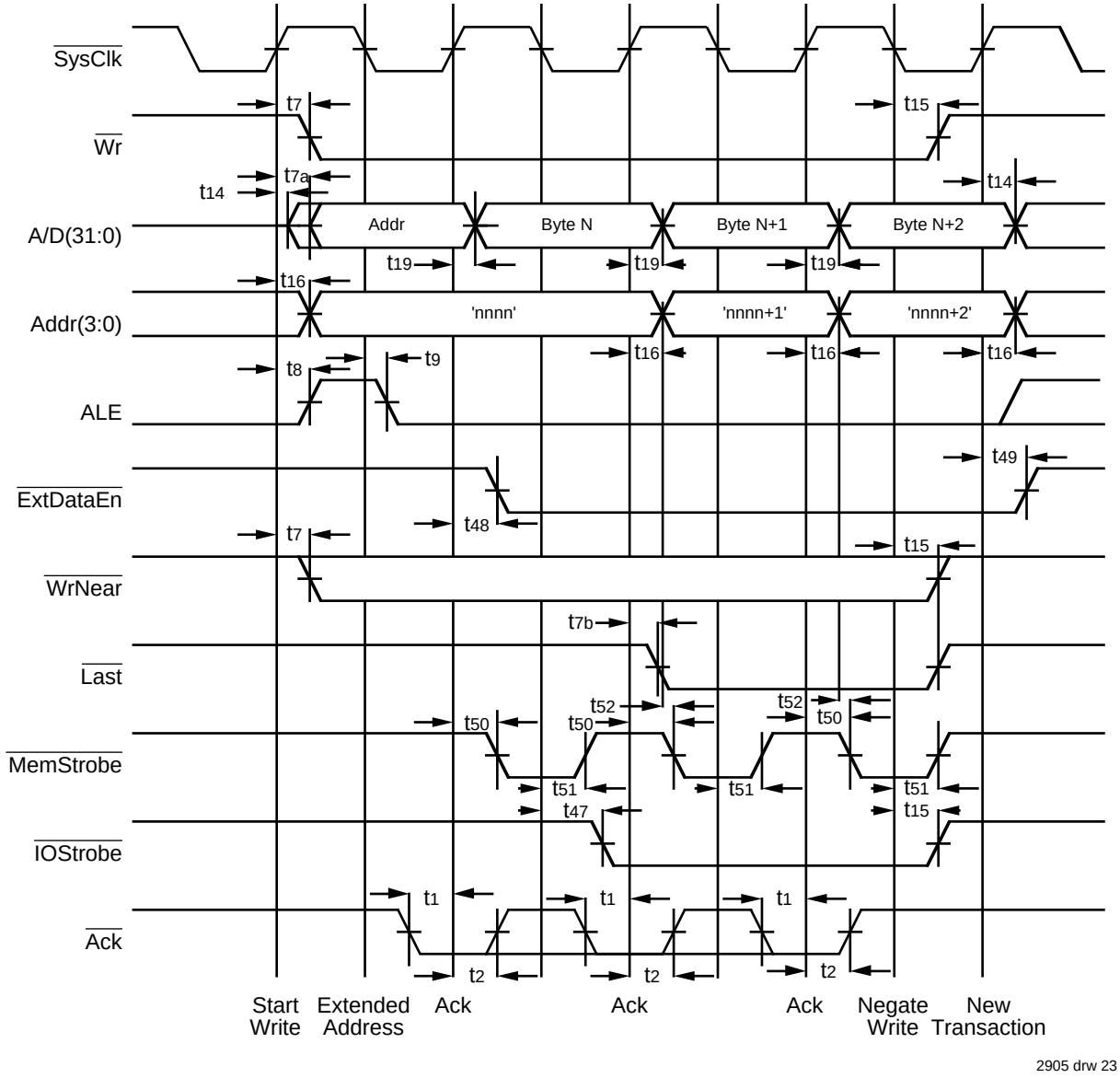


Figure 18. Tri-Byte Mini-burst Write to 8-bit Port

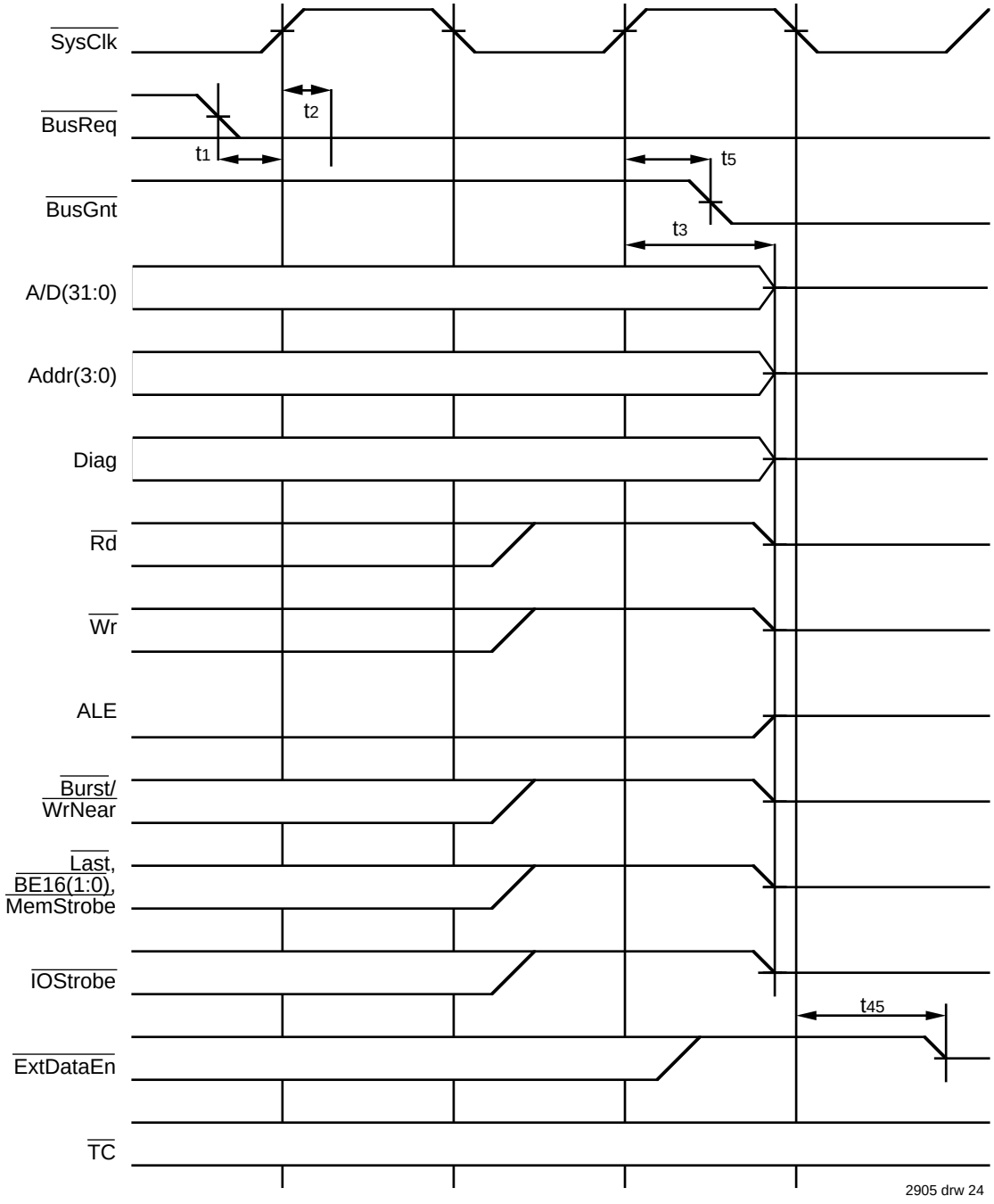


Figure 19. Request and Relinquish of R3041 Bus to External Master

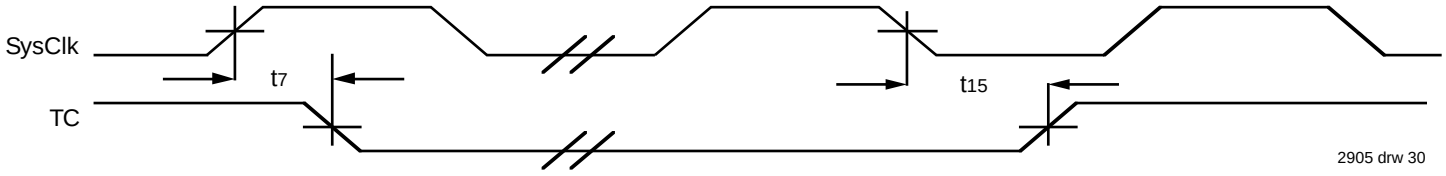
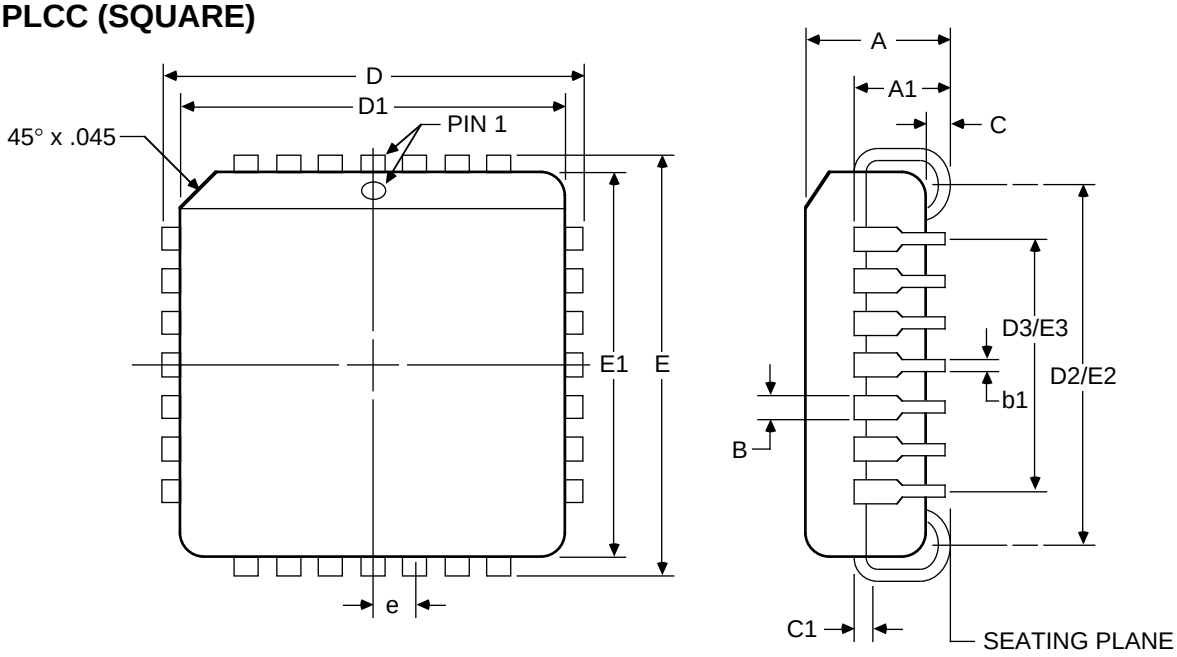


Figure 25. $\overline{TC}$ Output

84 LEAD PLCC (SQUARE)



DWG #	J84-1	
# of Leads	84	
Symbol	Min.	Max.
A	165	.180
A1	.095	.115
B	.026	.032
b1	.013	.021
C	.020	.040
C1	.008	.012
D	1.185	1.195
D1	1.150	1.156
D2/E2	1.090	1.130
D3/E3	1.000 REF	
E	1.185	1.195
E1	1.150	1.156
e	.050 BSC	
ND/NE	21	

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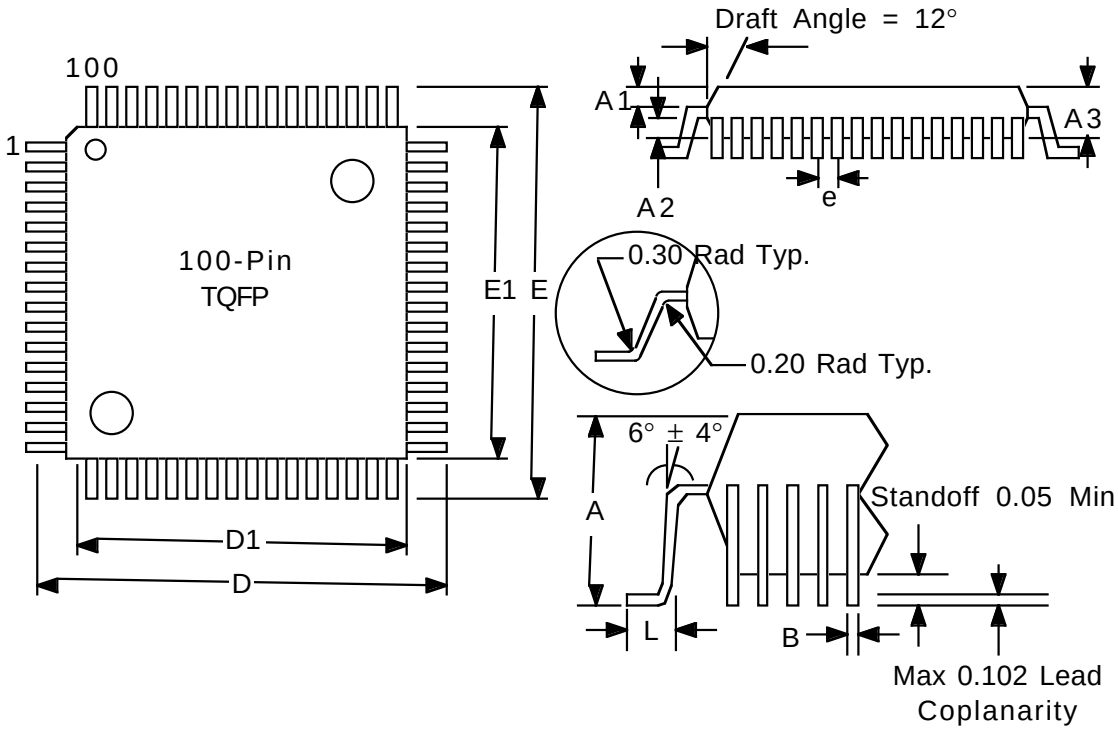
NOTES:
1. All dimensions are in inches, unless otherwise noted.
2. BSC—Basic lead Spacing between Centers.
3. D & E do not include mold flash or protutions.
4. Formed leads shall be planar with respect to one another and within .004" at the seating plane.
5. ND & NE represent the number of leads in the D & E directions respectively.
6. D1 & E1 should be measured from the bottom of the package.
7. PLCC is pin & form compatible with MQUAD; the MQUAD package is used in other RISController family members.

100-PIN TQFP



DWG #	TQFP	
# of Leads	100	
Symbol	Min.	Max.
A	—	1.60
A1	0.5	0.15
A2	1.35	1.45
D	15.75	16.25
D1	13.95	14.05
E	15.75	16.25
E1	13.95	14.05
L	0.45	0.70
N	100	
e	0.50BSC	
b	0.17	0.27
ccc	—	0.08
ddd	—	0.08
R	0.08	0.20
R1	0.08	—
θ	0	7.0
θ1	11.0	13.0
θ2	11.0	13.0
c	0.09	0.16

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