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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	MIPS-I
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	25MHz
Co-Processors/DSP	System Control; CP0
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 85°C (TC)
Security Features	-
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/idt79r3041-25jg8

System Control Co-Processor

The R3041 also integrates on-chip a System Control Co-processor, CP0. CP0 manages the exception handling capability of the R3041, the virtual to physical address mapping of the R3041, and the programmable bus interface capabilities of the R3041. These topics are discussed in subsequent sections.

The R3041 does not include the optional TLB found in other members of the RISController family, but instead performs the same virtual to physical address mapping of the base version of the RISController family. These devices still support distinct kernel and user mode operation, but do not require page management software or an on-chip TLB, leading to a simpler software model and a lower-cost processor.

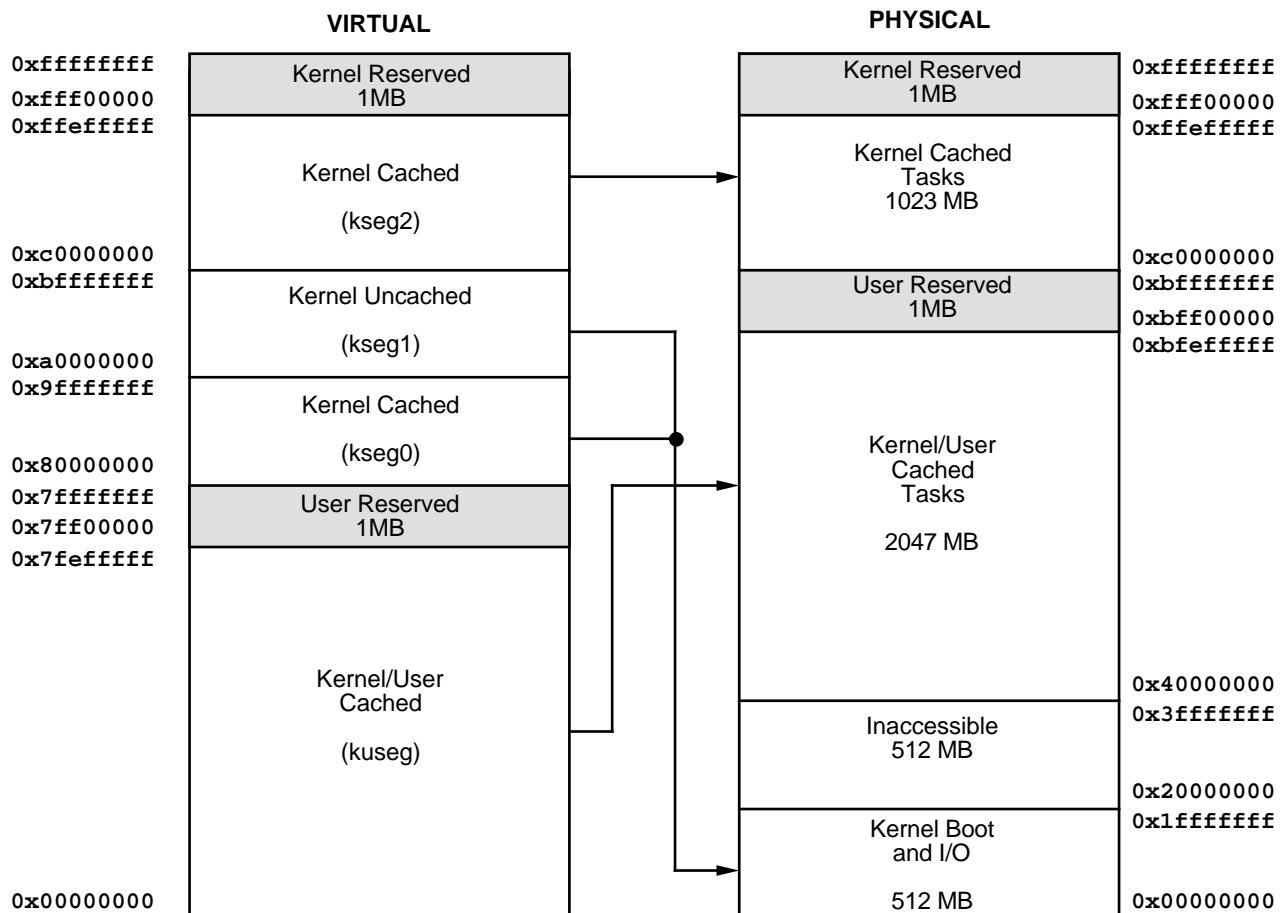
The memory mapping used by these devices is illustrated in Figure 3. Note that the reserved address spaces shown are for compatibility with future family members; in the current family members, references to these addresses are translated in the same fashion as their respective segments, with no traps or exceptions taken.

When using the base versions of the architecture, the system designer can implement a distinction between the user tasks and the kernel tasks, without having to execute page management software. This distinction can take the form of physical memory protection, accomplished by ad-

dress decoding, or in other system specific forms. In systems which do not wish to implement memory protection, and wish to have the kernel and user tasks operate out of a single unified memory space, upper address lines can be ignored by the address decoder, and thus all references will be seen in the lower gigabyte of the physical address space.

The R3041 adds additional resources into the on-chip CP0. These resources are detailed in the R3041 User's Manual. They allow kernel software to directly control activity of the processor internal resources and bus interface, and include:

- **Cache Configuration Register:** This register controls the data cache block size and miss refill algorithm.
- **Bus Control Register:** This register controls the behavior of the various bus interface signals.
- **Count and Compare Registers:** Together, these two registers implement a programmable 24-bit timer, which can be used for DRAM refresh or as a general purpose timer.
- **Port Size Control Register:** This register allows the kernel to indicate the port width of reads and writes to various sub-regions of the physical address space. Thus, the R3041 can interface directly with 8-, 16-, and 32-bit memory ports, including a mix of sizes, for both instruction and data references, without requiring additional external logic.



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Figure 3. Virtual to Physical Mapping of Base Architecture Versions

R3041.

SYSTEM USAGE

The IDT RISController family is specifically designed to easily connect to low-cost memory systems. Typical low-cost memory systems use inexpensive EPROMs, DRAMs, and application specific peripherals.

Figure 4 shows some of the flexibility inherent in the R3041. In this example system, which is typical of a laser printer, a 32-bit PROM interface is used due to the size of the PDL interpreter. An embedded system can optionally use an 8-bit

boot PROM instead. A 16-bit font/program cartridge interface is provided for add-in cards. A 16-bit DRAM interface is used for a low-cost page frame buffer. In this system example, a field or manufacturing upgrade to a 32-bit page frame buffer is supported by the boot software and DRAM controller. Embedded systems may optionally substitute SRAMs for the DRAMs. Finally various 8/16/32-bit I/O ports such as RS-232/422, SCSI, and LAN as well as the laser printer engine interface are supported. Such a system features a very low entry price, with a range of field upgrade options including the ability to upgrade to a more powerful member of the RISController family.

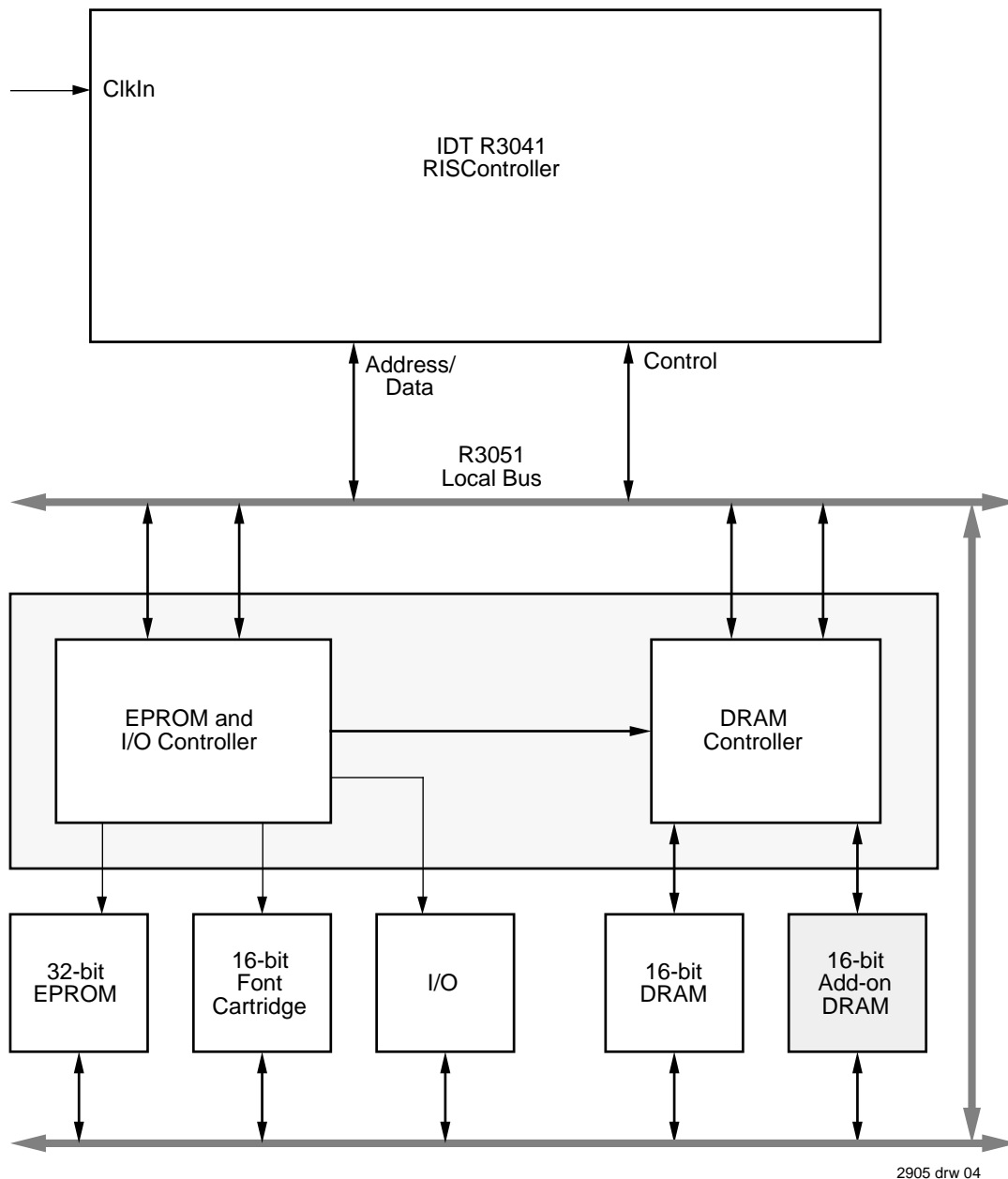


Figure 4. Typical R3041-Based Application

poke, etc.).

- IDT/kit™ (Kernel Integration Toolkit), providing library support and a frame work for the system run time environment.

PERFORMANCE OVERVIEW

The RISController family achieves a very high-level of performance. This performance is based on:

- **An efficient execution engine:** The CPU performs ALU operations and store operations in a single cycle, and has an effective load time of 1.3 cycles, and branch execution rate of 1.5 cycles (based on the ability of the compilers to avoid software interlocks). Thus, the R3041 achieves 20 MIPS performance at 25MHz when operating out of cache.
- **Large on-chip caches:** The RISController family contains caches which are substantially larger than those on the majority of embedded microprocessors. These large caches minimize the number of bus transactions required, and allow the RISController family to achieve actual sustained performance very close to its peak execution rate, even with low-cost memory systems.
- **Autonomous multiply and divide operations:** The RISController family features an on-chip integer multiplier/divide unit which is separate from the other ALU. This allows the R3041 to perform multiply or divide operations in parallel with other integer operations, using a single multiply or divide instruction rather than using "step" operations.
- **Integrated write buffer:** The R3041 features a four deep write buffer, which captures store target addresses and data at the processor execution rate and retires it to main memory at the slower main memory access rate. Use of on-chip write buffers eliminates the need for the processor to stall when performing store operations.
- **Burst read support:** The R3041 enables the system designer to utilize page mode, static column, or nibble mode RAMs when performing read operations to minimize the main memory read penalty and increase the effective cache hit rates.

The performance differences among the various RISController family members depends on the application software and the design of the memory system. Different family members feature different cache sizes, and the R3081 features a hardware floating point accelerator. Since all these devices can be used in a pin and software compatible fashion, the system designer has maximum freedom in trading between performance and cost. The memory simulation tools (e.g. Cache3041) allows the system designers to analyze and understand the performance differences among these de-

vices in their application.

SELECTABLE FEATURES

The RISController family uses two methods to allow the system designer to configure bus interface operation options.

The first set of options are established via the Reset Configuration Mode inputs, sampled during the device reset. After reset, the Reset Mode inputs become regular input or output signals.

The second set of configuration options are contained in the System Control Co-Processor registers. These Co-processor registers configuration options are typically initialized with the boot PROM and can also be changed dynamically by the kernel software.

Selectable features include:

- **Big Endian vs. Little Endian operation:** The part can be configured to operate with either byte ordering convention, and in fact may also be dynamically switched between the two conventions. This facilitates the porting of applications from other processor architectures, and also permits inter-communication between various types of processors and databases.
- **Data Cache Refill of one or four words:** The memory system must be capable of performing 4 word transfers to satisfy instruction cache misses and 1 word transfers to satisfy uncached references. The data cache refill size option allows the system designers to choose between one and four word refill on data cache misses, depending on the performance each option brings to their application.
- **Bus Turn Around speed:** The R3041 allows the kernel to increase the amount of time between bus transactions when changes in direction of the A/D bus occur (e.g., at the end of reads followed by writes). This allows transceivers and buffers to be eliminated from the system.
- **Extended Address Hold Time:** The R3041 allows the system designer to increase the amount of hold time available for address latching, thus allowing slower speed (low cost) address latches, FPGAs and ASICs to be used.
- **Programmable control signals:** The R3041 allows the system designer to optimally configure various memory control signals to be active on reads only, writes only, or on both reads and writes. This allows the simplification of external logic, thus reducing system cost.

- **Programmable memory Port Widths:** The R3041 allows the kernel to partition the physical memory space into various sub-regions, and to individually indicate the port width of these sub-regions. Thus, the bus interface unit can perform data packing and unpacking when communicating with narrow memory sub-regions. For example, these features, can be used to allow the R3041 to interface with narrow 8-bit boot PROMs, or to implement 16-bit only memory systems.

THERMAL CONSIDERATIONS

The RISController family utilizes special packaging techniques to improve the thermal properties of high-speed processors. Thus, all versions of the RISController family are packaged in cavity down packaging.

The lowest cost members of the family use a standard cavity down, injection molded PLCC package (the "J" package). This package is used for all speeds of the R3041 family.

Higher speed and higher performance members of the RISController family utilize more advanced packaging techniques to dissipate power while remaining both low-cost and pin- and socket- compatible with the PLCC package. Thus, these members of the RISController family are available in the MQUAD package (the "MJ" package), which is an all aluminum package with the die attached to a normal copper lead-frame mounted to the aluminum casing. The MQUAD package is pin and form compatible with the PLCC package. Thus, designers can choose to utilize this package without changing their PCB.

ØCA	Airflow (ft/min)					
	0	200	400	600	800	1000
"J" Package	29	26	21	18	16	15
TQFP	55	40	35	33	31	30

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Table 2. Thermal Resistance (ØCA) at Various Airflows

The members of the RISController family are guaranteed in a case temperature range of 0°C to +85°C. The type of package, speed (power) of the device, and airflow conditions, affect the equivalent ambient conditions which meet this specification.

The equivalent allowable ambient temperature, T_A , can be calculated using the thermal resistance from case to ambient (ØCA) of the given package. The following equation relates ambient and case temperature:

$$T_A = T_C - P * \text{ØCA}$$

where P is the maximum power consumption at hot temperature, calculated by using the maximum Icc specification for the device.

Typical values for ØCA at various airflows are shown in Table 2 for the PLCC package.

NOTES ON SYSTEM DESIGN

The R3041 has been designed to simplify the task of high-speed system design. Thus, set-up and hold-time requirements have been kept to a minimum, allowing a wide variety of system interface strategies.

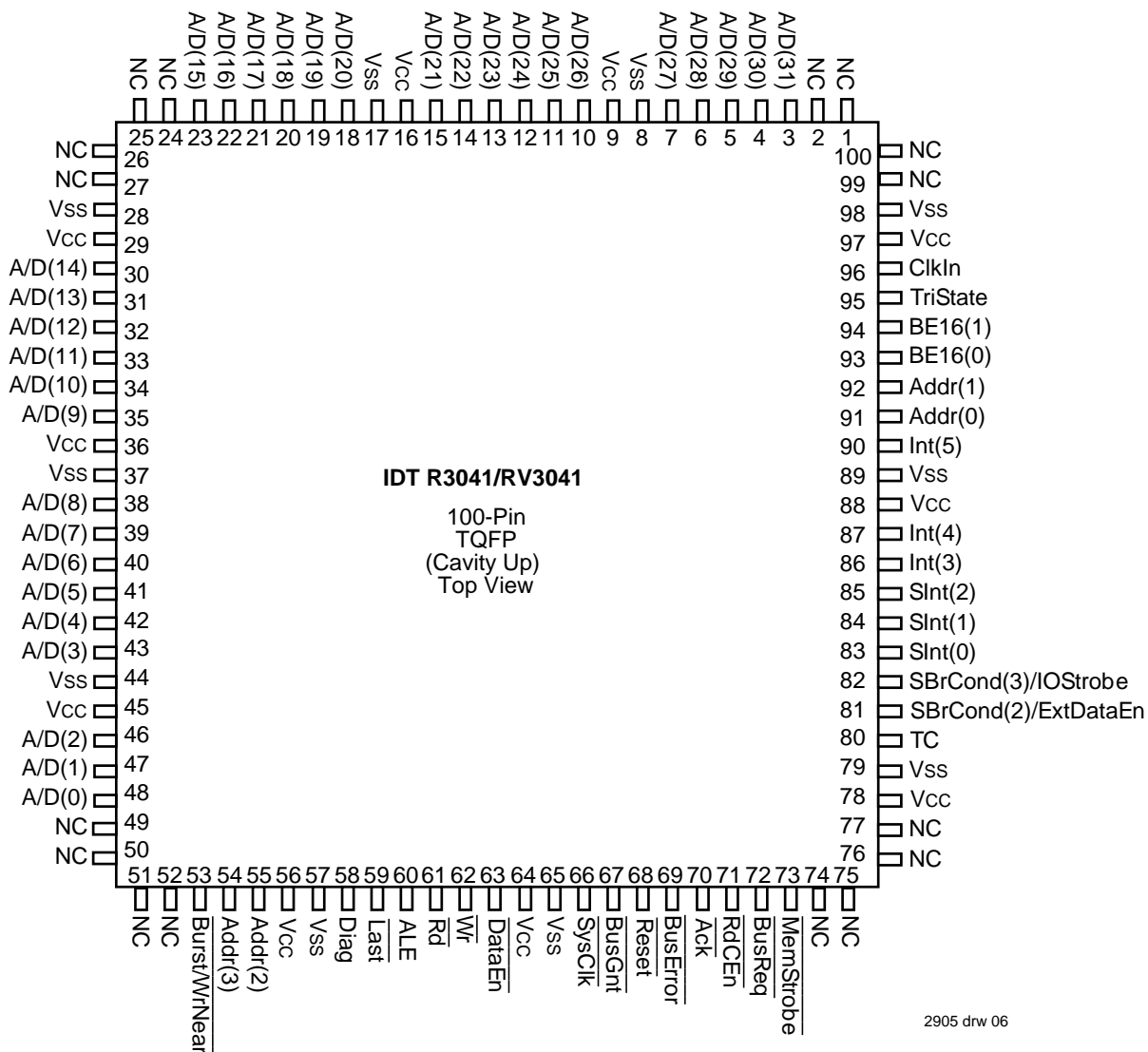
To minimize these AC parameters, the R3041 employs feedback from its SysClk output to the internal bus interface unit. This allows the R3041 to reference input signals to the reference clock seen by the external system. The SysClk output is designed to provide relatively large AC drive to minimize skew due to slow rise or fall times. A typical part will have less than 2ns rise or fall (10% to 90% signal times) when driving the test load.

Therefore, the system designer should use care when designing for direct SysClk use. Total loading (due to devices connected on the signal net and the routing of the net itself) should be minimized to ensure the SysClk output has a smooth and rapid transition. Long rise and/or fall times may cause a degradation in the speed capability of an individual device.

Similarly, the R3041 employs feedback on its ALE output to ensure adequate address hold time to ALE. The system designer should be careful when designing the ALE net to minimize total loading and to minimize skew between ALE and the A/D bus, which will ensure adequate address access latch time.

IDT's field and factory applications groups can provide the system designer with assistance for these and other design issues.

PIN CONFIGURATIONS



[illegible]

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PIN DESCRIPTION (Continued):

PIN NAME	I/O	DESCRIPTION
$\overline{\text{Burst/}}\text{WrNear}$	O	<p>Burst Transfer/Write Near: On read transactions, the $\overline{\text{Burst}}$ signal indicates that the current bus read is requesting a block of four contiguous words from memory. This signal is asserted only in read cycles due to cache misses; it is asserted for all I-Cache miss read cycles, and for D-Cache miss read cycles if the 4-word data block refill option is selected in the CP0 Cache Config Register.</p> <p>On write transactions, the $\overline{\text{WrNear}}$ output tells the external memory system that the bus interface unit is performing back-to-back write transactions to an address within the same 256 byte page as the prior write transaction. This signal is useful in memory systems which employ page mode or static column DRAMs, and allows nearby writes to be retired quickly.</p>
$\overline{\text{Rd}}$	O	Read: An output which indicates that the current bus transaction is a read.
$\overline{\text{Wr}}$	O	Write: An output which indicates that the current bus transaction is a write.
$\overline{\text{Ack}}$	I	Acknowledge: An input which indicates to the device that the memory system has sufficiently processed the bus transaction. On write transactions, this signal indicates that the CPU may either progress to the next data item (for mini-burst writes of wide datums to narrow memories), or terminate the write cycle. On read transactions, this signal indicates that the memory system has sufficiently processed the read, and that the processor core may begin processing the data from this read transfer.
$\overline{\text{RdCEn}}$	I	Read Buffer Clock Enable: An input which indicates to the device that the memory system has placed valid data on the A/D bus, and that the processor may move the data into the on-chip Read Buffer.
$\overline{\text{SysClk}}$	O	System Reference Clock: An output from the CPU which reflects the timing of the internal processor "System" clock. This clock is used to control state transitions in the read buffer, write buffer, memory controller, and bus interface unit.
$\overline{\text{BusReq}}$	I	DMA Arbiter Bus Request: An input to the device which requests that the CPU tri-state its bus interface signals so that they may be driven by an external master. The negation of this input relinquishes mastership back to the CPU.
$\overline{\text{BusGnt}}$	O	<p>DMA Arbiter Bus Grant. An output from the CPU used to acknowledge that a $\overline{\text{BusReq}}$ has been detected, and that the bus is relinquished to the external master.</p> <p>The R3041 adds an additional DMA protocol, under the control of CP0. If the DMA Protocol is enabled, the R3041 can request that the external master relinquish bus mastership back to the processor by negating the $\overline{\text{BusGnt}}$ output early, and waiting for the $\overline{\text{BusReq}}$ input to be negated.</p>
$\overline{\text{SBrCond(3)/}}\text{IOStrobe}$	I/O	<p>Branch Condition Port/IO Strobe: The use of this signal depends on the setting of various bits of the CP0 Bus Control register. If BrCond mode is selected, this input is logically connected to CpCond(3), and can be used by the branch on co-processor condition instructions as an input port. The SBrCond(3) input has special internal logic to synchronize the input, and thus may be driven by asynchronous agents.</p> <p>If this pin is selected to function as $\overline{\text{IOStrobe}}$, it may be asserted as an output on reads, writes, or both, as programmed into CP0. This strobe asserts in the second clock cycle of a transfer, and thus can be used to strobe various control signals on the bus interface.</p>
$\overline{\text{SBrCond(2)/}}\text{ExtDataEn}$	I/O	<p>Branch Condition Port/Extended Data Enable: The use of this signal depends on the settings in the CP0 Bus Control register. If BrCond mode is selected, this input is logically connected to CpCond(2), and can be used by the branch on co-processor condition instructions as an input port. The SBrCond(2) input has special internal logic to synchronize the input, and thus may be driven by asynchronous agents.</p> <p>If this pin is selected to function as Extended Data Enable, it may be asserted as an output on reads, writes, or both, as programmed into CP0. This strobe can be used as an extended data enable strobe, in that it is held asserted for one-half clock cycle after the negation of $\overline{\text{Rd}}$ or $\overline{\text{Wr}}$. This signal may typically be used as a write enable control line for transceivers, as a write line for I/O, or as an address mux select for DRAMs.</p>
$\overline{\text{MemStrobe}}$	O	<p>Memory Strobe: This active low output pulses low for each data read or written, as configured in the CP0 Bus Control register. Thus, it can be used as a read strobe, write strobe, or both, for SRAM type memories or for I/O devices.</p> <p>The R3041 $\overline{\text{MemStrobe}}$ output pin is designated as the BrCond(0) input pin in the R3051 and R3081.</p>

PIN DESCRIPTION (Continued):

PIN NAME	I/O	DESCRIPTION
$\overline{\text{BE16(1:0)}}$	O I ⁽¹⁾	<p>Byte Enable Strokes for 16-bit Memory Port: These active low outputs are the byte lane strobes for accesses to 16-bit wide memory ports; they are not necessarily valid for 8- or 32-bit wide ports. If $\overline{\text{BE16(1)}}$ is asserted, then the most significant byte (either D(31:24) or D(15:8), depending on system endianness) is going to be used in this transfer. If $\overline{\text{BE16(0)}}$ is asserted, the least significant byte (D(23:16) or D(7:0)) will be used.</p> <p>$\overline{\text{BE16(1:0)}}$ can be held inactive (masked) during read transfers, according to the programming of the CP0 Bus Control register.</p> <p>During $\overline{\text{Reset}}$, the $\overline{\text{BE16(1:0)}}$ act as Reset Configuration Mode bit inputs for two ReservedHigh options. The $\overline{\text{BE16(1:0)}}$ output pins are designated as the unconnected Rsvd(3:2) pins in the R3051 and R3081.</p>
$\overline{\text{Last}}$	O	<p>Last Datum in Mini-Burst: This active low output indicates that this is the last datum transfer in a given transaction. It is asserted after the next to last $\overline{\text{RdCEn}}$ (reads) or $\overline{\text{Ack}}$ (writes), and is negated when $\overline{\text{Rd}}$ or $\overline{\text{Wr}}$ is negated.</p> <p>The $\overline{\text{Last}}$ output pin is designated in the R3051 and R3081 as the Diag(0) output pin.</p>
$\overline{\text{TC}}$	O	<p>Terminal Count: This is an active low output from the processor which indicates that the on-chip timer has reached its terminal count. It will remain low for either 1.5 clock cycles, or until software resets the timer, depending on the mode selected in the CP0 Bus Control register. Thus, the on-chip timer can function either as a free running timer for system functions such as DRAM refresh, or can operate as a software controlled time-slice timer, or real-time clock.</p> <p>The $\overline{\text{TC}}$ output pin is designated in the R3051 as the BrCond(1) input pin, and in the R3081 as the Run pin output.</p>
$\overline{\text{BusError}}$	I	<p>Bus Error: Input to the bus interface unit to terminate a bus transaction due to an external bus error. This signal is only sampled during read and write operations. If the bus transaction is a read operation, then the CPU will take a bus error exception.</p>
$\overline{\text{Int(5:3)}}$ $\overline{\text{SInt(2:0)}}$	I I ⁽¹⁾	<p>Processor Interrupt: During normal operation, these signals are logically the same as the $\overline{\text{Int(5:0)}}$ signals of the R3000A. During processor reset, these signals perform mode initialization of the CPU, but in a different (simpler) fashion than the interrupt signals on the original R3000A.</p> <p>During $\overline{\text{Reset}}$, $\overline{\text{Int(3)}}$ and $\overline{\text{SInt(0)}}$ act as Reset Configuration Mode bit inputs for the AddrDisplayAndForceCacheMiss and BigEndian options.</p> <p>There are two types of interrupt inputs: the $\overline{\text{SInt}}$ inputs are internally synchronized by the processor, and may be driven by an asynchronous external agent. The direct interrupt inputs are not internally synchronized, and thus must be externally synchronized to the CPU. The direct interrupt inputs have one cycle lower latency than the synchronized interrupts.</p>
$\overline{\text{ClkIn}}$	I	<p>Master Clock Input: This is a double frequency input used to control the timing of the CPU.</p>
$\overline{\text{Reset}}$	I	<p>Master Processor Reset: This signal initializes the CPU. Reset initialization mode selection is performed during the last cycle of $\overline{\text{Reset}}$.</p>
$\overline{\text{TriState}}$	I	<p>Tri-State: This input to the R3041 requests that the R3041 tri-state all of its outputs. In addition to those outputs tri-stated during DMA, tri-state will cause $\overline{\text{SysClk}}$, $\overline{\text{TC}}$, and $\overline{\text{BusGnt}}$ to tri-state. This signal is intended for use during board testing and emulation during debug and board manufacture.</p> <p>The $\overline{\text{TriState}}$ input pin is designated as the unconnected Rsvd(4)pin in the R3051 and R3081.</p>
Vcc	I	<p>Power: These inputs must be supplied with the rated supply voltage (VCC). All Vcc inputs must be connected to insure proper operation.</p>
Vss	I	<p>Ground: These inputs must be connected to ground (GND). All Vss inputs must be connected to insure proper operation.</p>

NOTE:

1. Reset Configuration Mode bit input when $\overline{\text{Reset}}$ is asserted, normal signal function when $\overline{\text{Reset}}$ is de-asserted.

2905 tbl 05

AC ELECTRICAL CHARACTERISTICS R3041 ^(1, 2, 3) — (T_C = 0°C to +85°C, V_{CC} = +5.0V ±5%)

Symbol	Signals	Description	16.67MHz		20MHz		25MHz		33MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t1	BusReq, Ack, BusError, RdCEn	Set-up to SysClk rising	11	—	8	—	5.5	—	5.5	—	ns
t1a	A/D	Set-up to SysClk falling	12	—	9	—	7	—	7	—	ns
t2	BusReq, Ack, BusError, RdCEn	Hold from SysClk rising	4	—	3	—	2.5	—	2.5	—	ns
t2a	A/D	Hold from SysClk falling	2	—	2	—	1	—	1	—	ns
t3	A/D, Addr, Diag, ALE, Wr Burst/WrNear, Rd, DataEn	Tri-state from SysClk rising (after driven condition)	—	13	—	10	—	10	—	10	ns
t4	A/D, Addr, Diag, ALE, Wr Burst/WrNear, Rd, DataEn	Driven from SysClk falling (after tri-state condition)	—	13	—	10	—	10	—	10	ns
t5	BusGnt	Asserted from SysClk rising	—	10	—	8	—	7	—	7	ns
t6	BusGnt	Negated from SysClk falling	—	10	—	8	—	7	—	7	ns
t7	Wr, Rd, Burst/WrNear, TC	Valid from SysClk rising	—	8	—	6	—	5	—	5	ns
t7a	A/D	Valid from SysClk rising	—	12	—	9	—	8	—	8	ns
t7b	Last	Valid from SysClk rising	—	12	—	9	—	8	—	8	ns
t8	ALE	Asserted from SysClk rising	—	5	—	4	—	4	—	4	ns
t9	ALE	Negated from SysClk falling	—	5	—	4	—	4	—	4	ns
t10	A/D	Hold from ALE negated	2	—	2	—	2	—	1.5	—	ns
t11	DataEn	Asserted from SysClk	—	19	—	15	—	15	—	15	ns
t12	DataEn	Asserted from A/D tri-state ⁽⁴⁾	0	—	0	—	0	—	0	—	ns
t14	A/D	Driven from SysClk rising ⁽⁴⁾	0	—	0	—	0	—	0	—	ns
t15	Wr, Rd, DataEn, Burst/WrNear, Last, TC	Negated from SysClk falling	—	9	—	7	—	6	—	6	ns
t16	Addr(3:0), BE 16(1:0)	Valid from SysClk	—	11	—	8	—	7	—	7	ns
t17	Diag	Valid from SysClk	—	15	—	12	—	11	—	11	ns
t18	A/D	Tri-state from SysClk	—	13	—	10	—	10	—	10	ns
t19	A/D	SysClk to data out	—	16	—	13	—	12	—	12	ns
t20	ClkIn	Pulse Width High	12	—	10	—	8	—	6.5	—	ns
t21	ClkIn	Pulse Width Low	12	—	10	—	8	—	6.5	—	ns
t22	ClkIn	Clock Period	30	250	25	250	20	250	15	250	ns
t23	Reset	Pulse Width from Vcc valid	200	—	200	—	200	—	200	—	μs
t24	Reset	Minimum Pulse Width	32	—	32	—	32	—	32	—	sys
t25	Reset	Set-up to SysClk falling	8	—	6	—	5	—	5	—	ns
t26	Int	Mode set-up to Reset rising	8	—	6	—	5	—	5	—	ns
t27	Int	Mode hold from Reset rising	2.5	—	2.5	—	2.5	—	2.5	—	ns
t28	Slnt, SBrCond	Set-up to SysClk falling	8	—	6	—	5	—	5	—	ns
t29	Slnt, SBrCond	Hold from SysClk falling	4	—	3	—	3	—	3	—	ns
t30	Int, BrCond	Set-up to SysClk falling	8	—	6	—	5	—	5	—	ns
t31	Int, BrCond	Hold from SysClk falling	4	—	3	—	3	—	3	—	ns
tsys	SysClk	Pulse Width	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	ns
t32	SysClk	Clock High Time	t22 - 2	t22 + 2	t22 - 2	t22 + 2	t22 - 2	t22 + 2	t22 - 2	t22 + 2	ns
t33	SysClk	Clock Low Time	t22 - 2	t22 + 2	t22 - 2	t22 + 2	t22 - 2	t22 + 2	t22 - 2	t22 + 2	ns

2905 tbl 11

AC ELECTRICAL CHARACTERISTICS R3041 (CONT.)

Symbol	Signals	Description	16.67MHz		20MHz		25MHz		33MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t45	ExtDataEn	Tri-state from SysClk rising (after driven condition)	—	13	—	10	—	10	—	10	ns
t46	ExtDataEn	Driven from SysClk falling (after driven condition)	—	13	—	10	—	10	—	10	ns
t47	IOStrobe	Valid from SysClk falling	—	10	—	8	—	7	—	7	ns
t48	ExtDataEn, DataEn	Asserted from SysClk rising	—	15	—	12	—	9	—	9	ns
t49	ExtDataEn	Negated from SysClk rising	—	9	—	7	—	6	—	6	ns
t50	MemStrobe	Asserted from SysClk rising	—	19	—	15	—	15	—	15	ns
t51	MemStrobe	Negated from SysClk falling	—	19	—	15	—	15	—	15	ns
t52	MemStrobe	Asserted from Addr(3:0) valid ⁽⁴⁾	0	—	0	—	0	—	0	—	ns
tderate	All outputs	Timing deration for loading over 25pF ^(4, 5)	—	0.5	—	0.5	—	0.5	—	0.5	ns/ 25pF

NOTES:

2905 tbl 12

1. All timings referenced to 1.5 Volts, with a rise and fall time of less than 2.5ns.
2. All outputs tested with 25pF loading.
3. The AC values listed here reference timing diagrams contained in the R3041 Hardware User's Manual.
4. Guaranteed by design.
5. This parameter is used to derate the AC timings according to the loading of the system. This parameter provides a deration for loads over the specified test condition; that is, the deration factor is applied for each 25pF over the specified test load condition.
6. Timings t34 - t44 are reserved for other RISController family members.

ABSOLUTE MAXIMUM RATINGS^(1, 3) RV3041

Symbol	Rating	Commercial	Unit
VTERM	Terminal Voltage with Respect to GND	−0.5 to +7.0	V
Tc	Operating Case Temperature	0 to +85	°C
TBIAS	Temperature Under Bias	−55 to +125	°C
TSTG	Storage Temperature	−55 to +125	°C
VIN	Input Voltage	−0.5 to +7.0	V

NOTES:

2905 tbl 06

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VIN minimum = −3.0V for pulse width less than 15ns. VIN should not exceed VCC +0.5 Volts.
3. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

AC TEST CONDITIONS RV3041

Symbol	Parameter	Min.	Max.	Unit
VIH	Input HIGH Voltage	3.0	—	V
VIL	Input LOW Voltage	—	0	V
VIHS	Input HIGH Voltage	3.0	—	V
VILS	Input LOW Voltage	—	0	V

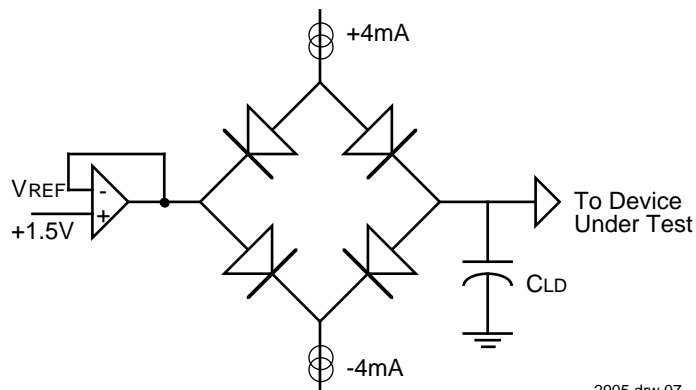
2905 tbl 08

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Commercial RV3041	0°C to +85°C (Case)	0V	3.3 ±5%

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OUTPUT LOADING FOR AC TESTING



2905 drw 07

Signal	Cld
All Signals	25 pF

2905 tbl 09

DC ELECTRICAL CHARACTERISTICS RV3041 — ($T_C = 0^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = +3.3\text{V} \pm 5\%$)

Symbol	Parameter	Test Conditions	16.67MHz		20MHz		25MHz		33MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4\text{mA}$	2.4	—	2.4	—	2.4	—	2.4	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 4\text{mA}$	—	0.4	—	0.4	—	0.4	—	0.4	V
V_{IH}	Input HIGH Voltage ⁽³⁾	—	2.0	—	2.0	—	2.0	—	2.0	—	V
V_{IL}	Input LOW Voltage ⁽¹⁾	—	—	0.8	—	0.8	—	0.8	—	0.8	V
V_{IHS}	Input HIGH Voltage ^(2,3)	—	2.5	—	2.5	—	2.5	—	2.5	—	V
V_{ILS}	Input LOW Voltage ^(1,2)	—	—	0.4	—	0.4	—	0.4	—	0.4	V
C_{IN}	Input Capacitance ⁽⁴⁾	—	—	10	—	10	—	10	—	10	pF
C_{OUT}	Output Capacitance ⁽⁴⁾	—	—	10	—	10	—	10	—	10	pF
I_{CC}	Operating Current	$V_{CC} = 3.3\text{V}, T_C = 25^\circ\text{C}$	—	130	—	150	—	180	—	225	mA
I_{IH}	Input HIGH Leakage	$V_{IH} = V_{CC}$	—	100	—	100	—	100	—	100	mA
I_{IL}	Input LOW Leakage	$V_{IL} = \text{GND}$	-100	—	-100	—	-100	—	-100	—	mA
I_{OZ}	Output Tri-state Leakage	$V_{OH} = 2.4\text{V}, V_{OL} = 0.5\text{V}$	-100	100	-100	100	-100	100	-100	100	mA

NOTES:

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1. V_{IL} Min. = -3.0V for pulse width less than 15ns. V_{IL} should not fall below -0.5 volts for larger periods.
2. V_{IHS} and V_{ILS} apply to ClkIn and Reset .
3. V_{IH} should not be held above $V_{CC} + 0.5$ volts.
4. Guaranteed by design.

AC ELECTRICAL CHARACTERISTICS RV3041 (1, 2, 3) — ($T_C = 0^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = +3.3\text{V} \pm 5\%$)

Symbol	Signals	Description	16.67MHz		20MHz		25MHz		33MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t1	BusReq, Ack, BusError, RdCEn	Set-up to SysClk rising	11	—	8	—	5.5	—	5.5	—	ns
t1a	A/D	Set-up to SysClk falling	12	—	9	—	7	—	7	—	ns
t2	BusReq, Ack, BusError, RdCEn	Hold from SysClk rising	4	—	3	—	2.5	—	2.5	—	ns
t2a	A/D	Hold from SysClk falling	2	—	2	—	1	—	1	—	ns
t3	A/D, Addr, Diag, ALE, Wr Burst/WrNear, Rd, DataEn	Tri-state from SysClk rising (after driven condition)	—	13	—	10	—	10	—	10	ns
t4	A/D, Addr, Diag, ALE, Wr Burst/WrNear, Rd, DataEn	Driven from SysClk falling (after tri-state condition)	—	13	—	10	—	10	—	10	ns
t5	BusGnt	Asserted from SysClk rising	—	10	—	8	—	7	—	7	ns
t6	BusGnt	Negated from SysClk falling	—	10	—	8	—	7	—	7	ns
t7	Wr, Rd, Burst/WrNear, TC	Valid from SysClk rising	—	8	—	6	—	5	—	5	ns
t7a	A/D	Valid from SysClk rising	—	12	—	9	—	8	—	8	ns
t7b	Last	Valid from SysClk rising	—	12	—	9	—	8	—	8	ns
t8	ALE	Asserted from SysClk rising	—	5	—	4	—	4	—	4	ns
t9	ALE	Negated from SysClk falling	—	5	—	4	—	4	—	4	ns
t10	A/D	Hold from ALE negated	2	—	2	—	2	—	1.5	—	ns
t11	DataEn	Asserted from SysClk	—	19	—	15	—	15	—	15	ns
t12	DataEn	Asserted from A/D tri-state ⁽⁴⁾	0	—	0	—	0	—	0	—	ns
t14	A/D	Driven from SysClk rising ⁽⁴⁾	0	—	0	—	0	—	0	—	ns
t15	Wr, Rd, DataEn, Burst/WrNear, Last, TC	Negated from SysClk falling	—	9	—	7	—	6	—	6	ns
t16	Addr(3:0), BE 16(1:0)	Valid from SysClk	—	11	—	8	—	7	—	7	ns
t17	Diag	Valid from SysClk	—	15	—	12	—	11	—	11	ns

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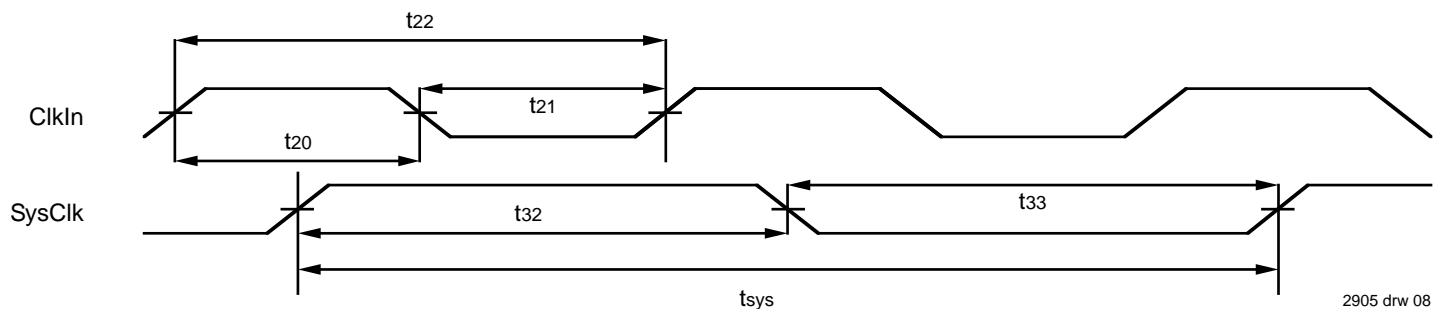


Figure 8. RISController Family Clocking

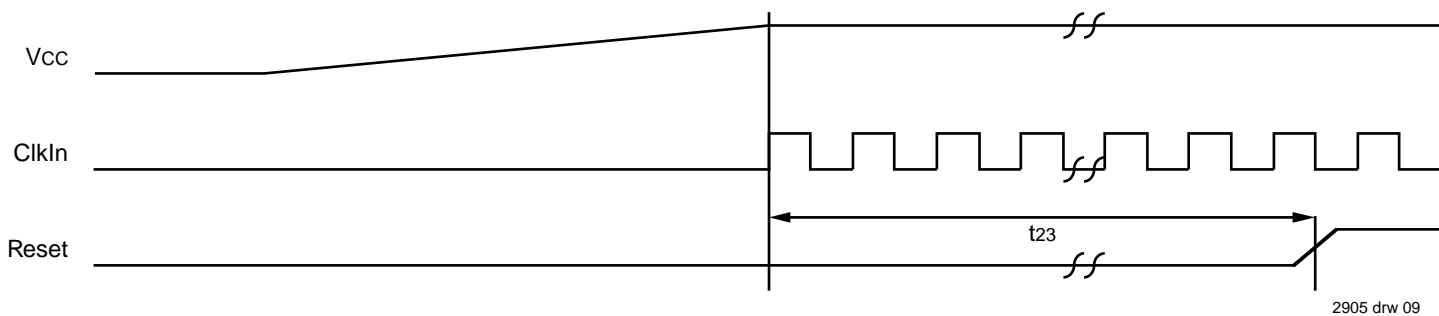


Figure 9. Power-On Reset Sequence

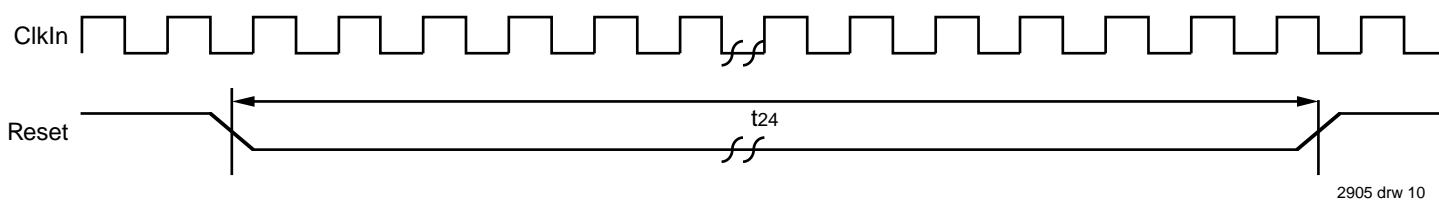


Figure 10(a). Warm Reset Sequence

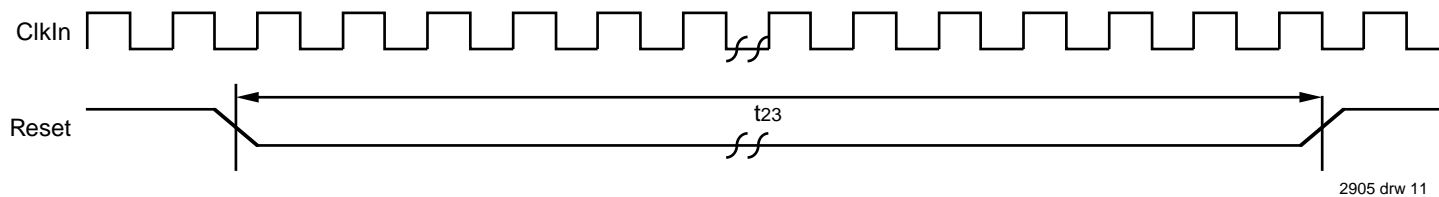


Figure 10(b). Warm Reset Sequence (Internal Pull-Ups Used)

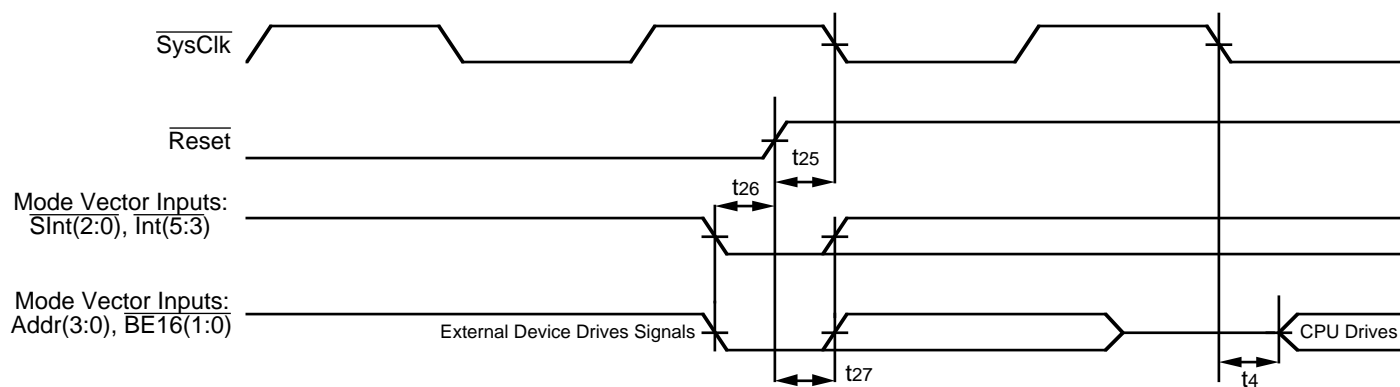


Figure 11. Mode Selection and Negation of Reset

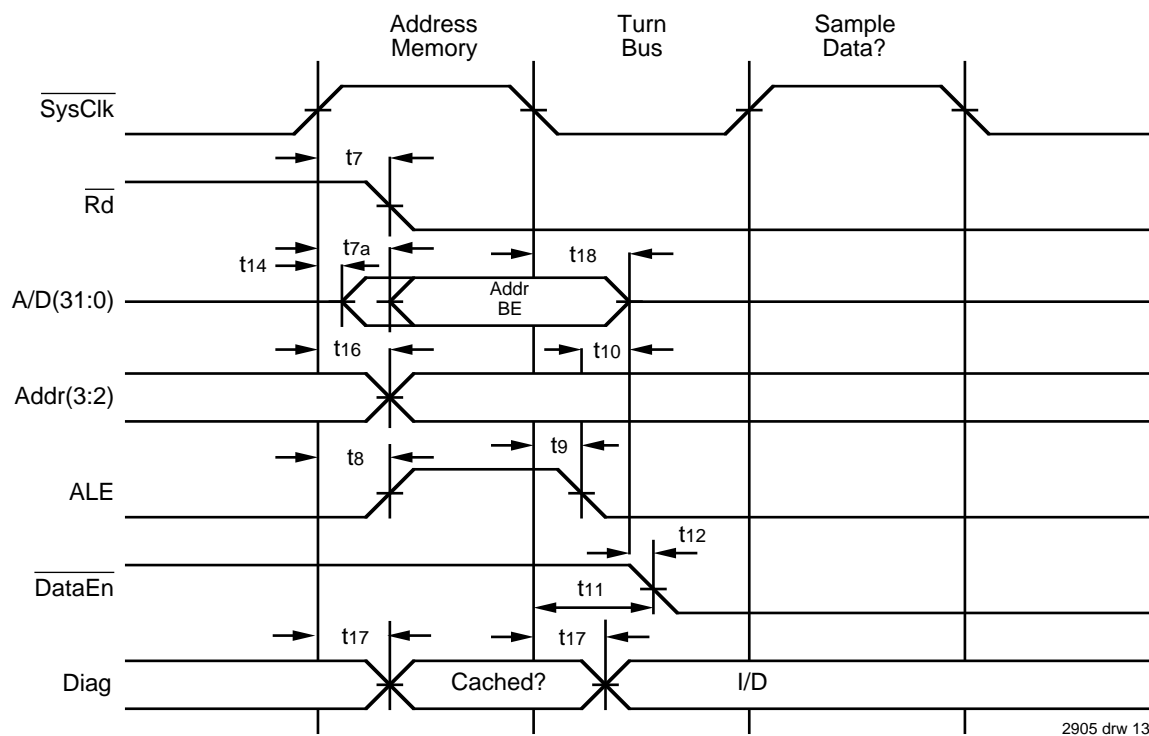


Figure 12(a). Start of Read Timing with Non-Extended Address Hold Option

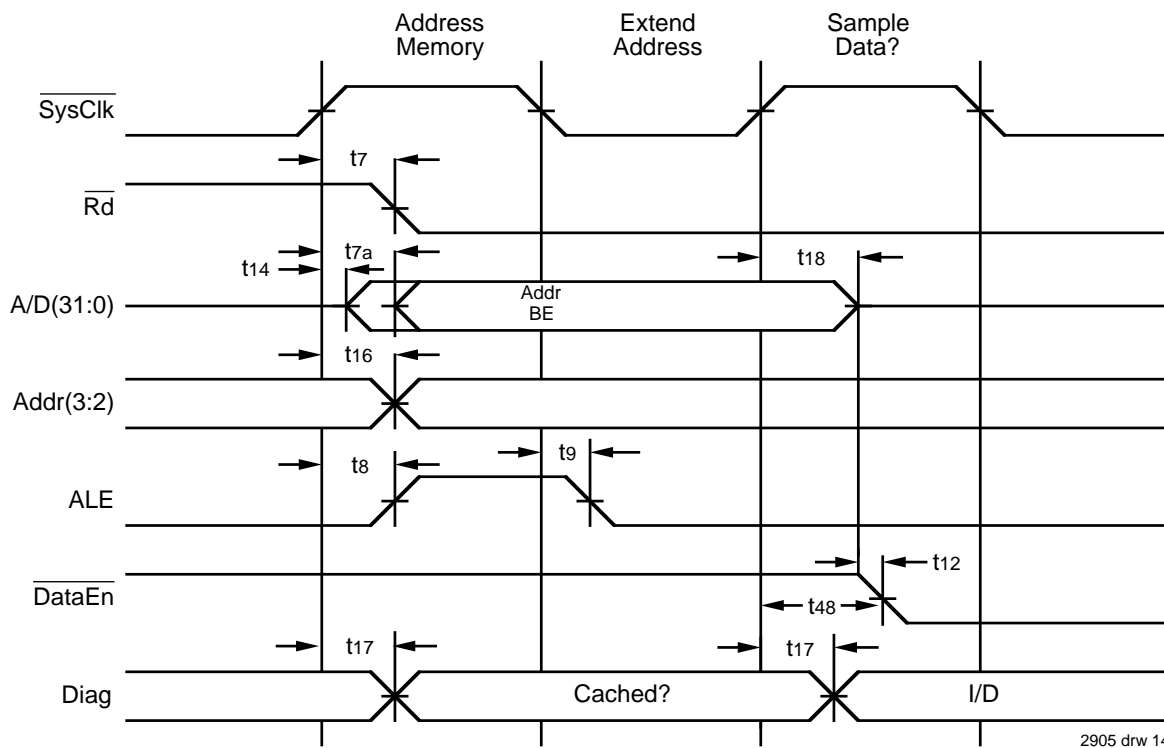
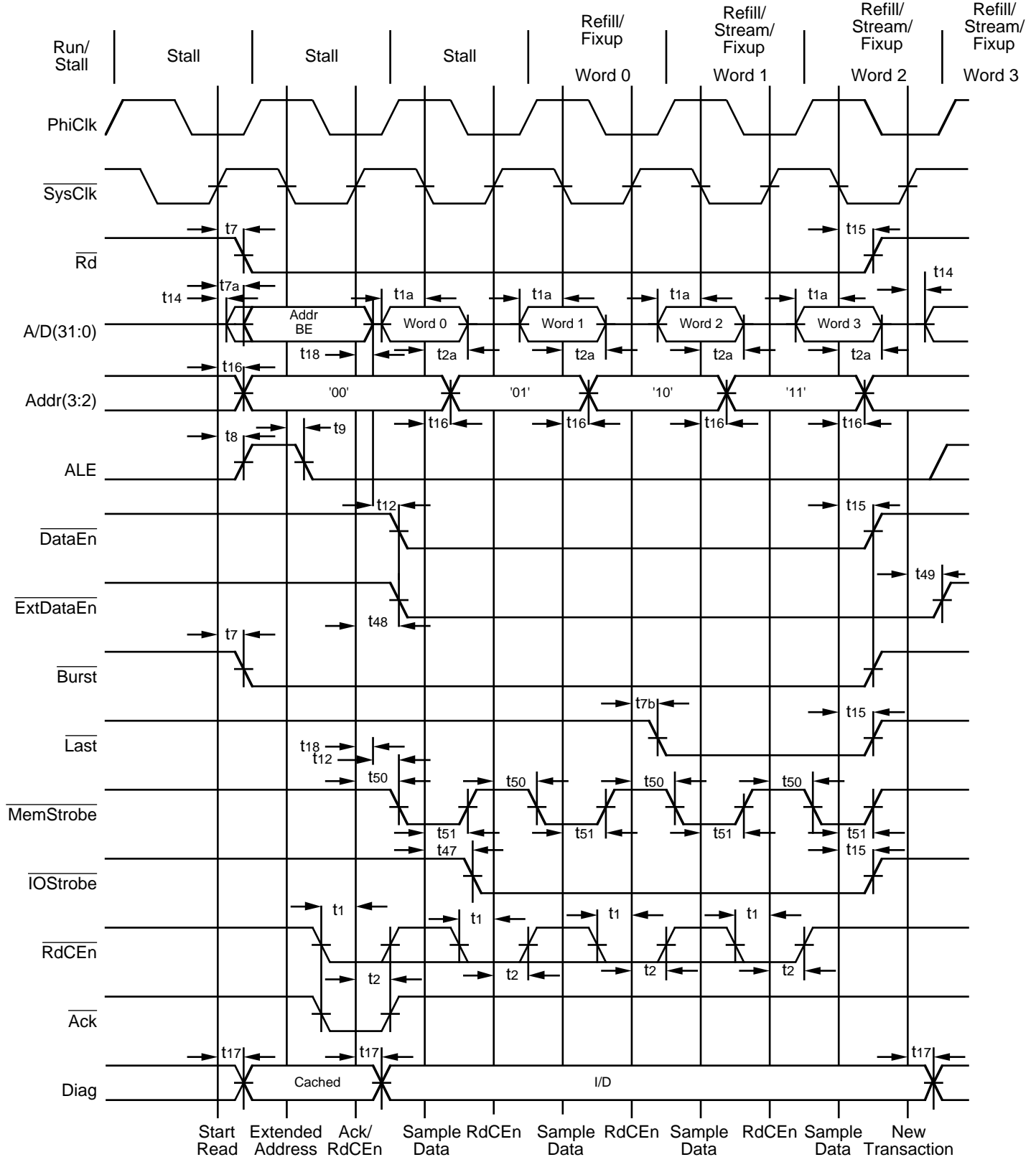


Figure 12(b). Start of Read Timing with Extended Address Hold Option



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Figure 15. R3041 Quad Word Read

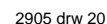
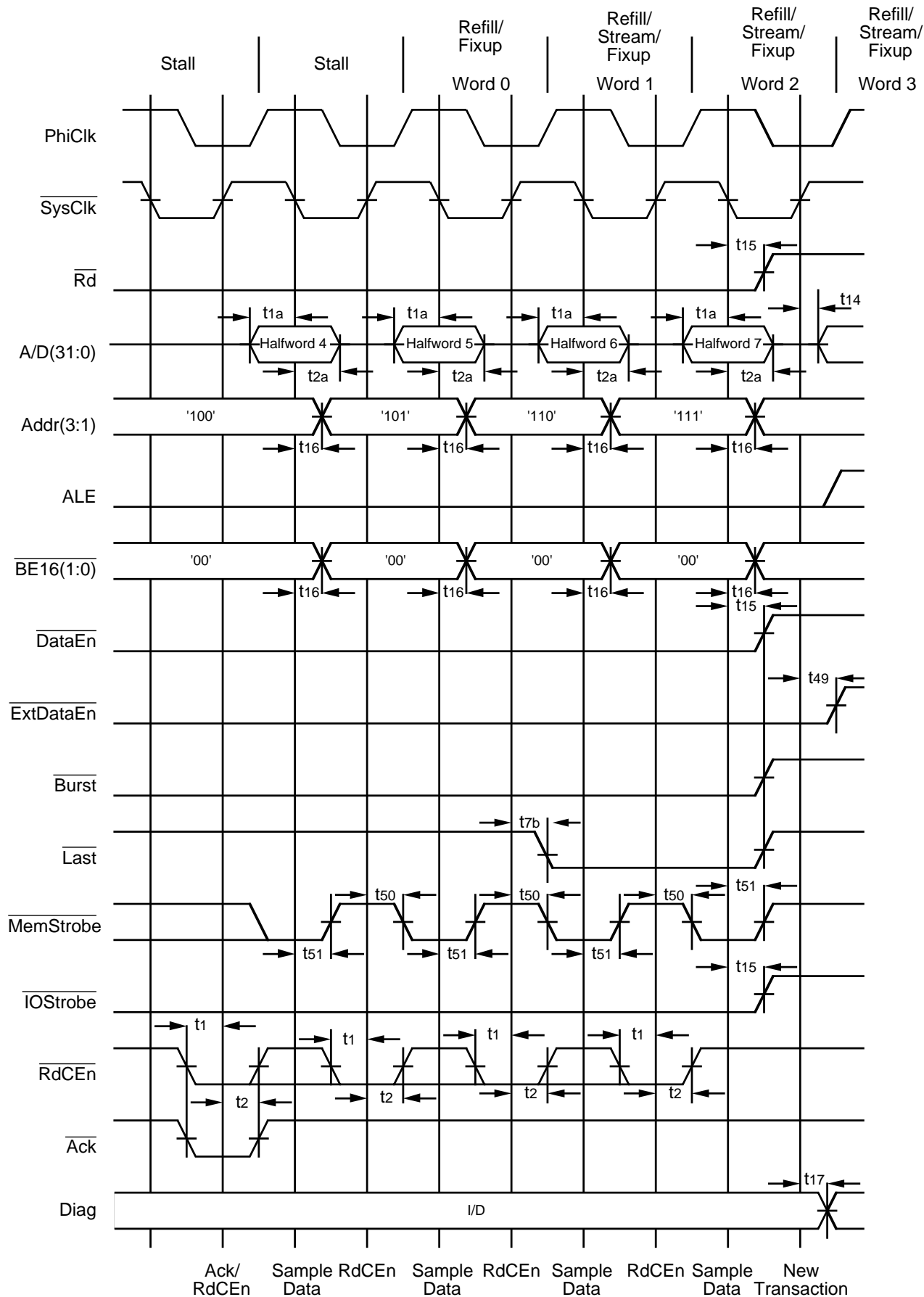
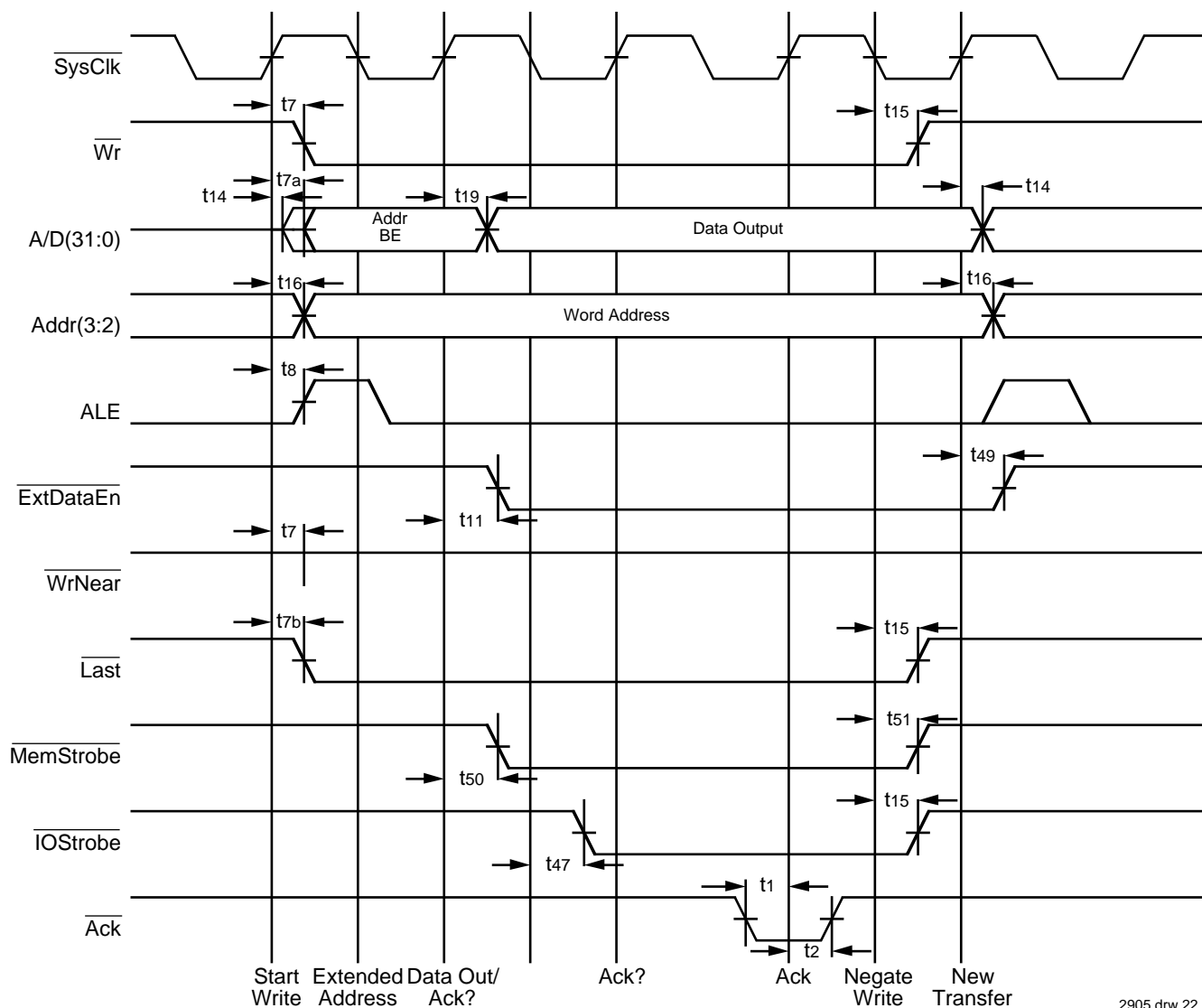


Figure 16(a). Quad Word Read to 16-bit wide Memory Port



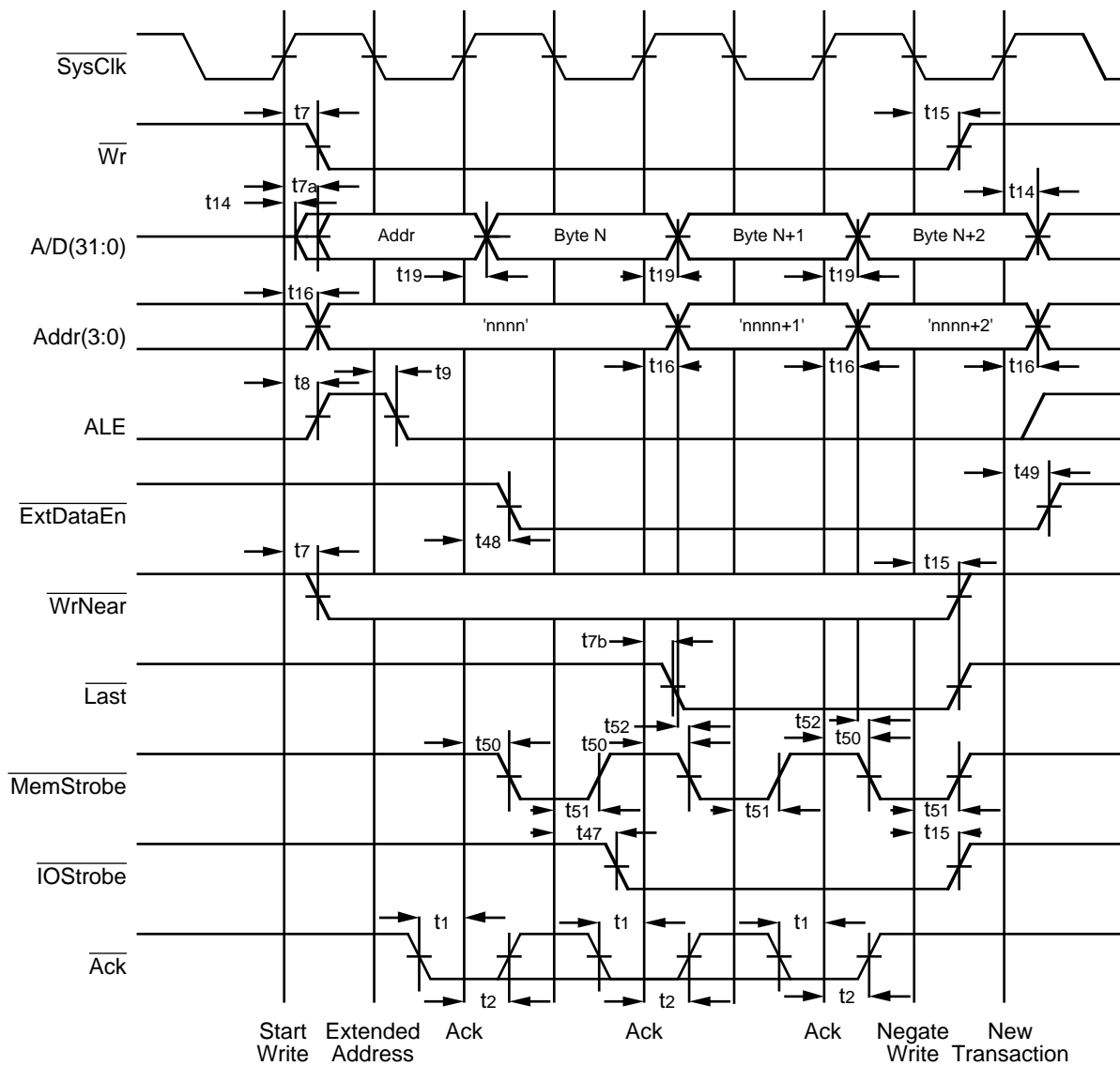
2905 drw 21

Figure 16(b). End of Quad Word read from 16-bit Wide Memory Port



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Figure 17. Basic Write to 32-bit Memory Port



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Figure 18. Tri-Byte Mini-burst Write to 8-bit Port

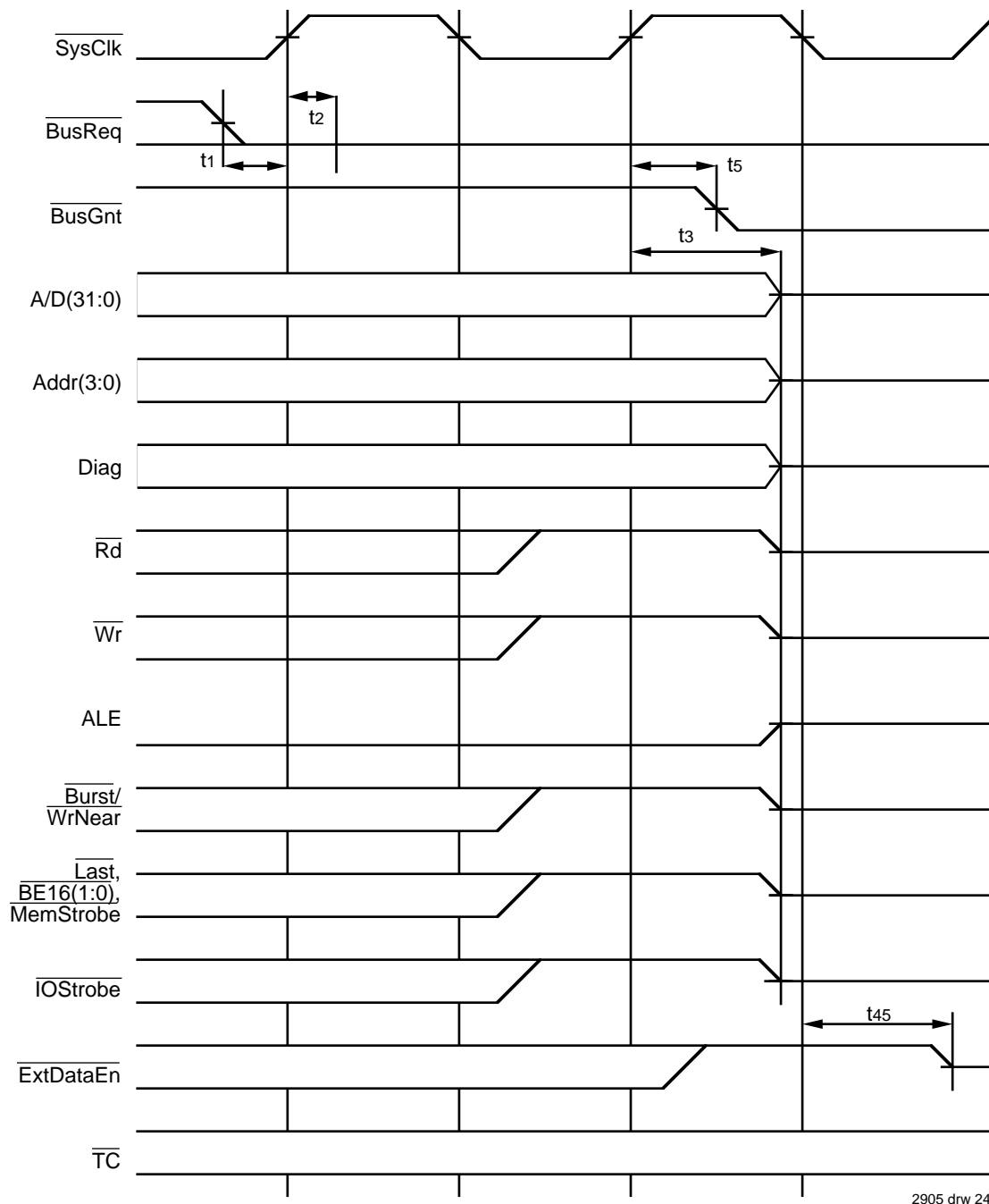


Figure 19. Request and Relinquish of R3041 Bus to External Master

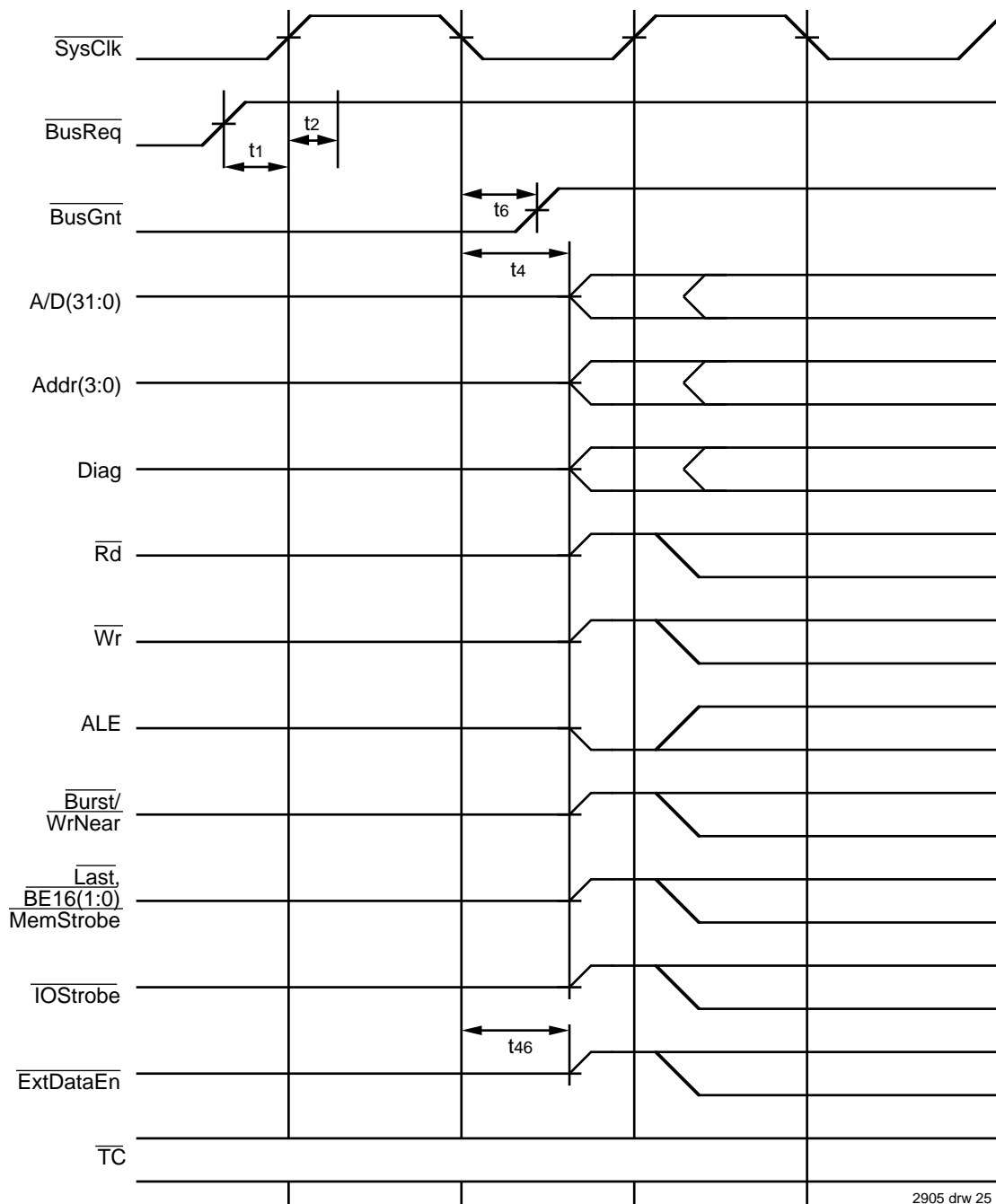


Figure 20. R3041 Regaining Bus Mastership