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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

XF

Obsolete
MIPS-I
1 Core, 32-Bit
25MHz
System Control; CP0
DRAM
No
-
-
-
-
5.0V
0°C ~ 85°C (TC)
-
100-LQFP
100-TQFP (14x14)
https://www.e-xfl.com/product-detail/renesas-electronics-america/idt79r3041-25pf8

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

System Control Co-Processor

The R3041 also integrates on-chip a System Control Coprocessor, CP0. CP0 manages the exception handling capability of the R3041, the virtual to physical address mapping of the R3041, and the programmable bus interface capabilities of the R3041. These topics are discussed in subsequent sections.

The R3041 does not include the optional TLB found in other members of the RISController family, but instead performs the same virtual to physical address mapping of the base version of the RISController family. These devices still support distinct kernel and user mode operation, but do not require page management software or an on-chip TLB, leading to a simpler software model and a lower-cost processor.

The memory mapping used by these devices is illustrated in Figure 3. Note that the reserved address spaces shown are for compatibility with future family members; in the current family members, references to these addresses are translated in the same fashion as their respective segments, with no traps or exceptions taken.

When using the base versions of the architecture, the system designer can implement a distinction between the user tasks and the kernel tasks, without having to execute page management software. This distinction can take the form of physical memory protection, accomplished by address decoding, or in other system specific forms. In systems which do not wish to implement memory protection, and wish to have the kernel and user tasks operate out of a single unified memory space, upper address lines can be ignored by the address decoder, and thus all references will be seen in the lower gigabyte of the physical address space.

The R3041 adds additional resources into the on-chip CP0. These resources are detailed in the R3041 User's Manual. They allow kernel software to directly control activity of the processor internal resources and bus interface, and include:

- Cache Configuration Register: This register controls the data cache block size and miss refill algorithm.
- Bus Control Register: This register controls the behavior of the various bus interface signals.
- Count and Compare Registers: Together, these two registers implement a programmable 24-bit timer, which can be used for DRAM refresh or as a general purpose timer.
- **Port Size Control Register:** This register allows the kernel to indicate the port width of reads and writes to various sub-regions of the physical address space. Thus, the R3041 can interface directly with 8-, 16-, and 32-bit memory ports, including a mix of sizes, for both instruction and data references, without requiring additional external logic.



VIRTUAL

PHYSICAL

Figure 3. Virtual to Physical Mapping of Base Architecture Versions

Clock Generation Unit

The R3041 is driven from a single 2x frequency input clock, capable of operating in a range of 40%-60% duty cycle. Onchip, the clock generator unit is responsible for managing the interaction of the CPU core, caches, and bus interface. The clock generator unit replaces the external delay line required in R3000A based applications.

Instruction Cache

The R3041 integrates 2kB of on-chip Instruction Cache, organized with a line size of 16 bytes (four 32-bit entries) and is direct mapped. This relatively large cache substantially contributes to the performance inherent in the R3041, and allows systems based on the R3041 to achieve high-performance even from low-cost memory systems. The cache is implemented as a direct mapped cache, and is capable of caching instructions from anywhere within the 4GB physical addresses and physical tags (rather than virtual addresses or tags), and thus does not require flushing on context switch.

Data Cache

The R3041 incorporates an on-chip data cache of 512B, organized as a line size of 4 bytes (one word) and is direct mapped. This relatively large data cache contributes substantially to the performance inherent in the RISController family. As with the instruction cache, the data cache is implemented as a direct mapped physical address cache. The cache is capable of mapping any word within the 4GB physical address space.

The data cache is implemented as a write through cache, to insure that main memory is always consistent with the internal cache. In order to minimize processor stalls due to data write operations, the bus interface unit incorporates a 4deep write buffer which captures address and data at the processor execution rate, allowing it to be retired to main memory at a much slower rate without impacting system performance.

Bus Interface Unit

The RISController family uses its large internal caches to provide the majority of the bandwidth requirements of the execution engine, and thus can utilize a simple bus interface connected to slow memory devices.

The RISController family bus interface utilizes a 32-bit address and data bus multiplexed onto a single set of pins. The bus interface unit also provides an ALE (Address Latch Enable) output signal to de-multiplex the A/D bus, and simple handshake signals to process CPU read and write requests. In addition to the read and write interface, the R3041 incorporates a DMA arbiter, to allow an external master to control the external bus.

The R3041 augments the basic RISController bus interface capability by adding the ability to directly interface with varying memory port widths, for instructions or data. For example, the R3041 can be used in a system with an 8-bit boot PROM, 16-bit font/program cartridges, and 32-bit main memory, transparently to software, and without requiring external data packing, rotation, and unpacking.

In addition, the R3041 incorporates the ability to change some of the interface timing of the bus. These features can be used to eliminate external data buffers and take advantage of lower speed and lower cost interface components.

One of the bus interface options is the Extended Address Hold mode which adds 1/2 clock of extra address hold time from ALE falling. This allows easier interfacing to FPGAs and ASICs.

The R3041 incorporates a 4-deep write buffer to decouple the speed of the execution engine from the speed of the memory system. The write buffers capture and FIFO processor address and data information in store operations, and present it to the bus interface as write transactions at the rate the memory system can accommodate. During main memory writes, the R3041 can break a large datum (e.g. 32-bit word) into a series of smaller transactions (e.g. bytes), according to the width of the memory port being written. This operation is transparent to the software which initiated the store, insuring that the same software can run in true 32-bit memory systems.

The RISController family read interface performs both single word reads and quad word reads. Single word reads work with a simple handshake, and quad word reads can either utilize the simple handshake (in lower performance, simple systems) or utilize a tighter timing mode when the memory system can burst data at the processor clock rate. Thus, the system designer can choose to use page or static column mode DRAMs (and possibly use interleaving, if desired, in high-performance systems), or even to use simpler SRAM techniques to reduce complexity.

In order to accommodate slower quad word reads, the RISController family incorporates a 4-deep read buffer FIFO, so that the external interface can queue up data within the processor before releasing it to perform a burst fill of the internal caches.

In addition, the R3041 can perform on-chip data packing when performing large datum reads (e.g., quad words) from narrower memory systems (e.g., 16-bits). Once again, this operation is transparent to the actual software, simplifying migration of software to higher performance (true 32-bit) systems, and simplifying field upgrades to wider memory. Since this capability works for either instruction or data reads, using 8-, 16-, or 32-bit boot PROMs is easily supported by the R3041.

SYSTEM USAGE

The IDT RISController family is specifically designed to easily connect to low-cost memory systems. Typical low-cost memory systems use inexpensive EPROMs, DRAMs, and application specific peripherals.

Figure 4 shows some of the flexibility inherent in the R3041. In this example system, which is typical of a laser printer, a 32bit PROM interface is used due to the size of the PDL interpreter. An embedded system can optionally use an 8-bit boot PROM instead. A 16-bit font/program cartridge interface is provided for add-in cards. A 16-bit DRAM interface is used for a low-cost page frame buffer. In this system example, a field or manufacturing upgrade to a 32-bit page frame buffer is supported by the boot software and DRAM controller. Embedded systems may optionally substitute SRAMs for the DRAMs. Finally various 8/16/32-bit I/O ports such as RS-232/ 422, SCSI, and LAN as well as the laser printer engine interface are supported. Such a system features a very low entry price, with a range of field upgrade options including the ability to upgrade to a more powerful member of the RISController family.



Figure 4. Typical R3041-Based Application

DEVELOPMENT SUPPORT

The IDT RISController family is supported by a rich set of development tools, ranging from system simulation tools through PROM monitor and debug support, applications software and utility libraries, logic analysis tools, and sub-system modules.

Figure 5 is an overview of the system development process typically used when developing R3041 applications. The RISController family is supported in all phases of project development. These tools allow timely, parallel development of hardware and software for RISController family based applications, and include tools such as:

· Optimizing compilers from MIPS Technology, the acknowl-

edged leader in optimizing compiler technology.

- Cross development tools, available in a variety of development environments.
- The high-performance IDT floating point emulation library software.
- The IDT Evaluation Board, which includes RAM, EPROM, I/O, and the IDT PROM Monitor.
- IDT Laser Printer System boards, which directly drive a lowcost print engine, and runs Adobe PostScript[™] Page Description Language
- Adobe PostScript Page Description Language running on the IDT RISController family.
- The IDT/sim[™] PROM Monitor, which implements a full PROM monitor (diagnostics, remote debug support, peek/



2905 drw 05

Figure 5. R3041 Development Environment

poke, etc.).

IDT/kit[™] (Kernel Integration Toolkit), providing library support and a frame work for the system run time environment.

PERFORMANCE OVERVIEW

The RISController family achieves a very high-level of performance. This performance is based on:

- An efficient execution engine: The CPU performs ALU operations and store operations in a single cycle, and has an effective load time of 1.3 cycles, and branch execution rate of 1.5 cycles (based on the ability of the compilers to avoid software interlocks). Thus, the R3041 achieves 20 MIPS performance at 25MHz when operating out of cache.
- Large on-chip caches: The RISController family contains caches which are substantially larger than those on the majority of embedded microprocessors. These large caches minimize the number of bus transactions required, and allow the RISController family to achieve actual sustained performance very close to its peak execution rate, even with low-cost memory systems.
- Autonomous multiply and divide operations: The RISController family features an on-chip integer multiplier/ divide unit which is separate from the other ALU. This allows the R3041 to perform multiply or divide operations in parallel with other integer operations, using a single multiply or divide instruction rather than using "step" operations.
- Integrated write buffer: The R3041 features a four deep write buffer, which captures store target addresses and data at the processor execution rate and retires it to main memory at the slower main memory access rate. Use of on-chip write buffers eliminates the need for the processor to stall when performing store operations.
- Burst read support: The R3041 enables the system designer to utilize page mode, static column, or nibble mode RAMs when performing read operations to minimize the main memory read penalty and increase the effective cache hit rates.

The performance differences among the various RISController family members depends on the application software and the design of the memory system. Different family members feature different cache sizes, and the R3081 features a hardware floating point accelerator. Since all these devices can be used in a pin and software compatible fashion, the system designer has maximum freedom in trading between performance and cost. The memory simulation tools (e.g. Cache3041) allows the system designers to analyze and understand the performance differences among these de-

vices in their application.

SELECTABLE FEATURES

The RISController family uses two methods to allow the system designer to configure bus interface operation options.

The first set of options are established via the Reset Configuration Mode inputs, sampled during the device reset. After reset, the Reset Mode inputs become regular input or output signals.

The second set of configuration options are contained in the System Control Co-Processor registers. These Co-processor registers configuration options are typically initialized with the boot PROM and can also be changed dynamically by the kernel software.

Selectable features include:

- **Big Endian vs. Little Endian operation**: The part can be configured to operate with either byte ordering convention, and in fact may also be dynamically switched between the two conventions. This facilitates the porting of applications from other processor architectures, and also permits intercommunication between various types of processors and databases.
- Data Cache Refill of one or four words: The memory system must be capable of performing 4 word transfers to satisfy instruction cache misses and 1 word transfers to satisfy uncached references. The data cache refill size option allows the system designers to choose between one and four word refill on data cache misses, depending on the performance each option brings to their application.
- **Bus Turn Around speed**: The R3041 allows the kernel to increase the amount of time between bus transactions when changes in direction of the A/D bus occur (e.g., at the end of reads followed by writes). This allows transceivers and buffers to be eliminated from the system.
- Extended Address Hold Time: The R3041 allows the system designer to increase the amount of hold time available for address latching, thus allowing slower speed (low cost) address latches, FPGAs and ASICs to be used.
- **Programmable control signals**: The R3041 allows the system designer to optimally configure various memory control signals to be active on reads only, writes only, or on both reads and writes. This allows the simplification of external logic, thus reducing system cost.

• **Programmable memory Port Widths**: The R3041 allows the kernel to partition the physical memory space into various sub-regions, and to individually indicate the port width of these sub-regions. Thus, the bus interface unit can perform data packing and unpacking when communicating with narrow memory sub-regions. For example, these features, can be used to allow the R3041 to interface with narrow 8-bit boot PROMs, or to implement 16-bit only memory systems.

THERMAL CONSIDERATIONS

The RISController family utilizes special packaging techniques to improve the thermal properties of high-speed processors. Thus, all versions of the RISController family are packaged in cavity down packaging.

The lowest cost members of the family use a standard cavity down, injection molded PLCC package (the "J" package). This package is used for all speeds of the R3041 family.

Higher speed and higher performance members of the RISController family utilize more advanced packaging techniques to dissipate power while remaining both low-cost and pin- and socket- compatible with the PLCC package. Thus, these members of the RISController family are available in the MQUAD package (the "MJ" package), which is an all aluminum package with the die attached to a normal copper leadframe mounted to the aluminum casing. The MQUAD package is pin and form compatible with the PLCC package. Thus, designers can choose to utilize this package without changing their PCB.

	Airflow (ft/min)									
ØCA	0	200	400	600	800	1000				
"J" Package	29	26	21	18	16	15				
TQFP	55	40	35	33	31	30				

2905 tbl 02

Table 2. Thermal Resistance (ØcA) at Various Airflows

The members of the RISController family are guaranteed in a case temperature range of 0°C to +85°C. The type of package, speed (power) of the device, and airflow conditions, affect the equivalent ambient conditions which meet this specification.

The equivalent allowable ambient temperature, TA, can be calculated using the thermal resistance from case to ambient (ØCA) of the given package. The following equation relates ambient and case temperature:

TA = TC - P * ØCA

where P is the maximum power consumption at hot temperature, calculated by using the maximum Icc specification for the device.

Typical values for ØCA at various airflows are shown in Table 2 for the PLCC package.

NOTES ON SYSTEM DESIGN

The R3041 has been designed to simplify the task of highspeed system design. Thus, set-up and hold-time requirements have been kept to a minimum, allowing a wide variety of system interface strategies.

To minimize these AC parameters, the R3041 employs feedback from its SysClk output to the internal bus interface unit. This allows the R3041 to reference input signals to the reference clock seen by the external system. The SysClk output is designed to provide relatively large AC drive to minimize skew due to slow rise or fall times. A typical part will have less than 2ns rise or fall (10% to 90% signal times) when driving the test load.

Therefore, the system designer should use care when designing for direct SysClk use. Total loading (due to devices connected on the signal net and the routing of the net itself) should be minimized to ensure the SysClk output has a smooth and rapid transition. Long rise and/or fall times may cause a degradation in the speed capability of an individual device.

Similarly, the R3041 employs feedback on its ALE output to ensure adequate address hold time to ALE. The system designer should be careful when designing the ALE net to minimize total loading and to minimize skew between ALE and the A/D bus, which will ensure adequate address access latch time.

IDT's field and factory applications groups can provide the system designer with assistance for these and other design issues.

PIN CONFIGURATIONS



PIN DESCRIPTION (Continued):

PIN NAME	I/O	DESCRIPTION
Burst/ WrNear	0	Burst Transfer/Write Near: On read transactions, the Burst signal indicates that the current bus read is requesting a block of four contiguous words from memory. This signal is asserted only in read cycles due to cache misses; it is asserted for all I-Cache miss read cycles, and for D-Cache miss read cycles if the 4-word data block refill option is selected in the CP0 Cache Config Register.
		On write transactions, the WrNear output tells the external memory system that the bus interface unit is performing back-to-back write transactions to an address within the same 256 byte page as the prior write transaction. This signal is useful in memory systems which employ page mode or static column DRAMs, and allows nearby writes to be retired quickly.
Rd	0	Read: An output which indicates that the current bus transaction is a read.
Wr	0	Write: An output which indicates that the current bus transaction is a write.
Ack	1	Acknowledge: An input which indicates to the device that the memory system has sufficiently processed the bus transaction. On write transactions, this signal indicates that the CPU may either progress to the next data item (for mini-burst writes of wide datums to narrow memories), or terminate the write cycle. On read transactions, this signal indicates that the memory system has sufficiently processed the read, and that the processor core may begin processing the data from this read transfer.
RdCEn	I	Read Buffer Clock Enable: An input which indicates to the device that the memory system has placed valid data on the A/D bus, and that the processor may move the data into the on-chip Read Buffer.
SysClk	0	System Reference Clock: An output from the CPU which reflects the timing of the internal processor "System" clock. This clock is used to control state transitions in the read buffer, write buffer, memory controller, and bus interface unit.
BusReq	I	DMA Arbiter Bus Request: An input to the device which requests that the CPU tri-state its bus interface signals so that they may be driven by an external master. The negation of this input relinquishes mastership back to the CPU.
BusGnt	0	DMA Arbiter Bus Grant. An output from the CPU used to acknowledge that a BusReq has been detected, and that the bus is relinquished to the external master.
		The R3041 adds an additional DMA protocol, under the control of CP0. If the DMA Protocol is enabled, the R3041 can request that the external master relinquish bus mastership back to the processor by negating the BusGnt output early, and waiting for the BusReq input to be negated.
SBrCond(3)/ IOStrobe	I/O	Branch Condition Port/IO Strobe: The use of this signal depends on the setting of various bits of the CP0 Bus Control register. If BrCond mode is selected, this input is logically connected to CpCond(3), and can be used by the branch on co-processor condition instructions as an input port. The SBrCond(3) input has special internal logic to synchronize the input, and thus may be driven by asynchronous agents.
		If this pin is selected to function as IOStrobe, it may be asserted as an output on reads, writes, or both, as programmed into CP0. This strobe asserts in the second clock cycle of a transfer, and thus can be used to strobe various control signals on the bus interface.
SBrCond(2)/ ExtDataEn	I/O	Branch Condition Port/Extended Data Enable: The use of this signal depends on the settings in the CP0 Bus Control register. If BrCond mode is selected, this input is logically connected to CpCond(2), and can be used by the branch on co-processor condition instructions as an input port. The SBrCond(2) input has special internal logic to synchronize the input, and thus may be driven by asynchronous agents.
		If this pin is selected to function as Extended Data Enable, it may be asserted as an output on reads, writes, or both, as programmed into CP0. This strobe can be used as an extended data enable strobe, in that it is held asserted for one-half clock cycle after the negation of \overline{Rd} or \overline{Wr} . This signal may typically be used as a write enable control line for transceivers, as a write line for I/O, or as an address mux select for DRAMs.
MemStrobe	0	Memory Strobe: This active low output pulses low for each data read or written, as configured in the CP0 Bus Control register. Thus, it can be used as a read strobe, write strobe, or both, for SRAM type memories or for I/O devices.
		The R3041 MemStrobe output pin is designated as the BrCond(0) input pin in the R3051 and R3081.

2905 tbl 04

ABSOLUTE MAXIMUM RATINGS^(1, 3) R3041

Symbol	Rating	Commercial	Unit
Vterm	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
Тс	Operating Case Temperature	0 to +85	°C
TBIAS	Temperature Under Bias	-55 to +125	°C
Тѕтс	Storage Temperature	-55 to +125	°C
Vin	Input Voltage	-0.5 to +7.0	V

NOTES:

2905 tbl 06 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS

may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. VIN minimum = -3.0V for pulse width less than 15ns. VIN should not exceed Vcc +0.5 Volts.

3. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

AC TEST CONDITIONS R3041

Symbol	Parameter	Min.	Max.	Unit
Vін	Input HIGH Voltage	3.0		V
VIL	Input LOW Voltage	_	0	V
Vihs	Input HIGH Voltage	3.5	—	V
VILS	Input LOW Voltage	_	0	V
				2905 tbl 08

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Commercial	0°C to +85°C	0V	5.0 ±5%
	(Case)		

2905 tbl 07

OUTPUT LOADING FOR AC TESTING



Signal	Cld
All Signals	25 pF
	2905 tbl 09

DC ELECTRICAL CHARACTERISTICS R3041 — (Tc = 0°C to +85°C, Vcc = +5.0V ±5%)

			16.67	16.67MHz		16.67MHz 20MHz		25MHz		33MHz		
Symbol	Parameter	Test Conditions	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit	
Vон	Output HIGH Voltage	Vcc = Min., Iон = -4mA	3.5	—	3.5	—	3.5	—	3.5		V	
Vol	Output LOW Voltage	VCC = Min., IOL = 4mA	_	0.4	—	0.4	-	0.4		0.4	V	
Viн	Input HIGH Voltage ⁽³⁾	—	2.0	_	2.0	_	2.0	_	2.0	Ì	V	
VIL	Input LOW Voltage ⁽¹⁾	—	—	0.8	—	0.8	—	0.8	1	0.8	V	
Vihs	Input HIGH Voltage ^(2,3)	—	3.0	_	3.0	_	3.0	_	3.0		V	
VILS	Input LOW Voltage ^(1,2)	—	—	0.4	_	0.4	—	0.4		0.4	V	
CIN	Input Capacitance ⁽⁴⁾	—	—	10	—	10	—	10	Y	10	pF	
Соит	Output Capacitance ⁽⁴⁾	—	—	10	_	10	—	10	1	10	pF	
Icc	Operating Current	Vcc = 5V, Tc = 25°C	_	225	_	250	_	300	+	370	mA	
Іін	Input HIGH Leakage	VIH = VCC	_	100	—	100	—	100	_	100	μA	
lı∟	Input LOW Leakage	VIL = GND	-100	—	-100	—	-100	—	-100		μA	
loz	Output Tri-state Leakage	VOH = 2.4V, VOL = 0.5V	-100	100	-100	100	-100	100	-100	100	μA	

NOTES:

1. VIL Min. = -3.0V for pulse width less than 15ns. VIL should not fall below -0.5 volts for larger periods.

2. VIHS and VILS apply to ClkIn and Reset.

3. VIH should not be held above Vcc + 0.5 volts.

4. Guaranteed by design.

2905 tbl 10

AC ELECTRICAL CHARACTERISTICS R3041 ^(1, 2, 3) (Tc = 0°C to +85°C, Vcc = +5.0V ±5%)

			16.67MHz		20MHz		Hz 25MHz		33MHz		
Symbol	Signals	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t1	BusReq, Ack, BusError, RdCEn	Set-up to SysClk rising	11	_	8	_	5.5	_	5.5	-	ns
t1a	A/D	Set-up to SysClk falling	12	_	9	_	7	_	7	+	ns
t2	BusReq, Ack, BusError, RdCEn	Hold from SysClk rising	4	_	3	_	2.5	_	2.5		ns
t2a	A/D	Hold from SysClk falling	2	_	2	_	1	_	1		ns
t3	A/D, Addr, Diag, ALE, Wr Burst/WrNear, Rd, DataEn	Tri-state from SysClk rising (after driven condition)	_	13	—	10	-	10	-	10	ns
t4	A/D, Addr, Diag, ALE, Wr Burst/WrNear, Rd, DataEn	Driven from SysClk falling (after tri-state condition)	_	13	_	10	—	10	+	10	ns
t5	BusGnt	Asserted from SysClk rising	_	10	_	8	_	7		7	ns
t6	BusGnt	Negated from SysClk falling	_	10	_	8	_	7	_	7	ns
t7	Wr, Rd, Burst/WrNear, TC	Valid from SysClk rising	_	8	_	6	_	5		5	ns
t7a	A/D	Valid from SysClk rising	_	12	_	9	_	8	\square	8	ns
t7b	Last	Valid from SysClk rising	_	12	_	9	_	8	-1	8	ns
t8	ALE	Asserted from SysClk rising	_	5	_	4	_	4	_	4	ns
t9	ALE	Negated from SysClk falling	_	5	_	4	_	4	+	4	ns
t10	A/D	Hold from ALE negated	2	_	2	_	2		1.5	_	ns
t11	DataEn	Asserted from SysClk	_	19	_	15	_	15		15	ns
t12	DataEn	Asserted from A/D tri-state ⁽⁴⁾	0	_	0		0	_	0	_	ns
t14	A/D	Driven from SysClk rising ⁽⁴⁾	0	_	0	_	0		0		ns
t15	Wr, Rd, DataEn, Burst/WrNear, Last, TC	Negated from SysClk falling	_	9	_	7	_	6		6	ns
t16	Addr(3:0), BE 16(1:0)	Valid from SysClk	_	11	_	8	_	7	_	7	ns
t17	Diag	Valid from SysClk	_	15	_	12	_	11	_	11	ns
t18	A/D	Tri-state from SysClk	_	13	_	10	_	10	_	10	ns
t19	A/D	SysClk to data out	_	16	_	13	_	12	+	12	ns
t20	ClkIn	Pulse Width High	12	_	10	_	8	_	6.5	_	ns
t21	ClkIn	Pulse Width Low	12	_	10	_	8	_	6.5		ns
t22	ClkIn	Clock Period	30	250	25	250	20	250	15	250	ns
t23	Reset	Pulse Width from Vcc valid	200	_	200	_	200	_	200	_	μs
t24	Reset	Minimum Pulse Width	32	_	32	_	32	_	32		sys
t25	Reset	Set-up to SysClk falling	8	_	6	—	5	_	5	-	ns
t26	Int	Mode set-up to Reset rising	8	_	6	_	5		5	-+	ns
t27	Int	Mode hold from Reset rising	2.5	_	2.5	_	2.5		2.5	-	ns
t28	SInt, SBrCond	Set-up to SysClk falling	8	_	6	_	5	_	5		ns
t29	SInt, SBrCond	Hold from SysClk falling	4	_	3	_	3		3		ns
t30	Int, BrCond	Set-up to SysClk falling	8	_	6	—	5	_	5		ns
t31	Int, BrCond	Hold from SysClk falling	4	_	3	_	3	_	3	4	ns
tsys	SysClk	Pulse Width	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	ns
t32	SysClk	Clock High Time	t22 - 2	t22 + 2	t22 - 2	t22 + 2	t22 - 2	t22 + 2	t22 - 2	t22 + 2	ns
t33	SysClk	Clock Low Time	t22 - 2	t22 + 2	t22 - 2	t22 + 2	t22 - 2	t22 + 2	t22 - 2	t22 + 2	ns

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			16.67 MHz 20 MHz		MHz	25MHz		33MHz			
Symbol	Signals	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t18	A/D	Tri-state from SysClk		13		10	_	10	—	10	ns
t19	A/D	SysClk to data out	—	16		13	_	12		12	ns
t20	ClkIn	Pulse Width High	12	_	10		8		6.5		ns
t21	ClkIn	Pulse Width Low	12	_	10	—	8	_	6.5	_	ns
t22	ClkIn	Clock Period	30	250	25	250	20	250	15	250	ns
t23	Reset	Pulse Width from Vcc valid	200	_	200	_	200	_	200	<u>r - </u>	μs
t24	Reset	Minimum Pulse Width	32	_	32	_	32	_	32		sys
t25	Reset	Set-up to SysClk falling	8	_	6	_	5	_	5		ns
t26	Int	Mode set-up to Reset rising	8	—	6	—	5	—	5	\rightarrow	ns
t27	Int	Mode hold from Reset rising	2.5	_	2.5	_	2.5	_	2.5		ns
t28	SInt, SBrCond	Set-up to SysClk falling	8		6	—	5	—	5		ns
t29	SInt, SBrCond	Hold from SysClk falling	4		3	—	3	_	3		ns
t30	Int, BrCond	Set-up to SysClk falling	8	—	6	—	5	—	5		ns
t31	Int, BrCond	Hold from SysClk falling	4	_	3	_	3		3	_	ns
tsys	SysClk	Pulse Width	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	2*t22	ns
t32	SysClk	Clock High Time	t22 - 2	t22 + 2	t22 - 2	t22 + 2	t22 - 2	t22 + 2	t22 - 2	t22 + 2	ns
t33	SysClk	Clock Low Time	t22 - 2	t22 + 2	t22 - 2	t22 + 2	t22 - 2	t22 + 2	t22 - 2	t22 + 2	ns
t45	ExtDataEn	Tri-state from SysClk rising (after driven condition)	—	13	—	10	—	10		10	ns
t46	ExtDataEn	Driven from SysClk falling (after driven condition)	-	13	—	10	_	10		10	ns
t47	IOStrobe	Valid from SysClk falling	—	10	—	8	_	7		7	ns
t48	ExtDataEn,	Asserted from SysClk rising	—	15		12	—	9	_	9	ns
t49	ExtDataEn DataEn	Negated from SysClk rising	_	9	_	7	_	6	_	6	ns
t50	MemStrobe	Asserted from SysClk rising	_	19	—	15	_	15	<u> </u>	15	ns
t51	MemStrobe	Negated from SysClk falling	_	19	_	15	_	15	-	15	ns
t52	MemStrobe	Asserted from Addr(3:0) valid ⁽⁴⁾	0		0	_	0		0	_	ns
tderate	All outputs	Timing deration for loading over 25pF ^(4, 5)	_	0.5	_	0.5	_	0.5	—	0.5	ns/ 25pF
NOTES:	•									;	2905 tbl 12

AC ELECTRICAL CHARACTERISTICS RV3041 (CONT.)

1. All timings referenced to 1.5 Volts, with a rise and fall time of less than 2.5ns.

2. All outputs tested with 25pF loading.

3. The AC values listed here reference timing diagrams contained in the R3041 Hardware User's Manual.

4. Guaranteed by design.

5. This parameter is used to derate the AC timings according to the loading of the system. This parameter provides a deration for loads over the specified test condition; that is, the deration factor is applied for each 25pF over the specified test load condition.

6. Timings t34 - t44 are reserved for other RISController family members.





Figure 12(c). Start of Write Timing with Non-Extended Address Hold Option



Figure 12(d). Start of Write Timing with Extended Address Hold Option



Figure 15. R3041 Quad Word Read







Figure 17. Basic Write to 32-bit Memory Port



Figure 18. Tri-Byte Mini-burst Write to 8-bit Port







Figure 20. R3041 Regaining Bus Mastership



