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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C500
Core Size	8-Bit
Speed	10MHz
Connectivity	CANbus, EBI/EMI, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	49
Program Memory Size	64KB (64K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	2.5K x 8
Voltage - Supply (Vcc/Vdd)	4.25V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	P-MQFP-80-1
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/c515c8emcafxqma1

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Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number P-MQFP-80-1	I/O[1)]	Function
$\overline{PE}$/SWD	75	I	**$\overline{Power\ saving\ mode\ enable}$ / Start watchdog timer** A low level on this pin allows the software to enter the power down, idle and slow down mode. In case the low level is also seen during reset, the watchdog timer function is off on default. Use of the software controlled power saving modes is blocked, when this pin is held on high level. A high level during reset performs an automatic start of the watchdog timer immediately after reset. When left unconnected this pin is pulled high by a weak internal pull-up resistor.
V_{SSCLK}	13	–	**Ground (0 V) for on-chip oscillator** This pin is used for ground connection of the on-chip oscillator circuit.
V_{DDCLK}	14	–	**Supply voltage for on-chip oscillator** This pin is used for power supply of the on-chip oscillator circuit.
V_{DDE1} V_{DDE2}	32 68	–	**Supply voltage for I/O ports** These pins are used for power supply of the I/O ports during normal, idle, and power down mode.
V_{SSE1} V_{SSE2}	35 70	–	**Ground (0 V) for I/O ports** These pins are used for ground connections of the I/O ports during normal, idle, and power down mode.
V_{DD1}	33	–	**Supply voltage for internal logic** This pins is used for the power supply of the internal logic circuits during normal, idle, and power down mode.
V_{SS1}	34	–	**Ground (0 V) for internal logic** This pin is used for the ground connection of the internal logic circuits during normal, idle, and power down mode.

The XRAM/CAN controller can be accessed by read/write instructions (MOVX A,DPTR, MOVX @DPTR,A), which use the 16-bit DPTR for indirect addressing. For accessing the XRAM or CAN controller, the effective address stored in DPTR must be in the range of $F700_H$ to $FFFF_H$.

The XRAM can be also accessed by read/write instructions (MOVX A,@Ri, MOVX @Ri,A), which use only an 8-bit address (indirect addressing with registers R0 or R1). Therefore, a special page register XPAGE which provides the upper address information (A8-A15) during 8-bit XRAM accesses. The behaviour of Port 0 and P2 during a MOVX access depends on the control bits XMAP0 and XMAP1 in register SYSCON and on the state of pin $\overline{EA}$. **Table 3** lists the various operating conditions.

Table 3 Behaviour of P0/P2 and $\overline{RD}/\overline{WR}$ During MOVX Accesses

			XMAP1, XMAP0		
			00	**10**	**X1**
$\overline{EA}$ = 0	MOVX @DPTR	DPTR < XRAM/CAN address range	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used
		DPTR ≥ XRAMCAN address range	a) P0/P2→Bus ($\overline{RD}/\overline{WR}$-Data) b) $\overline{RD}/\overline{WR}$ inactive c) XRAM is used	a) P0/P2→Bus ($\overline{RD}/\overline{WR}$-Data) b) $\overline{RD}/\overline{WR}$ active c) XRAM is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used
	MOVX @ Ri	XPAGE < XRAMCAN addr. page range	a) P0→Bus P2→I/O b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used	a) P0→Bus P2→I/O b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used	a) P0→Bus P2→I/O b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used
		XPAGE ≥ XRAMCAN addr. page range	a) P0→Bus ($\overline{RD}/\overline{WR}$-Data) P2→I/O b) $\overline{RD}/\overline{WR}$ inactive c) XRAM is used	a) P0→Bus ($\overline{RD}/\overline{WR}$-Data only) P2→I/O b) $\overline{RD}/\overline{WR}$ active c) XRAM is used	a) P0→Bus P2→I/O b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used
$\overline{EA}$ = 1	MOVX @DPTR	DPTR < XRAM/CAN address range	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used
		DPTR ≥ XRAMCAN address range	a) P0/P2→I/0 b) $\overline{RD}/\overline{WR}$ inactive c) XRAM is used	a) P0/P2→Bus ($\overline{RD}/\overline{WR}$-Data) b) $\overline{RD}/\overline{WR}$ active c) XRAM is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used
	MOVX @ Ri	XPAGE < XRAMCAN addr. page range	a) P0→Bus P2→I/O b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used	a) P0→Bus P2→I/O b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used	a) P0→Bus P2→I/O b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used
		XPAGE ≥ XRAMCAN addr. page range	a) P2→I/O P0/P2→I/O b) $\overline{RD}/\overline{WR}$ inactive c) XRAM is used	a) P0→Bus ($\overline{RD}/\overline{WR}$-Data) P2→I/O b) $\overline{RD}/\overline{WR}$ active c) XRAM is used	a) P0→Bus P2→I/O b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used

modes compatible to 8051/C501 family

Enhanced Hooks Emulation Concept

The Enhanced Hooks Emulation Concept of the C500 microcontroller family is a new, innovative way to control the execution of C500 MCUs and to gain extensive information on the internal operation of the controllers. Emulation of on-chip ROM based programs is possible, too.

Each production chip has built-in logic for the support of the Enhanced Hooks Emulation Concept. Therefore, no costly bond-out chips are necessary for emulation. This also ensure that emulation and production chips are identical.

The Enhanced Hooks Technology, which requires embedded logic in the C500 allows the C500 together with an EH-IC to function similar to a bond-out chip. This simplifies the design and reduces costs of an ICE-system. ICE-systems using an EH-IC and a compatible C500 are able to emulate all operating modes of the different versions of the C500 microcontrollers. This includes emulation of ROM, ROM with code rollover and ROMless modes of operation. It is also able to operate in single step mode and to read the SFRs after a break.

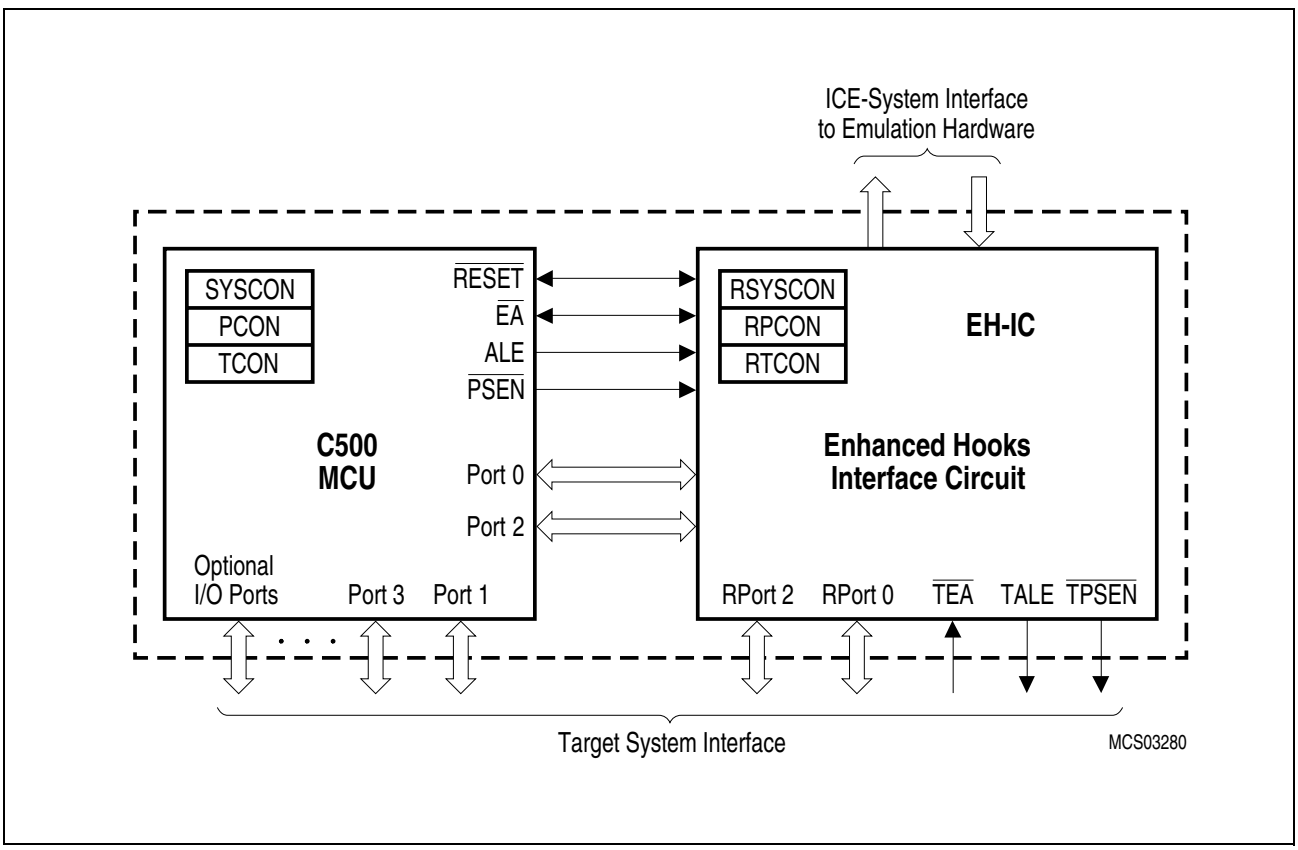


Figure 9 Basic C500 MCU Enhanced Hooks Concept Configuration

Port 0, port 2 and some of the control lines of the C500 based MCU are used by Enhanced Hooks Emulation Concept to control the operation of the device during emulation and to transfer informations about the program execution and data transfer between the external emulation hardware (ICE-system) and the C500 MCU.

Table 4 Special Function Registers - Functional Block

Block	Symbol	Name	Addr	Contents after Reset
CPU	ACC	Accumulator	**$E0_H$**[2]	00_H
	B	B-Register	**$F0_H$**[2]	00_H
	DPH	Data Pointer, High Byte	83_H	00_H
	DPL	Data Pointer, Low Byte	82_H	00_H
	DPSEL	Data Pointer Select Register	92_H	$XXXXX000_B$[3]
	PSW	Program Status Word Register	**$D0_H$**[2]	00_H
	SP	Stack Pointer	81_H	07_H
	SYSCON[1]	System Control Register C515C-8R	$B1_H$	$X010XX01_B$[3]
		C515C-8E	$B1_H$	$X010X001_B$[3]
A/D-Converter	ADCON0[1]	A/D Converter Control Register 0	**$D8_H$**[2]	00_H
	ADCON1	A/D Converter Control Register 1	DC_H	$0XXXX000_B$[3]
	ADDATH	A/D Converter Data Register High Byte	$D9_H$	00_H
	ADDATL	A/D Converter Data Register Low Byte	DA_H	$00XXXXXX_B$[3]
Interrupt System	IEN0[1]	Interrupt Enable Register 0	**$A8_H$**[2]	00_H
	IEN1[1]	Interrupt Enable Register 1	**$B8_H$**[2]	00_H
	IEN2	Interrupt Enable Register 2	$9A_H$	$XX00X00X_B$[3]
	IP0[1]	Interrupt Priority Register 0	$A9_H$	00_H
	IP1	Interrupt Priority Register 1	$B9_H$	$0X000000_B$[3]
	TCON[1]	Timer Control Register	**88_H**[2]	00_H
	T2CON[1]	Timer 2 Control Register	**$C8_H$**[2]	00_H
	SCON[1]	Serial Channel Control Register	**98_H**[2]	00_H
	IRCON	Interrupt Request Control Register	**$C0_H$**[2]	00_H
XRAM	XPAGE	Page Address Register for Extended on-chip XRAM and CAN Controller	91_H	00_H
	SYSCON[1]	System Control Register C515C-8R	$B1_H$	$X010XX01_B$[3]
		C515C-8E	$B1_H$	$X010X001_B$[3]
Ports	P0	Port 0	**80_H**[2]	FF_H
	P1	Port 1	**90_H**[2]	FF_H
	P2	Port 2	**$A0_H$**[2]	FF_H
	P3	Port 3	**$B0_H$**[2]	FF_H
	P4	Port 4	**$E8_H$**[2]	FF_H
	P5	Port 5	**$F8_H$**[2]	FF_H
	DIR5	Port 5 Direction Register	**$F8_H$**[2][4]	FF_H
	P6	Port 6, Analog/Digital Input	DB_H	–
	P7	Port 7	FA_H	$XXXXXXX1_B$[3]
	SYSCON[1]	System Control Register C515C-8R	$B1_H$	$X010XX01_B$[3]
		C515C-8E		$X010X001_B$[3]
Watchdog	WDTREL	Watchdog Timer Reload Register	86_H	00_H
	IEN0[1]	Interrupt Enable Register 0	**$A8_H$**[2]	00_H
	IEN1[1]	Interrupt Enable Register 1	**$B8_H$**[2]	00_H
	IP0[1]	Interrupt Priority Register 0	$A9_H$	00_H

Table 5 Contents of the SFRs, SFRs in Numeric Order of their Addresses

Addr.	Register	Content after Reset[1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
80_H[2]	P0	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
81_H	SP	07_H	.7	.6	.5	.4	.3	.2	.1	.0
82_H	DPL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
83_H	DPH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
86_H	WDTREL	00_H	WDT PSEL	.6	.5	.4	.3	.2	.1	.0
87_H	PCON	00_H	SMOD	PDS	IDLS	SD	GF1	GF0	PDE	IDLE
88_H[2]	TCON	00_H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
88_H[3]	PCON1[4]	$0XXX\text{-}XXXX_B$	EWPD	–	–	–	–	–	–	–
88_H[3]	PCON1[5]	$0XX0\text{-}XXXX_B$	EWPD	–	–	WS	–	–	–	–
89_H	TMOD	00_H	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
$8A_H$	TL0	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8B_H$	TL1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8C_H$	TH0	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8D_H$	TH1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
90_H[2]	P1	FF_H	T2	CLK-OUT	T2EX	$\overline{INT2}$	INT6	INT5	INT4	$\overline{INT3}$
91_H	XPAGE	00_H	.7	.6	.5	.4	.3	.2	.1	.0
92_H	DPSEL	$XXXX\text{-}X000_B$	–	–	–	–	–	.2	.1	.0
93_H	SSCCON	07_H	SCEN	TEN	MSTR	CPOL	CPHA	BRS2	BRS1	BRS0
94_H	STB	XX_H	.7	.6	.5	.4	.3	.2	.1	.0
95_H	SRB	XX_H	.7	.6	.5	.4	.3	.2	.1	.0
96_H	SSCMOD	00_H	LOOPB	TRIO	0	0	0	0	0	LSBSM
98_H[2]	SCON	00_H	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
99_H	SBUF	XX_H	.7	.6	.5	.4	.3	.2	.1	.0
$9A_H$	IEN2	$X00X\text{-}X00X_B$	–	–	EX8	EX7	–	ESSC	ECAN	–
$A0_H$[2]	P2	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
$A8_H$[2]	IEN0	00_H	EAL	WDT	ET2	ES	ET1	EX1	ET0	EX0
$A9_H$	IP0	00_H	OWDS	WDTS	.5	.4	.3	.2	.1	.0

Table 5 Contents of the SFRs, SFRs in Numeric Order of their Addresses (cont'd)

Addr.	Register	Content after Reset[1)]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AA_H	SRELL	$D9_H$	.7	.6	.5	.4	.3	.2	.1	.0
AB_H	SCF	XXXX-XX00$_B$	–	–	–	–	–	–	WCOL	TC
AC_H	SCIEN	XXXX-XX00$_B$	–	–	–	–	–	–	WCEN	TCEN
$B0_H$[2)]	P3	FF_H	RD	WR	T1	T0	INT1	INT0	TxD	RxD
$B1_H$	SYSCON[4)]	X010-XX01$_B$	–	PMOD	EALE	RMAP	–	–	XMAP1	XMAP0
$B1_H$	SYSCON[5)]	X010-X001$_B$	–	PMOD	EALE	RMAP	–	CSWO	XMAP1	XMAP0
$B8_H$[2)]	IEN1	00_H	EXEN2	SWDT	EX6	EX5	EX4	EX3	EX2	EADC
$B9_H$	IP1	0X00-0000$_B$	PDIR	–	.5	.4	.3	.2	.1	.0
BA_H	SRELH	XXXX-XX11$_B$	–	–	–	–	–	–	.1	.0
$C0_H$[2)]	IRCON	00_H	EXF2	TF2	IEX6	IEX5	IEX4	IEX3	IEX2	IADC
$C1_H$	CCEN	00_H	COCAH3	COCAL3	COCAH2	COCAL2	COCAH1	COCAL1	COCAH0	COCAL0
$C2_H$	CCL1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C3_H$	CCH1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C4_H$	CCL2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C5_H$	CCH2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C6_H$	CCL3	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C7_H$	CCH3	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C8_H$[2)]	T2CON	00_H	T2PS	I3FR	I2FR	T2R1	T2R0	T2CM	T2I1	T2I0
CA_H	CRCL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CB_H	CRCH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CC_H	TL2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CD_H	TH2	00_H	.7	.6	.5	.4	.3	.2	.1	.0

Table 5 Contents of the SFRs, SFRs in Numeric Order of their Addresses (cont'd)

Addr.	Register	Content after Reset[1)]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$D0_H$[2)]	PSW	00_H	CY	AC	F0	RS1	RS0	OV	F1	P
$D8_H$[2)]	ADCON0	00_H	BD	CLK	ADEX	BSY	ADM	MX2	MX1	MX0
$D9_H$	ADDATH	00_H	.9	.8	.7	.6	.5	.4	.3	.2
DA_H	ADDATL	$00XX\text{-}XXXX_B$	.1	.0	–	–	–	–	–	–
DB_H	P6	–	.7	.6	.5	.4	.3	.2	.1	.0
DC_H	ADCON1	$0XXX\text{-}X000_B$	ADCL	–	–	–	0	MX2	MX1	MX0
$E0_H$[2)]	ACC	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$E8_H$[2)]	P4	FF_H	RXDC	TXDC	$\overline{INT8}$	$\overline{SLS}$	STO	SRI	SCLK	$\overline{ADST}$
$F0_H$[2)]	B	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F8_H$[2)]	P5	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
$F8_H$[2)]	DIR5[6)]	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
FA_H	P7	$XXXX\text{-}XXX1_B$	–	–	–	–	–	–	–	$\overline{INT7}$
FC_H	VR0[7)8)]	$C5_H$	1	1	0	0	0	1	0	1
FD_H	VR1[7)8)]	95_H	1	0	0	1	0	1	0	1
FE_H	VR2[7)8)]	02_H[9)]	0	0	0	0	0	0	1	0

1) "X" means that the value is undefined and the location is reserved.

2) Bit-addressable special function registers

3) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.

4) This SFR is available in the C515C-8R and C515C-L.

5) This SFR is available in the C515C-8E.

6) This SFR is a mapped SFR. For accessing this SFR, bit PDIR in SFR IP1 must be set.

7) This SFR is a mapped SFR. For accessing this SFR, bit RMAP in SFR SYSCON must be set.

8) These SFRs are read-only registers (C515C-8E only).

9) The content of this SFR varies with the actual step of the C515C-8E (e.g. 01_H for the first step).

Port Structure Selection of Port 5

After a reset operation of the C515C, the quasi-bidirectional 8051-compatible port structure is selected. For selection of the bidirectional (CMOS) port 5 structure the bit PMOD of SFR SYSCON must be set. Because each port 5 pin can be programmed as an input or an output, additionally, after the selection of the bidirectional mode the direction register DIR5 of port 5 must be written. This direction register is mapped to the port 5 register. This means, the port register address is equal to its direction register address. **Figure 10** illustrates the port and direction register configuration.

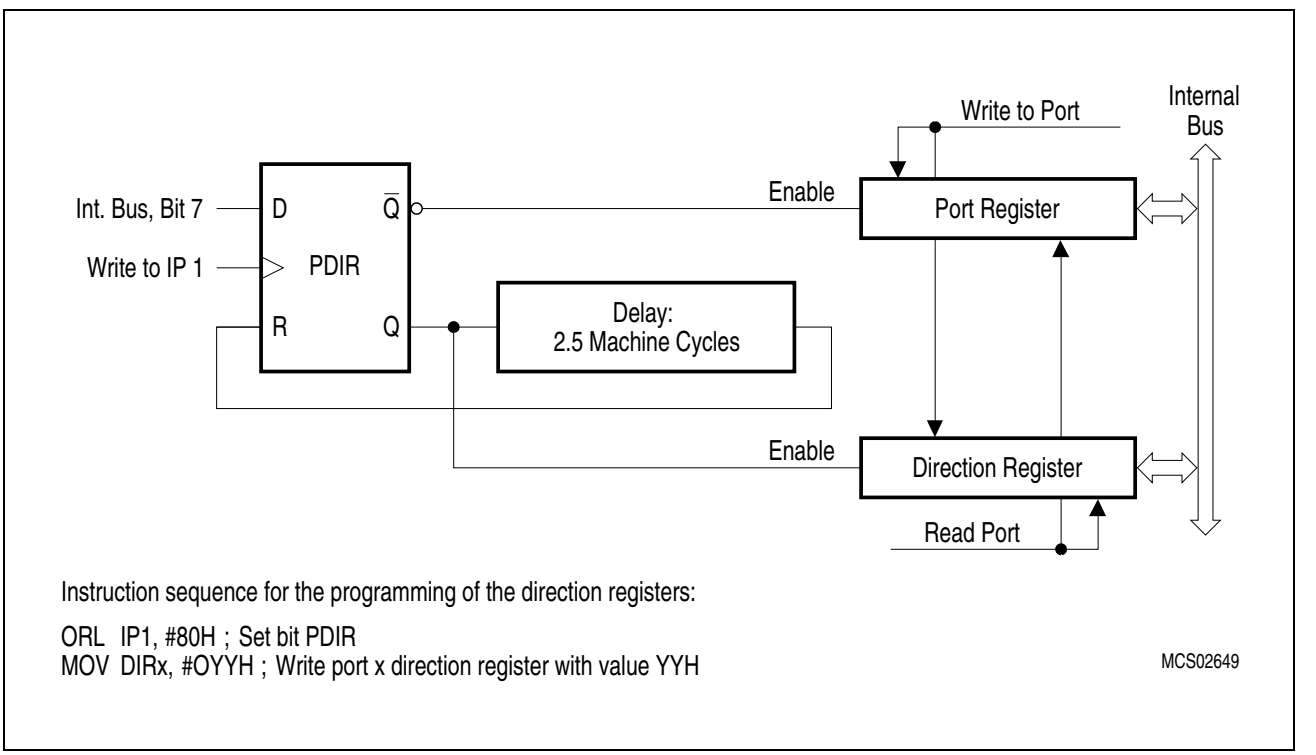
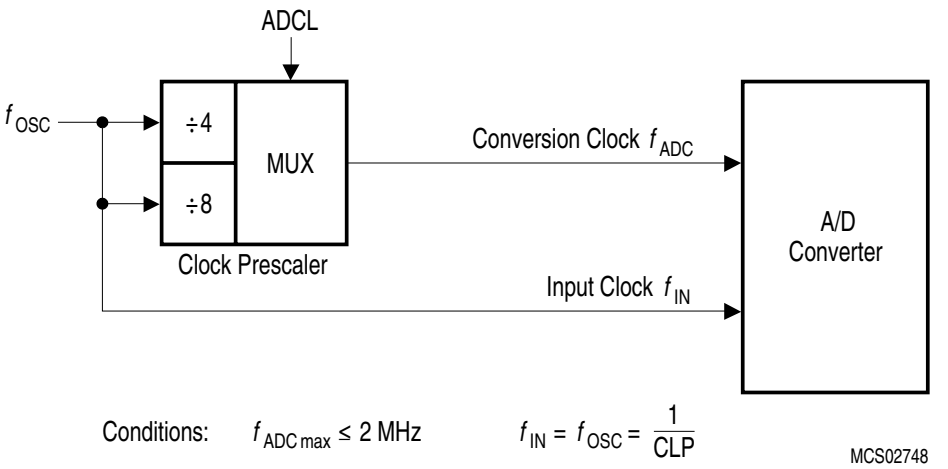


Figure 10 Port Register, Direction Register



MCU System Clock Rate (f_{OSC})	ADCL	Conversion Clock f_{ADC} [MHz]
2 MHz	0	.5
4 MHz	0	1
6 MHz	0	1.5
8 MHz	0	2
10 MHz	1	1.25

Figure 18 A/D Converter Clock Selection

Interrupt System

The C515C provides 17 interrupt sources with four priority levels. Seven interrupts can be generated by the on-chip peripherals (timer 0, timer 1, timer 2, serial interface, A/D converter, SSC interface, CAN controller), and ten interrupts may be triggered externally (P1.5/T2EX, P3.2/INT0, P3.3/INT1, P1.4/INT2, P1.0/$\overline{\text{INT3}}$, P1.1/INT4, P1.2/INT5, P1.3/INT6, P7.0/$\overline{\text{INT7}}$, P4.5/$\overline{\text{INT8}}$). The wake-up from power-down mode interrupt has a special functionality which allows to exit from the software power-down mode by a short low pulse at pin P3.2/$\overline{\text{INT0}}$.

In the C515C the 17 interrupt sources are combined to six groups of two or three interrupt sources. Each interrupt group can be programmed to one of the four interrupt priority levels. **Figure 20** to **Figure 22** give a general overview of the interrupt sources and illustrate the interrupt request and control flags.

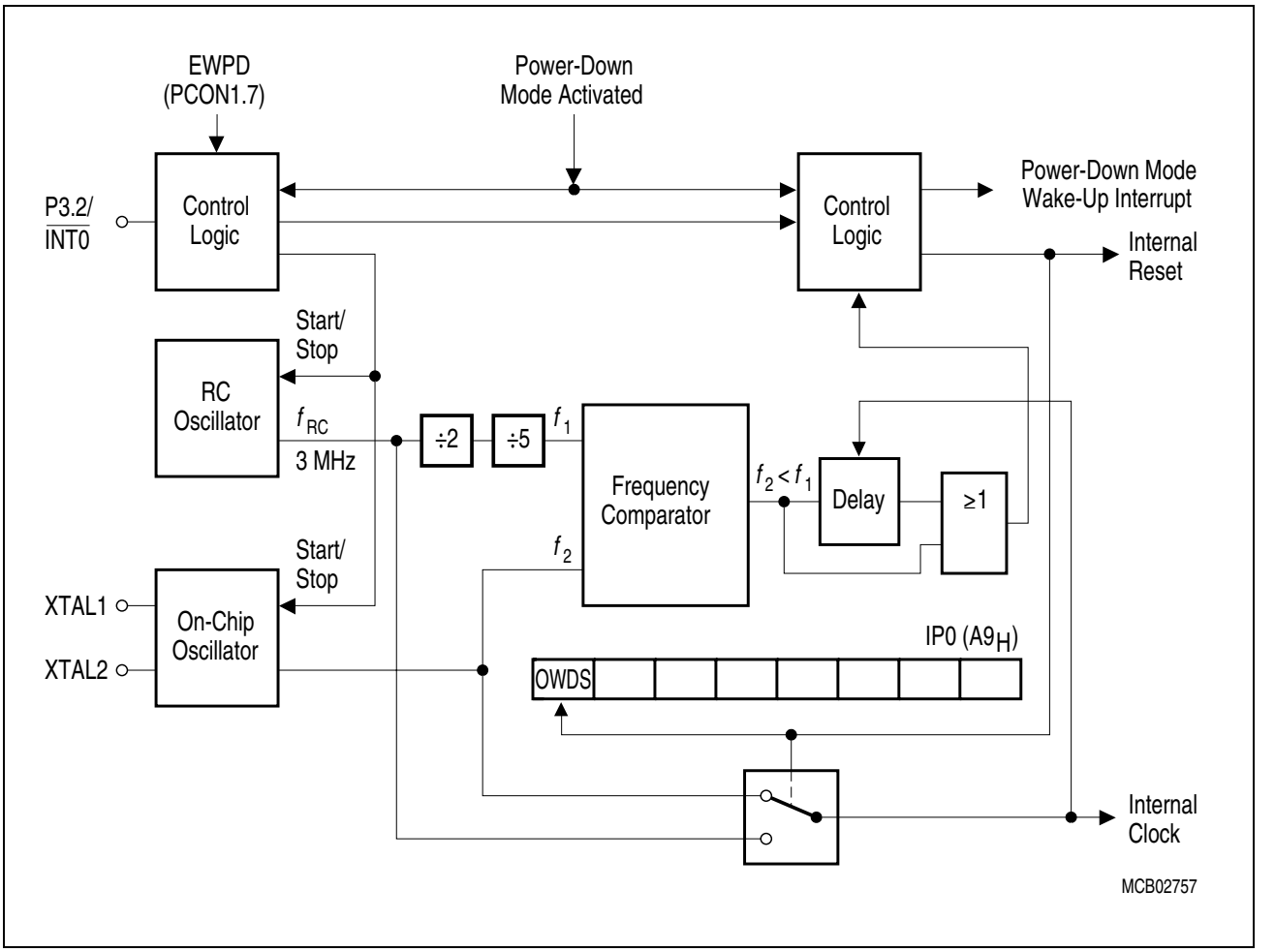


Figure 24 Block Diagram of the Oscillator Watchdog

Power Saving Modes

The C515C provides two basic power saving modes, the idle mode and the power down mode. Additionally, a slow down mode is available. This power saving mode reduces the internal clock rate in normal operating mode and it can be also used for further power reduction in idle mode.

- **Idle mode**
  The CPU is gated off from the oscillator. All peripherals are still provided with the clock and are able to work. Idle mode is entered by software and can be left by an interrupt or reset.
- **Power down mode**
  The operation of the C515C is completely stopped and the oscillator is turned off. This mode is used to save the contents of the internal RAM with a very low standby current.
  Software power down mode: Software power down mode is entered by software and can be left by reset or by a short low pulse at pin P3.2/$\overline{\text{INT0}}$ (or P4.7/$\overline{\text{RXDC}}$, C515C-8E only).
  Hardware power down mode: Hardware power down mode is entered when the pin $\overline{\text{HWPD}}$ is put to low level.
- **Slow-down mode**
  The controller keeps up the full operating functionality, but its normal clock frequency is internally divided by 32. This slows down all parts of the controller, the CPU and all peripherals, to 1/32th of their normal operating frequency. Slowing down the frequency significantly reduces power consumption. The slow down mode can be combined with the idle mode.

Table 11 gives a general overview of the entry and exit conditions of the power saving modes.

In the power down mode of operation, V_{DD} can be reduced to minimize power consumption. It must be ensured, however, that V_{DD} is not reduced before the power down mode is invoked, and that V_{DD} is restored to its normal operating level, before the power down mode is terminated.

If e.g. the idle mode is left through an interrupt, the microcontroller state (CPU, ports, peripherals) remains preserved. If a power saving mode is left by a hardware reset, the microcontroller state is disturbed and replaced by the reset state of the C515C.

If WS (bit 4) is SFR PCON1 is set (C515C-8E only), pin P4.7/$\overline{\text{RXDC}}$ is alternatively selected as wake-up pin for the software power down mode. If WS (bit 4) is SFR PCON1 is cleared (C515C-8E only), pin P3.2/$\overline{\text{INT0}}$ is selected as wake-up pin for the software power down mode.

For the C515C-8R, P3.2/$\overline{\text{INT0}}$ is always selected as wake-up pin.

C515C-8E Pin Configuration in Programming Mode

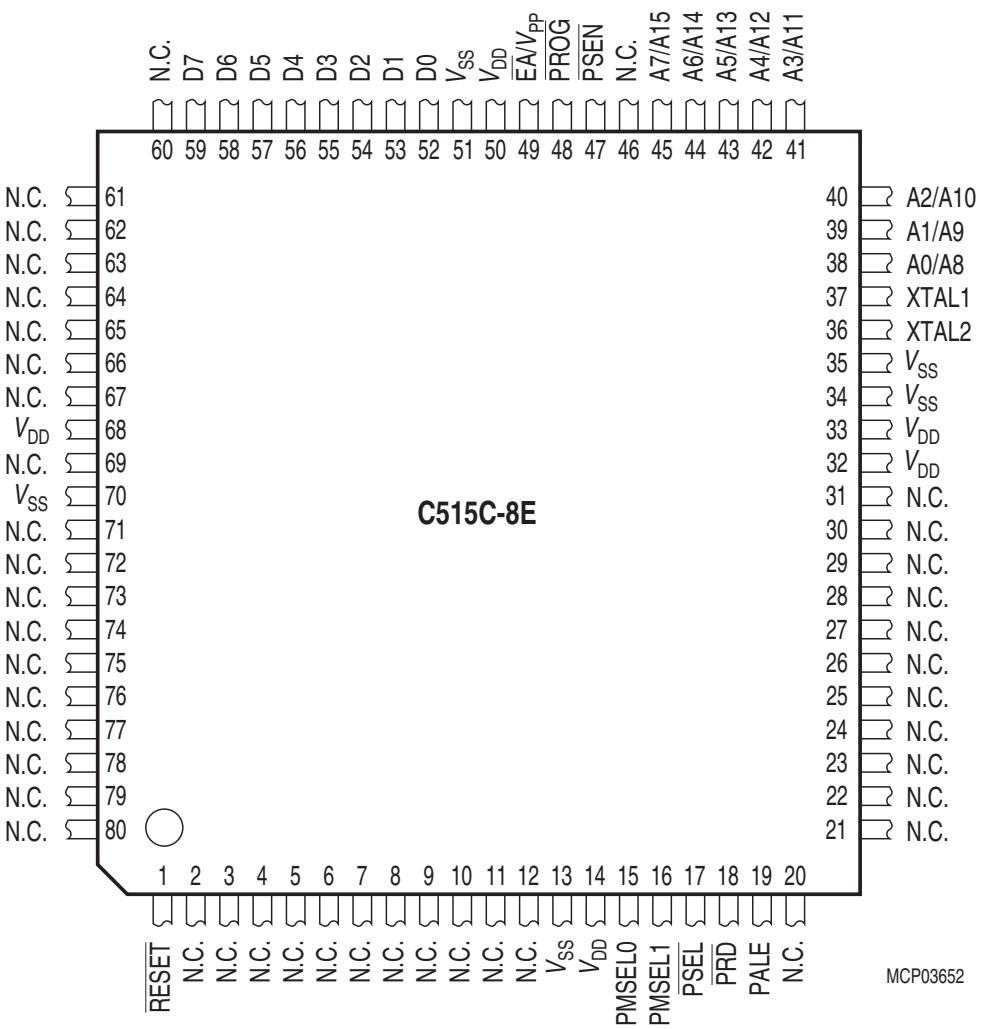


Figure 26 **P-MQFP-80-1 Pin Configuration of the C515C-8E in Programming Mode** (top view)

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Storage temperature	T_{ST}	-65	150	°C	–
Voltage on V_{DD} pins with respect to ground (V_{SS})	V_{DD}	-0.5	6.5	V	–
Voltage on any pin with respect to ground (V_{SS})	V_{IN}	-0.5	V_{DD} + 0.5	V	–
Input current on any pin during overload condition	–	-10	10	mA	–
Absolute sum of all input currents during overload condition	–	–	|100 mA|	mA	–
Power dissipation	P_{DISS}	–	1	W	–

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During absolute maximum rating overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$) the voltage on V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Power Supply Current Calculation Formulas

Parameter		Symbol	Formula
Active mode	C515C-8R/ C515C-LM	$I_{DD\ typ}$ $I_{DD\ max}$	$1.71 \times f_{OSC} + 1.71$ $1.84 \times f_{OSC} + 2.7$
	C515C-8E	$I_{DD\ typ}$ $I_{DD\ max}$	$1.59 \times f_{OSC} + 1.76$ $1.79 \times f_{OSC} + 2.2$
Idle mode	C515C-8R/ C515C-LM	$I_{DD\ typ}$ $I_{DD\ max}$	$0.89 \times f_{OSC} + 1.56$ $1.00 \times f_{OSC} + 1.87$
	C515C-8E	$I_{DD\ typ}$ $I_{DD\ max}$	$0.19 \times f_{OSC} + 2.81$ $0.20 \times f_{OSC} + 3.5$
Active mode with slow-down enabled	C515C-8R/ C515C-LM	$I_{DD\ typ}$ $I_{DD\ max}$	$0.14 \times f_{OSC} + 3.22$ $0.18 \times f_{OSC} + 3.95$
	C515C-8E	$I_{DD\ typ}$ $I_{DD\ max}$	$0.16 \times f_{OSC} + 3.05$ $0.19 \times f_{OSC} + 3.63$
Idle mode with slow-down enabled	C515C-8R/ C515C-LM	$I_{DD\ typ}$ $I_{DD\ max}$	$0.08 \times f_{OSC} + 3.06$ $0.11 \times f_{OSC} + 3.8$
	C515C-8E	$I_{DD\ typ}$ $I_{DD\ max}$	$0.13 \times f_{OSC} + 2.84$ $0.14 \times f_{OSC} + 3.37$

Note: f_{OSC} is the oscillator frequency in MHz. I_{DD} values are given in mA.

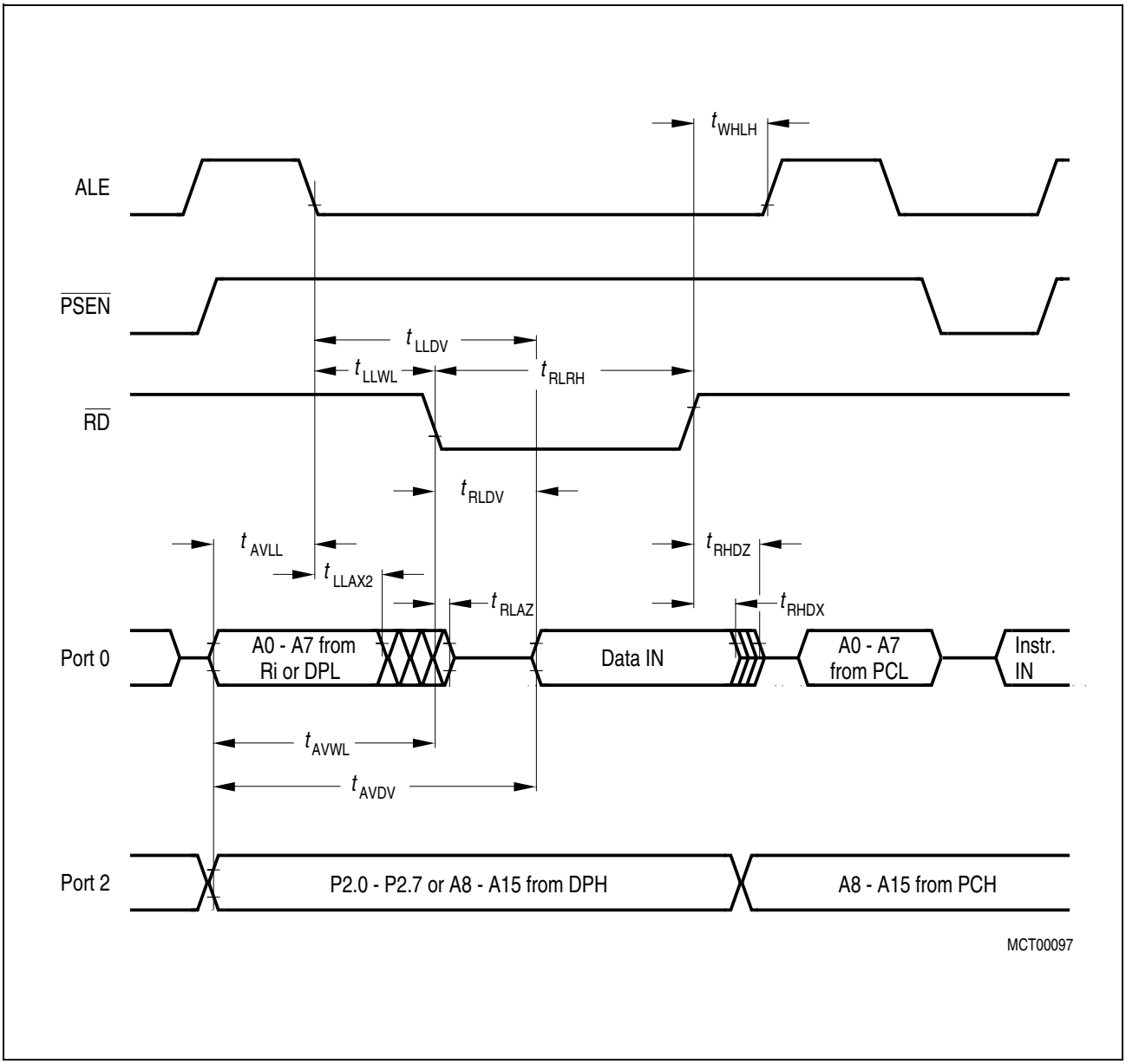


Figure 31 Data Memory Read Cycle

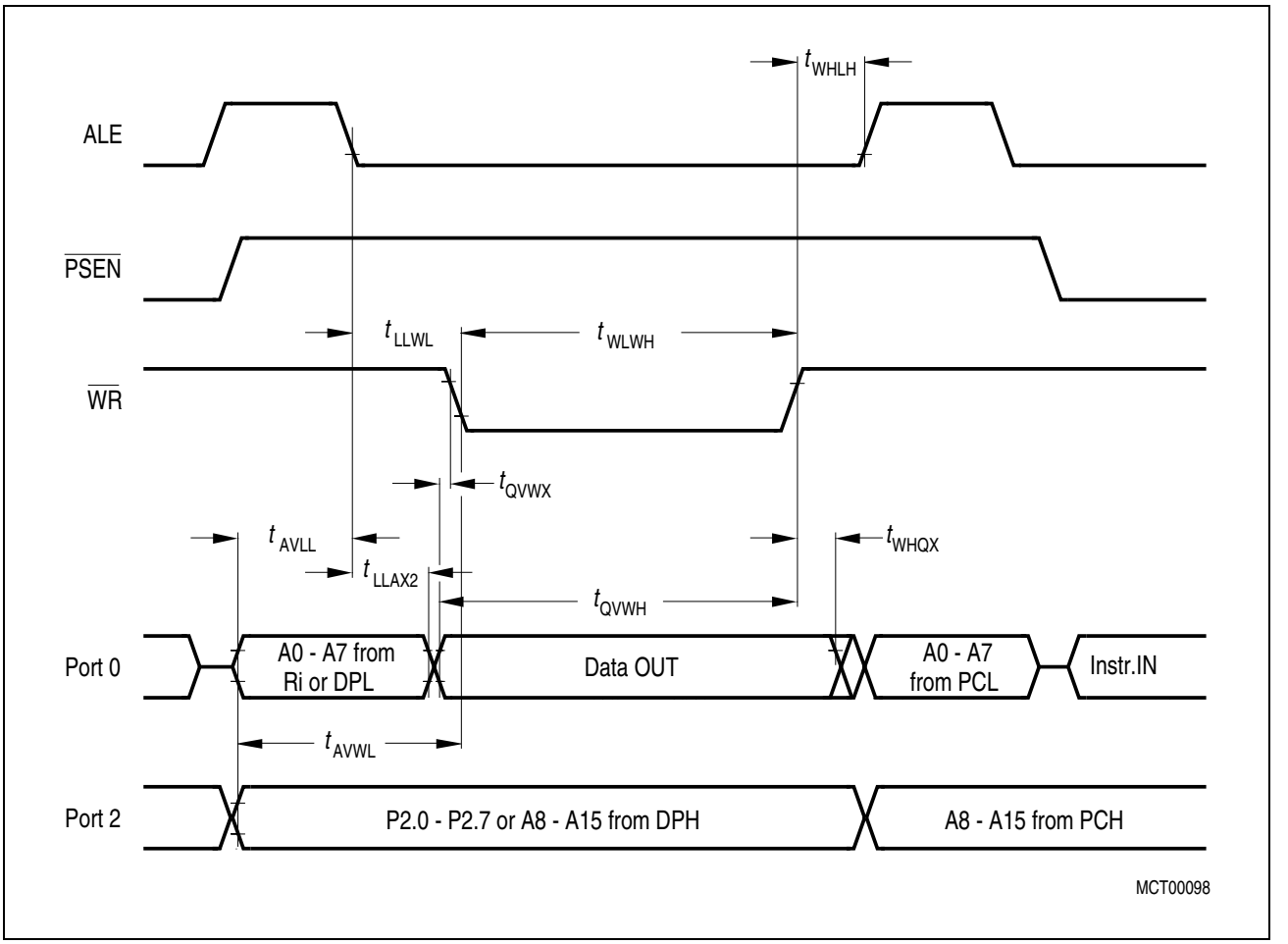


Figure 32 Data Memory Write Cycle

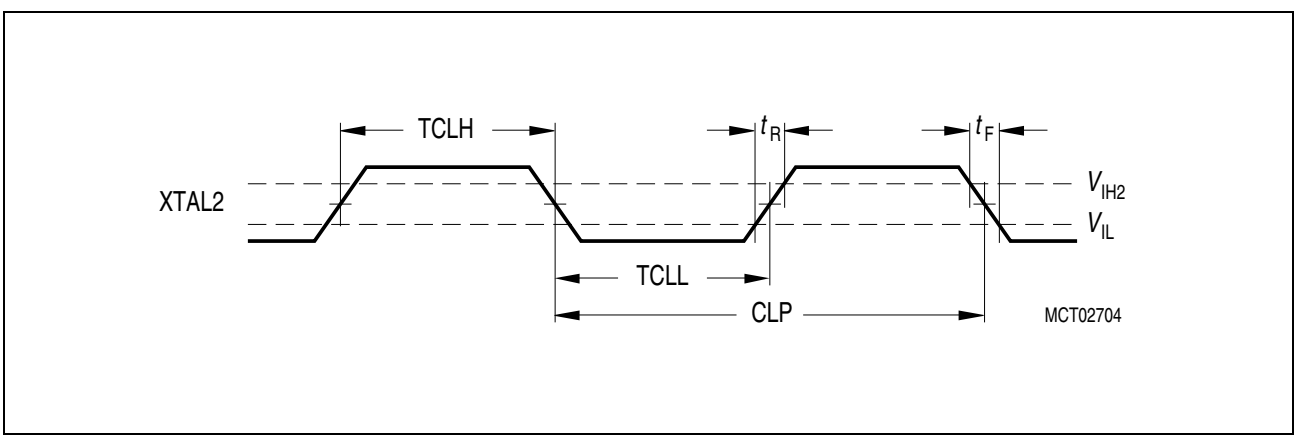
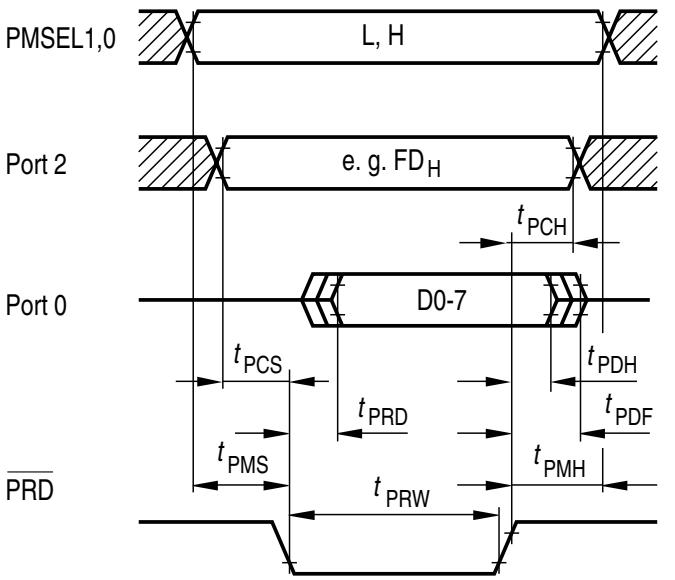


Figure 33 External Clock Drive at XTAL2



Note: $\overline{\text{PROG}}$ must be high during a programming read cycle.

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Figure 38 Version Byte - Read Timing