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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C500
Core Size	8-Bit
Speed	10MHz
Connectivity	CANbus, EBI/EMI, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	49
Program Memory Size	64KB (64K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	2.5K x 8
Voltage - Supply (Vcc/Vdd)	4.25V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	PG-MQFP-80-7
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/c515c8emcafxuma1

The C515C-8R contains a non-volatile 64 Kbytes read-only program memory. The C515C-L is identical to the C515C-8R, except that it lacks the on-chip program memory. The C515C-8E is the OTP version in the C515C microcontroller with an on-chip 64 Kbytes one-time programmable (OTP) program memory. The C515C is mounted in a P-MQFP-80-1 package.

If compared to the C515C-8R and C515C-L, the C515C-8E OTP version additionally provides two features:

- The wake-up from software power down mode can, additionally to the external pin P3.2/$\overline{\text{INT0}}$ wake-up capability, also be triggered alternatively by a second pin P4.7/RXDC.
- For power consumption reasons the on-chip CAN controller can be switched off.

Table 1 Differences in Internal Program Memory of the C505 MCUs

Device	Internal Program Memory	
	ROM	**OTP**
C515C-LM	–	–
C515C-8RM	64 Kbytes	–
C515C-8EM	–	64 Kbytes

Note: The term C515C refers to all versions described within this document unless otherwise noted.

Ordering Information

The ordering code for Infineon Technologies' microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set
- The specified temperature rage
- The package and the type of delivery

For the available ordering codes for the C515C please refer to the "**Product information Microcontrollers**", which summarizes all available microcontroller variants.

Note: The ordering codes for the Mask-ROM versions are defined for each product after verification of the respective ROM code.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number P-MQFP-80-1	I/O[1)]	Function
$\overline{PE}$/SWD	75	I	**$\overline{Power\ saving\ mode\ enable}$ / Start watchdog timer** A low level on this pin allows the software to enter the power down, idle and slow down mode. In case the low level is also seen during reset, the watchdog timer function is off on default. Use of the software controlled power saving modes is blocked, when this pin is held on high level. A high level during reset performs an automatic start of the watchdog timer immediately after reset. When left unconnected this pin is pulled high by a weak internal pull-up resistor.
V_{SSCLK}	13	–	**Ground (0 V) for on-chip oscillator** This pin is used for ground connection of the on-chip oscillator circuit.
V_{DDCLK}	14	–	**Supply voltage for on-chip oscillator** This pin is used for power supply of the on-chip oscillator circuit.
V_{DDE1} V_{DDE2}	32 68	–	**Supply voltage for I/O ports** These pins are used for power supply of the I/O ports during normal, idle, and power down mode.
V_{SSE1} V_{SSE2}	35 70	–	**Ground (0 V) for I/O ports** These pins are used for ground connections of the I/O ports during normal, idle, and power down mode.
V_{DD1}	33	–	**Supply voltage for internal logic** This pins is used for the power supply of the internal logic circuits during normal, idle, and power down mode.
V_{SS1}	34	–	**Ground (0 V) for internal logic** This pin is used for the ground connection of the internal logic circuits during normal, idle, and power down mode.

CPU

The C515C is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44% one-byte, 41% two-byte, and 15% three-byte instructions. With a 6 MHz crystal, 58% of the instructions are executed in 1 µs (10 MHz: 600 ns).

PSW

Special Function Register (D0$_H$) Reset Value: 00$_H$

Bit No.	MSB							LSB	
	D7$_H$	D6$_H$	D5$_H$	D4$_H$	D3$_H$	D2$_H$	D1$_H$	D0$_H$	
D0$_H$	CY	AC	F0	RS1	RS0	OV	F1	P	PSW

Bit	Function
CY	Carry Flag Used by arithmetic instruction.
AC	Auxiliary Carry Flag Used by instructions which execute BCD operations.
F0	General Purpose Flag
RS1 RS0	Register Bank select control bits These bits are used to select one of the four register banks.
OV	Overflow Flag Used by arithmetic instruction.
F1	General Purpose Flag
P	Parity Flag Set/cleared by hardware after each instruction to indicate an odd/even number of “one” bits in the accumulator, i.e. even parity.

RS1	RS0	Function
0	0	Bank 0 selected, data address 00$_H$-07$_H$
0	1	Bank 1 selected, data address 08$_H$-0F$_H$
1	0	Bank 2 selected, data address 10$_H$-17$_H$
1	1	Bank 3 selected, data address 18$_H$-1F$_H$

Enhanced Hooks Emulation Concept

The Enhanced Hooks Emulation Concept of the C500 microcontroller family is a new, innovative way to control the execution of C500 MCUs and to gain extensive information on the internal operation of the controllers. Emulation of on-chip ROM based programs is possible, too.

Each production chip has built-in logic for the support of the Enhanced Hooks Emulation Concept. Therefore, no costly bond-out chips are necessary for emulation. This also ensure that emulation and production chips are identical.

The Enhanced Hooks Technology, which requires embedded logic in the C500 allows the C500 together with an EH-IC to function similar to a bond-out chip. This simplifies the design and reduces costs of an ICE-system. ICE-systems using an EH-IC and a compatible C500 are able to emulate all operating modes of the different versions of the C500 microcontrollers. This includes emulation of ROM, ROM with code rollover and ROMless modes of operation. It is also able to operate in single step mode and to read the SFRs after a break.

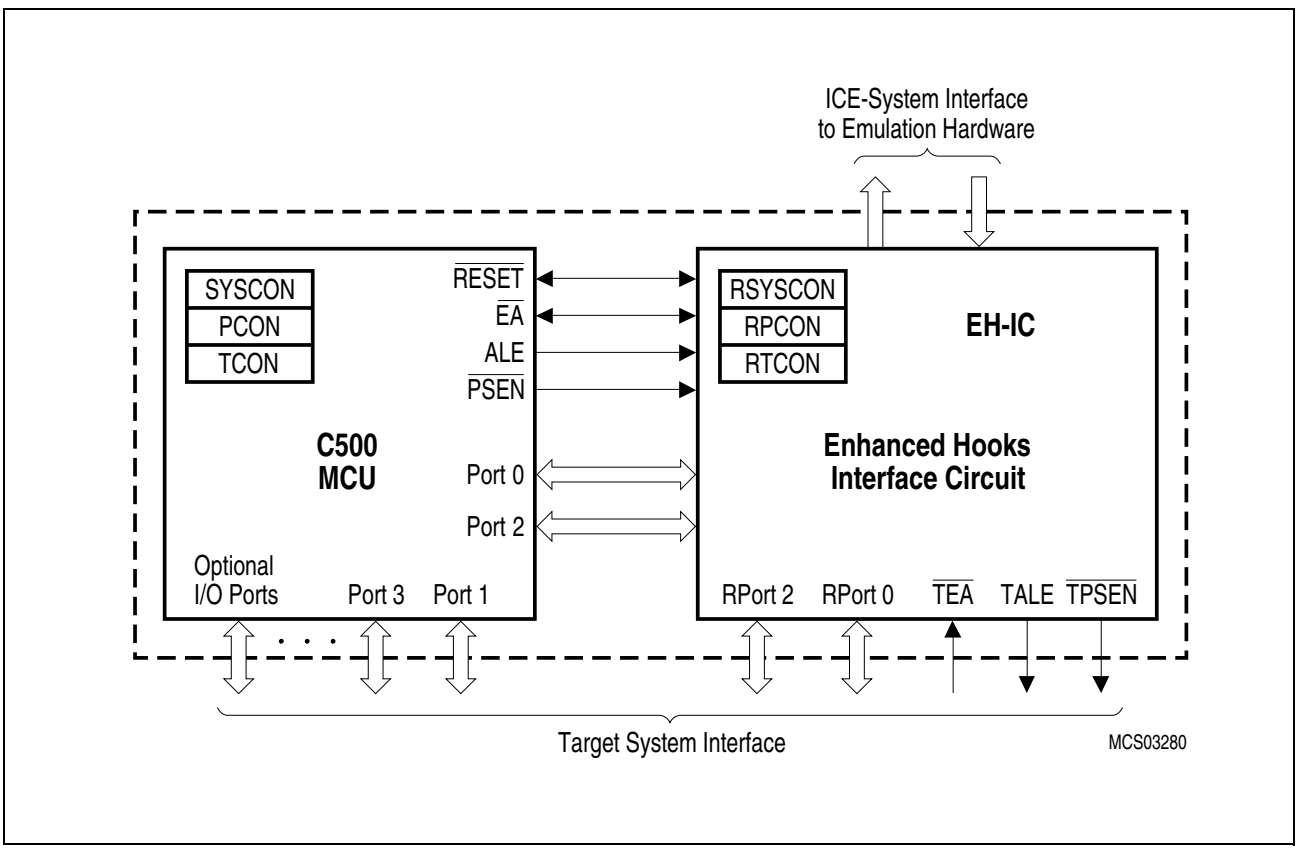

Figure 9 Basic C500 MCU Enhanced Hooks Concept Configuration

Port 0, port 2 and some of the control lines of the C500 based MCU are used by Enhanced Hooks Emulation Concept to control the operation of the device during emulation and to transfer informations about the program execution and data transfer between the external emulation hardware (ICE-system) and the C500 MCU.

Table 4 Special Function Registers - Functional Block (cont'd)

Block	Symbol	Name	Addr	Contents after Reset
Serial Channel	ADCON0[1]	A/D Converter Control Register 0	**$D8_H$**[2]	00_H
	PCON[1]	Power Control Register	87_H	00_H
	SBUF	Serial Channel Buffer Register	99_H	XX_H[3]
	SCON	Serial Channel Control Register	**98_H**[2]	00_H
	SRELL	Serial Channel Reload Register, low byte	AA_H	$D9_H$
	SRELH	Serial Channel Reload Register, high byte	BA_H	$XXXXXX11_B$[3]
CAN Controller	CR	Control Register	$F700_H$	101_H
	SR	Status Register	$F701_H$	XX_H[6]
	IR	Interrupt Register	$F702_H$	XX_H[6]
	BTR0	Bit Timing Register Low	$F704_H$	UU_H[6]
	BTR1	Bit Timing Register High	$F705_H$	$0UUUUUUU_B$[6]
	GMS0	Global Mask Short Register Low	$F706_H$	UU_H[6]
	GMS1	Global Mask Short Register High	$F707_H$	$UUU11111_B$[6]
	UGML0	Upper Global Mask Long Register Low	$F708_H$	UU_H[6]
	UGML1	Upper Global Mask Long Register High	$F709_H$	UU_H[6]
	LGML0	Lower Global Mask Long Register Low	$F70A_H$	UU_H[6]
	LGML1	Lower Global Mask Long Register High	$F70B_H$	$UUUUU000_B$[6]
	UMLM0	Upper Mask of Last Message Register Low	$F70C_H$	UU_H[6]
	UMLM1	Upper Mask of Last Message Register High	$F70D_H$	UU_H[6]
	LMLM0	Lower Mask of Last Message Register Low	$F70E_H$	UU_H[6]
	LMLM1	Lower Mask of Last Message Register High	$F70F_H$	$UUUUU000_B$[6]
		Message Object Registers:		
	MCR0	Message Control Register Low	$F7n0_H$[5]	UU_H[6]
	MCR1	Message Control Register High	$F7n1_H$[5]	UU_H[6]
	UAR0	Upper Arbitration Register Low	$F7n2_H$[5]	UU_H[6]
	UAR1	Upper Arbitration Register High	$F7n3_H$[5]	UU_H[6]
	LAR0	Lower Arbitration Register Low	$F7n4_H$[5]	UU_H[6]
	LAR1	Lower Arbitration Register High	$F7n5_H$[5]	$UUUUU000_B$[6]
	MCFG	Message Configuration Register	$F7n6_H$[5]	$UUUUUU00_B$[6]
	DB0n	Message Data Byte 0	$F7n7_H$[5]	XX_H[6]
	DB1n	Message Data Byte 1	$F7n8_H$[5]	XX_H[6]
	DB2n	Message Data Byte 2	$F7n9_H$[5]	XX_H[6]
	DB3n	Message Data Byte 3	$F7nA_H$[5]	XX_H[6]
	DB4n	Message Data Byte 4	$F7nB_H$[5]	XX_H[6]
	DB5n	Message Data Byte 5	$F7nC_H$[5]	XX_H[6]
	DB6n	Message Data Byte 6	$F7nD_H$[5]	XX_H[6]
	DB7n	Message Data Byte 7	$F7nE_H$[5]	XX_H[6]

Table 5 Contents of the SFRs, SFRs in Numeric Order of their Addresses

Addr.	Register	Content after Reset[1]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
80_H[2]	P0	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
81_H	SP	07_H	.7	.6	.5	.4	.3	.2	.1	.0
82_H	DPL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
83_H	DPH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
86_H	WDTREL	00_H	WDT PSEL	.6	.5	.4	.3	.2	.1	.0
87_H	PCON	00_H	SMOD	PDS	IDLS	SD	GF1	GF0	PDE	IDLE
88_H[2]	TCON	00_H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
88_H[3]	PCON1[4]	$0XXX\text{-}XXXX_B$	EWPD	–	–	–	–	–	–	–
88_H[3]	PCON1[5]	$0XX0\text{-}XXXX_B$	EWPD	–	–	WS	–	–	–	–
89_H	TMOD	00_H	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
$8A_H$	TL0	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8B_H$	TL1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8C_H$	TH0	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8D_H$	TH1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
90_H[2]	P1	FF_H	T2	CLK-OUT	T2EX	$\overline{INT2}$	INT6	INT5	INT4	$\overline{INT3}$
91_H	XPAGE	00_H	.7	.6	.5	.4	.3	.2	.1	.0
92_H	DPSEL	$XXXX\text{-}X000_B$	–	–	–	–	–	.2	.1	.0
93_H	SSCCON	07_H	SCEN	TEN	MSTR	CPOL	CPHA	BRS2	BRS1	BRS0
94_H	STB	XX_H	.7	.6	.5	.4	.3	.2	.1	.0
95_H	SRB	XX_H	.7	.6	.5	.4	.3	.2	.1	.0
96_H	SSCMOD	00_H	LOOPB	TRIO	0	0	0	0	0	LSBSM
98_H[2]	SCON	00_H	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
99_H	SBUF	XX_H	.7	.6	.5	.4	.3	.2	.1	.0
$9A_H$	IEN2	$X00X\text{-}X00X_B$	–	–	EX8	EX7	–	ESSC	ECAN	–
$A0_H$[2]	P2	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
$A8_H$[2]	IEN0	00_H	EAL	WDT	ET2	ES	ET1	EX1	ET0	EX0
$A9_H$	IP0	00_H	OWDS	WDTS	.5	.4	.3	.2	.1	.0

Table 5 Contents of the SFRs, SFRs in Numeric Order of their Addresses (cont'd)

Addr.	Register	Content after Reset[1)]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AA_H	SRELL	$D9_H$	.7	.6	.5	.4	.3	.2	.1	.0
AB_H	SCF	XXXX-XX00$_B$	–	–	–	–	–	–	WCOL	TC
AC_H	SCIEN	XXXX-XX00$_B$	–	–	–	–	–	–	WCEN	TCEN
$B0_H$[2)]	P3	FF_H	RD	WR	T1	T0	INT1	INT0	TxD	RxD
$B1_H$	SYSCON[4)]	X010-XX01$_B$	–	PMOD	EALE	RMAP	–	–	XMAP1	XMAP0
$B1_H$	SYSCON[5)]	X010-X001$_B$	–	PMOD	EALE	RMAP	–	CSWO	XMAP1	XMAP0
$B8_H$[2)]	IEN1	00_H	EXEN2	SWDT	EX6	EX5	EX4	EX3	EX2	EADC
$B9_H$	IP1	0X00-0000$_B$	PDIR	–	.5	.4	.3	.2	.1	.0
BA_H	SRELH	XXXX-XX11$_B$	–	–	–	–	–	–	.1	.0
$C0_H$[2)]	IRCON	00_H	EXF2	TF2	IEX6	IEX5	IEX4	IEX3	IEX2	IADC
$C1_H$	CCEN	00_H	COCAH3	COCAL3	COCAH2	COCAL2	COCAH1	COCAL1	COCAH0	COCAL0
$C2_H$	CCL1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C3_H$	CCH1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C4_H$	CCL2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C5_H$	CCH2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C6_H$	CCL3	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C7_H$	CCH3	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C8_H$[2)]	T2CON	00_H	T2PS	I3FR	I2FR	T2R1	T2R0	T2CM	T2I1	T2I0
CA_H	CRCL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CB_H	CRCH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CC_H	TL2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CD_H	TH2	00_H	.7	.6	.5	.4	.3	.2	.1	.0

Table 5 Contents of the SFRs, SFRs in Numeric Order of their Addresses (cont'd)

Addr.	Register	Content after Reset[1)]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$D0_H$[2)]	PSW	00_H	CY	AC	F0	RS1	RS0	OV	F1	P
$D8_H$[2)]	ADCON0	00_H	BD	CLK	ADEX	BSY	ADM	MX2	MX1	MX0
$D9_H$	ADDATH	00_H	.9	.8	.7	.6	.5	.4	.3	.2
DA_H	ADDATL	$00XX\text{-}XXXX_B$	.1	.0	–	–	–	–	–	–
DB_H	P6	–	.7	.6	.5	.4	.3	.2	.1	.0
DC_H	ADCON1	$0XXX\text{-}X000_B$	ADCL	–	–	–	0	MX2	MX1	MX0
$E0_H$[2)]	ACC	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$E8_H$[2)]	P4	FF_H	RXDC	TXDC	$\overline{INT8}$	$\overline{SLS}$	STO	SRI	SCLK	$\overline{ADST}$
$F0_H$[2)]	B	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$F8_H$[2)]	P5	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
$F8_H$[2)]	DIR5[6)]	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
FA_H	P7	$XXXX\text{-}XXX1_B$	–	–	–	–	–	–	–	$\overline{INT7}$
FC_H	VR0[7)8)]	$C5_H$	1	1	0	0	0	1	0	1
FD_H	VR1[7)8)]	95_H	1	0	0	1	0	1	0	1
FE_H	VR2[7)8)]	02_H[9)]	0	0	0	0	0	0	1	0

1) "X" means that the value is undefined and the location is reserved.

2) Bit-addressable special function registers

3) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.

4) This SFR is available in the C515C-8R and C515C-L.

5) This SFR is available in the C515C-8E.

6) This SFR is a mapped SFR. For accessing this SFR, bit PDIR in SFR IP1 must be set.

7) This SFR is a mapped SFR. For accessing this SFR, bit RMAP in SFR SYSCON must be set.

8) These SFRs are read-only registers (C515C-8E only).

9) The content of this SFR varies with the actual step of the C515C-8E (e.g. 01_H for the first step).

Table 6 Contents of the CAN Registers in Numeric Order of their Addresses

Addr. n = 1 to F_H[1)]	Register	Content after Reset[2)]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$F700_H$	CR	01_H	TEST	CCE	0	0	EIE	SIE	IE	INIT
$F701_H$	SR	XX_H	BOFF	EWRN	–	RXOK	TXOK	LEC2	LEC1	LEC0
$F702_H$	IR	XX_H	INTID							
$F704_H$	BTR0	UU_H	SJW		BRP					
$F705_H$	BTR1	$0UUU.UUUU_B$	0	TSEG2			TSEG1			
$F706_H$	GMS0	UU_H	ID28-21							
$F707_H$	GMS1	$UUU1.1111_B$	ID20-18			1	1	1	1	1
$F708_H$	UGML0	UU_H	ID28-21							
$F709_H$	UGML1	UU_H	ID20-13							
$F70A_H$	LGML0	UU_H	ID12-5							
$F70B_H$	LGML1	$UUUU.U000_B$	ID4-0					0	0	0
$F70C_H$	UMLM0	UU_H	ID28-21							
$F70D_H$	UMLM1	UU_H	ID20-18			ID17-13				
$F70E_H$	LMLM0	UU_H	ID12-5							
$F70F_H$	LMLM1	$UUUU.U000_B$	ID4-0					0	0	0
$F7n0_H$	MCR0	UU_H	MSGVAL		TXIE		RXIE		INTPND	
$F7n1_H$	MCR1	UU_H	RMTPND		TXRQ		MSGLST CPUUPD		NEWDAT	
$F7n2_H$	UAR0	UU_H	ID28-21							
$F7n3_H$	UAR1	UU_H	ID20-18			ID17-13				
$F7n4_H$	LAR0	UU_H	ID12-5							
$F7n5_H$	LAR1	$UUUU.U000_B$	ID4-0					0	0	0
$F7n6_H$	MCFG	$UUUU.UU00_B$	DLC				DIR	XTD	0	0
$F7n7_H$	DB0n	XX_H	.7	.6	.5	.4	.3	.2	.1	.0
$F7n8_H$	DB1n	XX_H	.7	.6	.5	.4	.3	.2	.1	.0
$F7n9_H$	DB2n	XX_H	.7	.6	.5	.4	.3	.2	.1	.0
$F7nA_H$	DB3n	XX_H	.7	.6	.5	.4	.3	.2	.1	.0
$F7nB_H$	DB4n	XX_H	.7	.6	.5	.4	.3	.2	.1	.0

Timer 2 Compare Modes

The compare function of a timer/register combination operates as follows: the 16-bit value stored in a compare or compare/capture register is compared with the contents of the timer register; if the count value in the timer register matches the stored value, an appropriate output signal is generated at a corresponding port pin and an interrupt can be generated.

Compare Mode 0

In compare mode 0, upon matching the timer and compare register contents, the output signal changes from low to high. It goes back to a low level on timer overflow. As long as compare mode 0 is enabled, the appropriate output pin is controlled by the timer circuit only and writing to the port will have no effect. **Figure 13** shows a functional diagram of a port circuit when used in compare mode 0. The port latch is directly controlled by the timer overflow and compare match signals. The input line from the internal bus and the write-to-latch line of the port latch are disconnected when compare mode 0 is enabled.

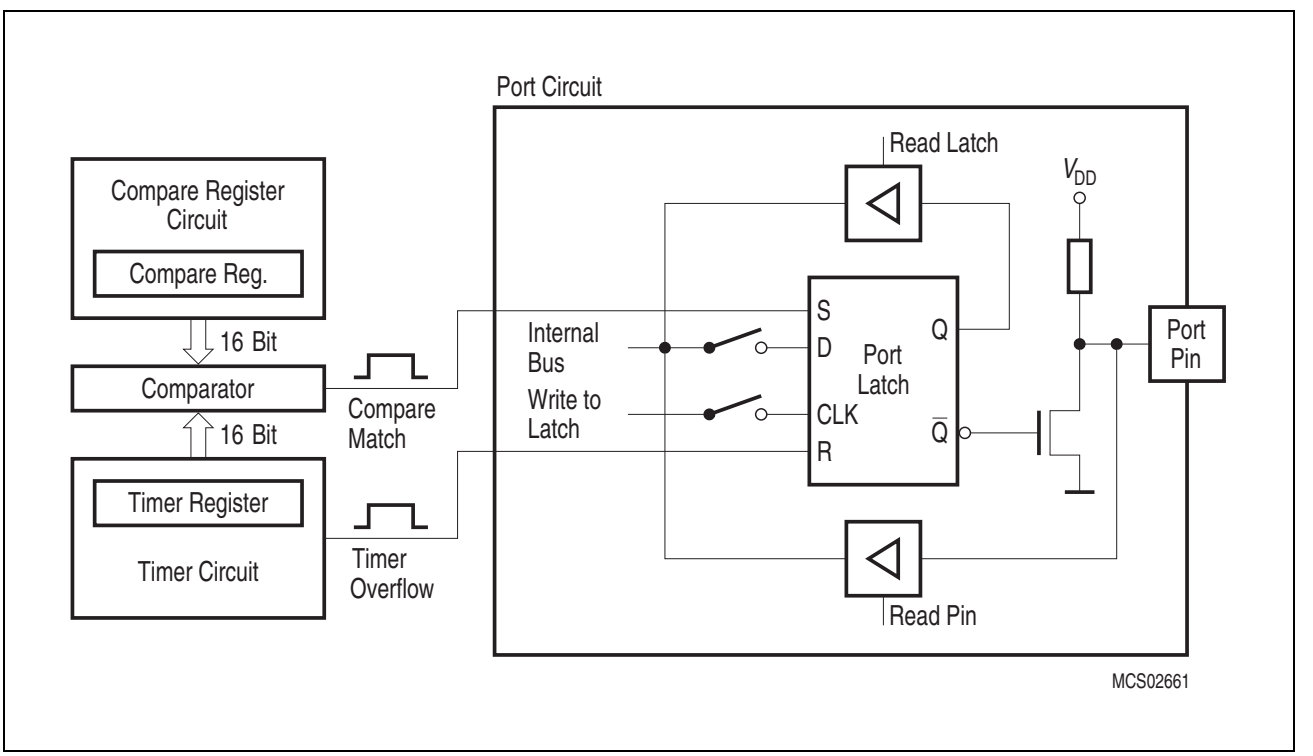

Figure 13 Port Latch in Compare Mode 0

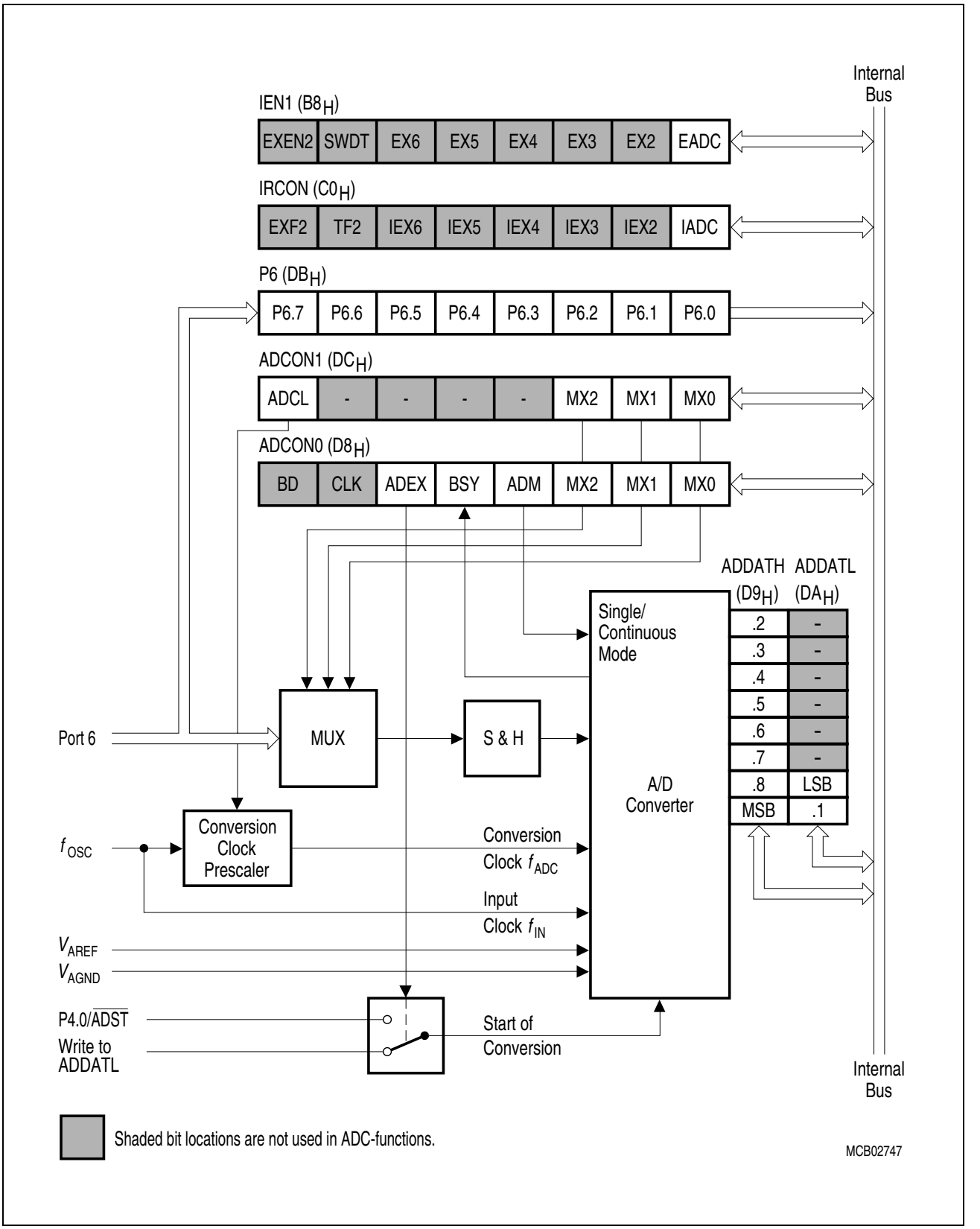

Figure 19 A/D Converter Block Diagram

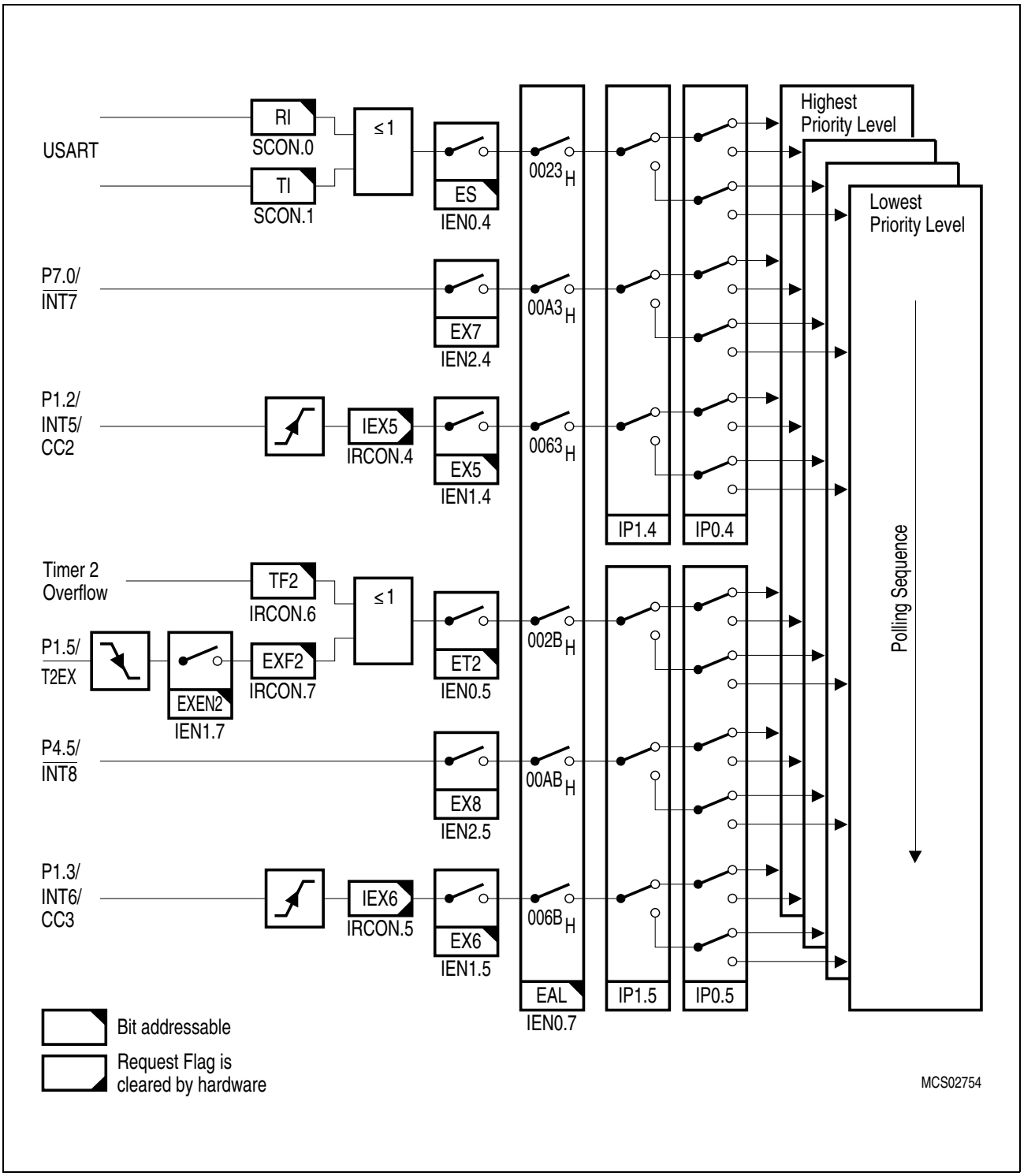

Figure 22 Interrupt Request Sources (Part 3)

Table 10 Interrupt Source and Vectors

Interrupt Source	Interrupt Vector Address	Interrupt Request Flags
External Interrupt 0	0003_H	IE0
Timer 0 Overflow	$000B_H$	TF0
External Interrupt 1	0013_H	IE1
Timer 1 Overflow	$001B_H$	TF1
Serial Channel	0023_H	RI / TI
Timer 2 Overflow / Ext. Reload	$002B_H$	TF2 / EXF2
A/D Converter	0043_H	IADC
External Interrupt 2	$004B_H$	IEX2
External Interrupt 3	0053_H	IEX3
External Interrupt 4	$005B_H$	IEX4
External Interrupt 5	0063_H	IEX5
External Interrupt 6	$006B_H$	IEX6
Wake-up from power-down mode	$007B_H$	–
CAN controller	$008B_H$	–
External Interrupt 7	$00A3_H$	–
External Interrupt 8	$00AB_H$	–
SSC interface	0093_H	TC / WCOL

Table 12 Pin Definitions and Functions in Programming Mode (cont'd)

Symbol	Pin Number	I/O[1)]	Function
A0/A8 - A7/A15	38 - 45	I	**Address lines** P2.0-7 are used as multiplexed address input lines A0-A7 and A8-A15. A8-A15 must be latched with PALE.
$\overline{\text{PSEN}}$	47	I	**$\overline{\text{Program store enable}}$** This input must be at static "0" level during the whole programming mode.
$\overline{\text{PROG}}$	48	I	**$\overline{\text{Programming mode write strobe}}$** This input is used in programming mode as a write strobe for OTP memory program and lock bit write operations. During basic programming mode selection a low level must be applied to $\overline{\text{PROG}}$.
$\overline{\text{EA}}/V_{\text{PP}}$	49	I	**$\overline{\text{External Access}}$ / Programming voltage** This pin must be at 11.5 V (V_{PP}) voltage level during programming of an OTP memory byte or lock bit. During an OTP memory read operation this pin must be at high level (V_{IH}). This pin is also used for basic programming mode selection. At basic programming mode selection a low level must be applied to $\overline{\text{EA}}/V_{\text{PP}}$.
D0 - 7	52 - 58	I/O	**Data lines 0-7** During programming mode, data bytes are read or written from or to the C515C-8E via the bidirectional D0-7 which are located at port 0.
V_{SS}	13, 34, 35, 51, 70	–	**Circuit ground potential** must be applied to these pins in programming mode.
V_{DD}	14, 32, 33, 50, 69	–	**Power supply terminal** must be applied to these pins in programming mode.
N.C.	2-12, 20-31, 46, 60-67, 69, 71-80	–	**Not Connected** These pins should not be connected in programming mode.

1) I = Input; O = Output

Table 13 Access Modes Selection

Access Mode	$\overline{EA}$/ V_{PP}	$\overline{PROG}$	$\overline{PRD}$	PMSEL		Address (Port 2)	Data (Port 0)
				1	0		
Program OTP memory byte	V_{PP}	⊓	H	H	H	A0-7 A8-15	D0-7
Read OTP memory byte	V_{IH}	H	⊓				
Program OTP lock bits	V_{PP}	⊓	H	H	L	–	D1, D0 see Table 14
Read OTP lock bits	V_{IH}	H	⊓				
Read OTP version byte	V_{IH}	H	⊓	L	H	Byte addr. of version byte	D0-7

C515C-8E Lock Bits Programming / Read

The C515C-8E has two programmable lock bits which, when programmed according Table 14, provide four levels of protection for the on-chip OTP code memory. The state of the lock bits can also be read.

DC Characteristics (Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltages all except $\overline{EA}$, $\overline{RESET}$, $\overline{HWPD}$ $\overline{EA}$ pin $\overline{RESET}$ and $\overline{HWPD}$ pins Port 5 in CMOS mode	 V_{IL} V_{IL1} V_{IL2} V_{ILC}	 -0.5 -0.5 -0.5 -0.5	 0.2 V_{DD} - 0.1 0.2 V_{DD} - 0.3 0.2 V_{DD} + 0.1 0.3 V_{DD}	V	–
Input high voltages all except XTAL2, $\overline{RESET}$, and $\overline{HWPD}$) XTAL2 pin $\overline{RESET}$ and $\overline{HWPD}$ pins Port 5 in CMOS mode	 V_{IH} V_{IH1} V_{IH2} V_{IHC}	 0.2 V_{DD} + 0.9 0.7 V_{DD} 0.6 V_{DD} 0.7 V_{DD}	 V_{DD} + 0.5 V_{DD} + 0.5 V_{DD} + 0.5 V_{DD} + 0.5	V	–
Output low voltages Ports 1, 2, 3, 4, 5, 7 (incl. CMOS) Port 0, ALE, $\overline{PSEN}$, $\overline{CPUR}$ P4.1, P4.3 in push-pull mode	 V_{OL} V_{OL1} V_{OL3}	 – – –	 0.45 0.45 0.45	V	 I_{OL} = 1.6 mA[1)] I_{OL} = 3.2 mA[1)] I_{OL} = 3.75 mA[1)]
Output high voltages Ports 1, 2, 3, 4, 5, 7 Port 0 in external bus mode, ALE, $\overline{PSEN}$, $\overline{CPUR}$ Port 5 in CMOS mode P4.1, P4.3 in push-pull mode	 V_{OH} V_{OH2} V_{OHC} V_{OH3}	 2.4 0.9 V_{DD} 2.4 0.9 V_{DD} 0.9 V_{DD} 0.9 V_{DD}	 – – – – – –	V	 I_{OH} = -80 µA I_{OH} = -10 µA I_{OH} = -800 µA I_{OH} = -80 µA[2)] I_{OH} = -800 µA I_{OH} = -833 µA
Logic 0 input current Ports 1, 2, 3, 4, 5, 7	I_{IL}	-10	-70	µA	V_{IN} = 0.45 V
Logical 0-to-1 transition current Ports 1, 2, 3, 4, 5, 7	I_{TL}	-65	-650	µA	V_{IN} = 2 V
Input leakage current Port 0, $\overline{EA}$, P6, $\overline{HWPD}$, AIN0-7	I_{LI}	–	±1	µA	0.45 < V_{IN} < V_{DD}
Input low current To $\overline{RESET}$ for reset XTAL2 $\overline{PE}$/SWD	 I_{LI2} I_{LI3} I_{LI4}	 – – –	 -100 -15 -20	µA	 V_{IN} = 0.45 V V_{IN} = 0.45 V V_{IN} = 0.45 V
Pin capacitance	C_{IO}	–	10	pF	f_c = 1 MHz, T_A = 25 °C
Overload current	I_{OV}	–	±5	mA	[3)4)]
Programming voltage	V_{PP}	10.9	12.1	V	11.5 V ± 5%

Power Supply Current

Parameter			Sym-bol	Limit Values		Unit	Test Condition
				typ.[1]	max.[2]		
Active mode	C515C-8R/ C515C-LM	6 MHz 10 MHz	I_{DD}	11.97 18.81	13.74 21.10	mA	[3]
	C515C-8E	6 MHz 10 MHz	I_{DD}	11.3 17.66	12.94 20.10	mA	
Idle mode	C515C-8R/ C515C-LM	6 MHz 10 MHz	I_{DD}	6.9 10.46	7.87 11.87	mA	[4]
	C515C-8E	6 MHz 10 MHz	I_{DD}	3.95 4.71	4.70 5.50	mA	
Active mode with slow-down enabled	C515C-8R/ C515C-LM	6 MHz 10 MHz	I_{DD}	4.06 4.62	5.03 5.75	mA	[5]
	C515C-8E	6 MHz 10 MHz	I_{DD}	4.01 4.65	4.77 5.53	mA	
Idle mode with slow-down enabled	C515C-8R/ C515C-LM	6 MHz 10 MHz	I_{DD}	3.54 3.86	4.46 4.90	mA	[6]
	C515C-8E	6 MHz 10 MHz	I_{DD}	3.62 4.14	4.21 4.77	mA	
Power-down mode	C515C-8R/ C515C-LM		I_{PD}	26	42.9	µA	V_{DD} = 2 … 5.5 V [7]
	C515C-8E		I_{PD}	11.14	30	µA	
At $\overline{EA}/V_{PP}$ in programming mode	C515C-8E		I_{DDP}	–	30	mA	–

[1] The typical I_{DD} values are periodically measured at T_A = +25 °C and V_{DD} = 5 V but not 100% tested.

[2] The maximum I_{DD} values are measured under worst case conditions (T_A = 0 °C or -40 °C and V_{DD} = 5.5 V)

[3] I_{DD} (active mode) is measured with:
XTAL2 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{DD} - 0.5 V; XTAL1 = N.C.;
$\overline{EA}$ = $\overline{PE}$/SWD = Port 0 = Port 6 = V_{DD}; $\overline{HWPD}$ = V_{DD}; $\overline{RESET}$ = V_{SS}; all other pins are disconnected.

[4] I_{DD} (idle mode) is measured with all output pins disconnected and with all peripherals disabled;
XTAL2 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{DD} - 0.5 V; XTAL1 = N.C.;
$\overline{RESET}$ = V_{DD}; $\overline{EA}$ = V_{SS}; Port0 = V_{DD}; all other pins are disconnected;

[5] I_{DD} (active mode with slow-down mode) is measured with all output pins disconnected and with all peripherals disabled;
XTAL2 driven with t_{CLCH}, t_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{DD} - 0.5 V; XTAL1 = N.C.;
$\overline{RESET}$ = V_{DD}; all other pins are disconnected; the microcontroller is put into slow-down mode by software.

SSC Interface Characteristics

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Clock Cycle Time: Master Mode Slave Mode	 t_{SCLK} t_{SCLK}	 0.4 1.0	 – –	 µs µs
Clock high time	t_{SCH}	360	–	ns
Clock low time	t_{SCL}	360	–	ns
Data output delay	t_D	–	100	ns
Data output hold	t_{HO}	0	–	ns
Data input setup	t_S	100	–	ns
Data input hold	t_{HI}	100	–	ns
TC bit set delay	t_{DTC}	–	8 CLP	ns

External Clock Drive at XTAL2

Parameter	Symbol	CPU Clock = 10 MHz Duty cycle 0.4 to 0.6		Variable CPU Clock 1/CLP = 2 to 10 MHz		Unit
		min.	max.	min.	max.	
Oscillator period	CLP	100	100	100	500	ns
High time	TCL_H	40	–	40	CLP - TCL_L	ns
Low time	TCL_L	40	–	40	CLP - TCL_H	ns
Rise time	t_R	–	12	–	12	ns
Fall time	t_F	–	12	–	12	ns
Oscillator duty cycle	DC	0.4	0.6	40 / CLP	1 - 40 / CLP	–
Clock cycle	TCL	40	60	CLP × DC_{min}	CLP × DC_{max}	ns

Note: The 10 MHz values in the tables are given as an example for a typical duty cycle variation of the oscillator clock from 0.4 to 0.6.

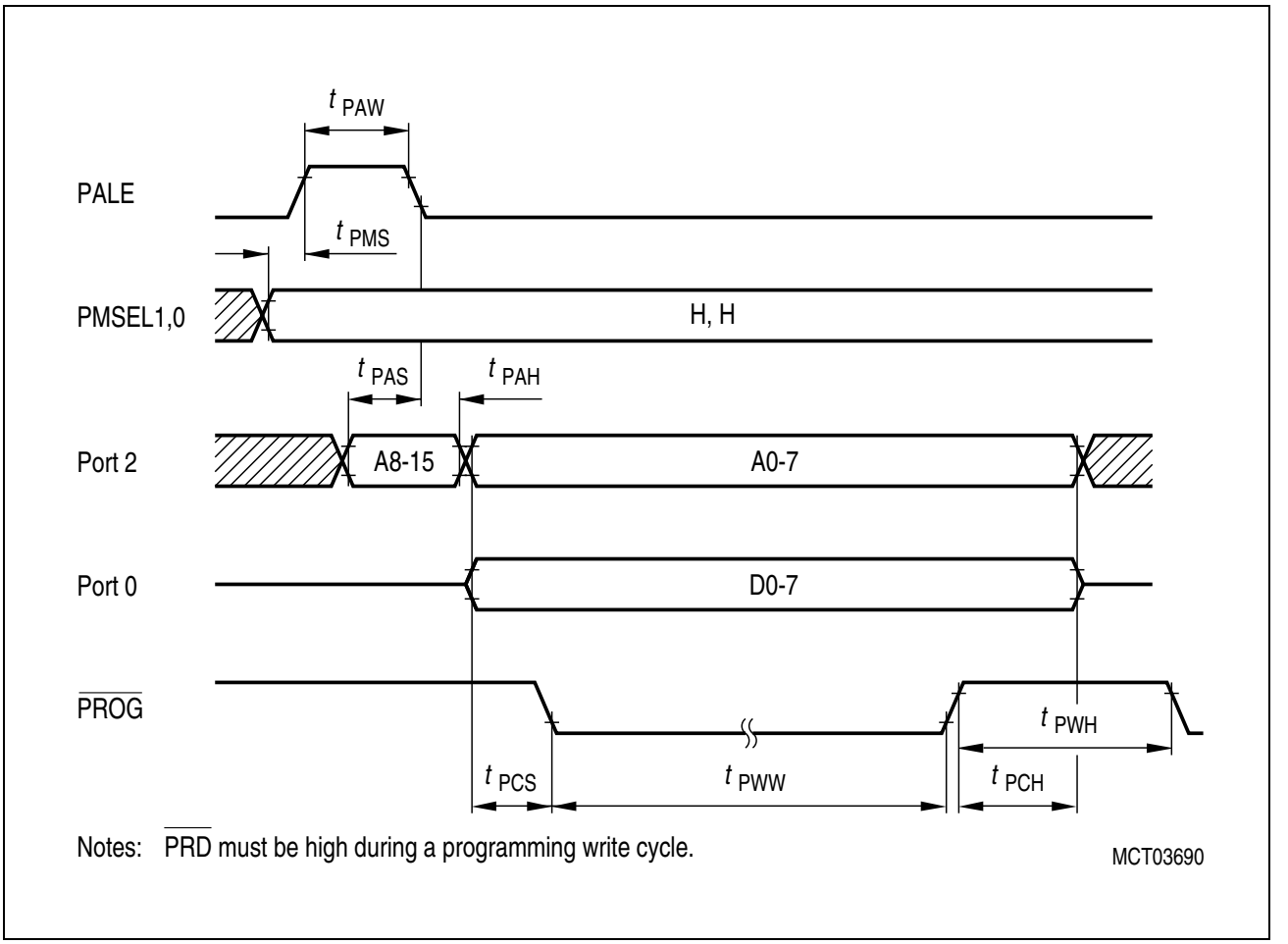

Figure 35 Programming Code Byte - Write Cycle Timing

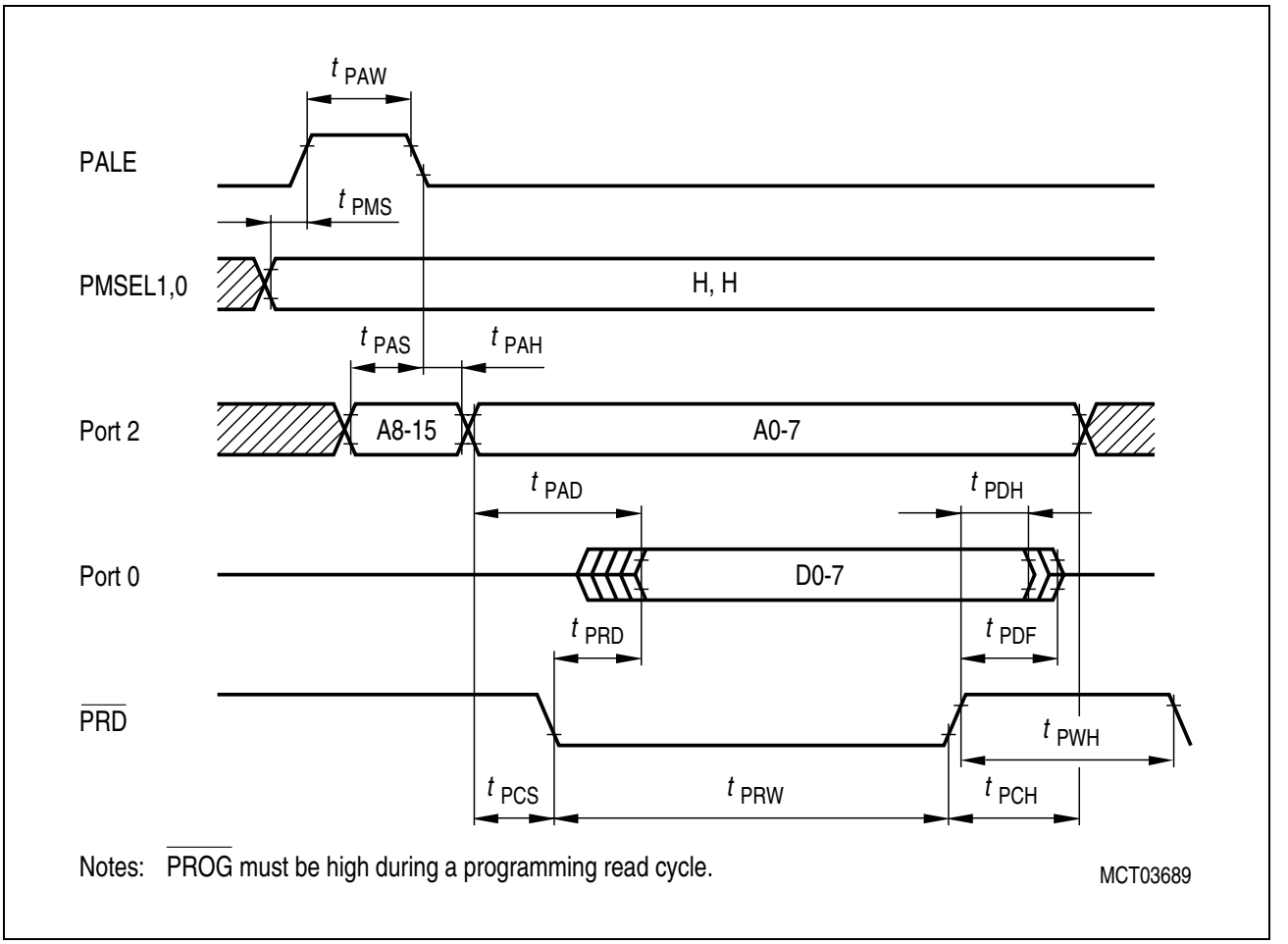

Figure 36 Verify Code Byte - Read Cycle Timing