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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C500
Core Size	8-Bit
Speed	10MHz
Connectivity	CANbus, EBI/EMI, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	49
Program Memory Size	64KB (64K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	2.5K x 8
Voltage - Supply (Vcc/Vdd)	4.25V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-QFP
Supplier Device Package	P-MQFP-80-1
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/c515c8emcafxuma2

Data Sheet, Feb. 2003

C515C

8-Bit Single-Chip Microcontroller

Microcontrollers

Infineon technologies

Never stop thinking.

C515C Data Sheet

Revision History: 2003-02

Previous Version: 2000-08

Page	Subjects (major changes since last revision)

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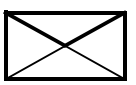


- Eight ports: 48 + 1 digital I/O lines, 8 analog inputs
  - Quasi-bidirectional port structure (8051 compatible)
  - Port 5 selectable for bidirectional port structure (CMOS voltage levels)
- Full-CAN controller on-chip
  - 256 register/data bytes are located in external data memory area
  - max. 1 MBaud at 8 - 10 MHz operating frequency
- Three 16-bit timer/counters
  - Timer 2 can be used for compare/capture functions
- 10-bit A/D converter with multiplexed inputs and built-in self calibration
- Full duplex serial interface with programmable baudrate generator (USART)
- SSC synchronous serial interface (SPI compatible)
  - Master and slave capable
  - Programmable clock polarity/clock-edge to data phase relation
  - LSB/MSB first selectable
  - 2.5 MHz transfer rate at 10 MHz operating frequency
- Seventeen interrupt vectors, at four priority levels selectable
- Extended watchdog facilities
  - 15-bit programmable watchdog timer
  - Oscillator watchdog
- Power saving modes
  - Slow-down mode
  - Idle mode (can be combined with slow-down mode)
  - Software power-down mode with wake-up capability through $\overline{\text{INT0}}$ or RXDC pin
  - Hardware power-down mode
- CPU running condition output pin
- ALE can be switched off
- Multiple separate V_{DD}/V_{SS} pin pairs
- P-MQFP-80-1 package
- Temperature Ranges:
  SAB-C515C versions: T_A = 0 to 70 °C
  SAF-C515C versions: T_A = -40 to 85 °C
  SAH-C515C versions: T_A = -40 to 110 °C

Note: Versions for extended temperature range -40 °C to 110 °C (SAH-C515C) are available on request.

The C515C is an enhanced, upgraded version of the SAB 80C515A 8-bit microcontroller which additionally provides a full CAN interface, a SPI compatible synchronous serial interface, extended power save provisions, additional on-chip RAM, 64K of on-chip program memory, two new external interrupts and RFI related improvements. With a maximum external clock rate of 10 MHz it achieves a 600 ns instruction cycle time (1 µs at 6 MHz).

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number P-MQFP-80-1	I/O[1)]	Function
ALE	48	O	The **Address Latch Enable** output is used for latching the address into external memory during normal operation. It is activated every six oscillator periods, except during an external data memory access. ALE can be switched off when the program is executed internally.
$\overline{EA}$	49	I	**$\overline{\text{External Access Enable}}$** When held high, the C515C executes instructions always from the internal ROM. When held low, the C515C fetches all instructions from external program memory. *Note: For the ROM protection version $\overline{EA}$ pin is latched during reset.*
P0.0-P0.7	52-59	I/O	**Port 0** is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application it uses strong internal pullup resistors when issuing 1's. Port 0 also outputs the code bytes during program verification in the C515C. External pullup resistors are required during program verification.
P5.0-P5.7	67-60	I/O	**Port 5** is an 8-bit quasi-bidirectional I/O port with internal pullup resistors. Port 5 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 5 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 5 can also be switched into a bidirectional mode, in which CMOS levels are provided. In this bidirectional mode, each port 5 pin can be programmed individually as input or output.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number P-MQFP-80-1	I/O[1)]	Function
V_{DDEXT}	50	–	**Supply voltage for external access pins** This pin is used for power supply of the I/O ports and control signals which are used during external accesses (for Port 0, Port 2, ALE, $\overline{PSEN}$, P3.6/$\overline{WR}$, and P3.7/$\overline{RD}$).
V_{SSEXT}	51	–	**Ground (0 V) for external access pins** This pin is used for the ground connection of the I/O ports and control signals which are used during external accesses (for Port 0, Port 2, ALE, $\overline{PSEN}$, P3.6/$\overline{WR}$, and P3.7/$\overline{RD}$).
N.C.	2, 71	–	**Not connected** These pins should not be connected.

1) I = Input; O = Output

Control of XRAM/CAN Controller Access

The XRAM in the C515C is a memory area that is logically located at the upper end of the external memory space, but is integrated on the chip. Because the XRAM and the CAN controller is used in the same way as external data memory the same instruction types (MOVX) must be used for accessing the XRAM. Two bits in SFR SYSCON, XMAP0 and XMAP1, control the accesses to the XRAM and the CAN controller.

SYSCON
Special Function Register **($B1_H$)** **C515C-8R Reset Value: $X010XX01_B$**
C515C-8E Reset Value: $X010X001_B$

Bit No.	MSB							LSB	
	7	6	5	4	3	2	1	0	
$B1_H$	–	PMOD	EALE	RMAP	–	CSWO	XMAP1	XMAP0	SYSCON

The function of the shaded bits is not described in this section.

Bit	Function
XMAP1	XRAM/CAN controller visible access control Control bit for $\overline{RD}$/$\overline{WR}$ signals during XRAM/CAN Controller accesses. If addresses are outside the XRAM/CAN controller address range or if XRAM is disabled, this bit has no effect. XMAP1 = 0: The signals $\overline{RD}$ and $\overline{WR}$ are not activated during accesses to the XRAM/CAN Controller XMAP1 = 1: Ports 0, 2 and the signals $\overline{RD}$ and $\overline{WR}$ are activated during accesses to XRAM/CAN Controller. In this mode, address and data information during XRAM/CAN Controller accesses are visible externally.
XMAP0	Global XRAM/CAN controller access enable/disable control XMAP0 = 0: The access to XRAM and CAN controller is enabled. XMAP0 = 1: The access to XRAM and CAN controller is disabled (default after reset). All MOVX accesses are performed via the external bus. Further, this bit is hardware protected.

Bit XMAP0 is hardware protected. If it is reset once (XRAM/CAN controller access enabled) it cannot be set by software. Only a reset operation will set the XMAP0 bit again.

Table 3 Behaviour of P0/P2 and $\overline{RD}/\overline{WR}$ During MOVX Accesses

			XMAP1, XMAP0		
			00	**10**	**X1**
$\overline{EA}$ = 0	MOVX @DPTR	DPTR < XRAM/CAN address range	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used
		DPTR ≥ XRAMCAN address range	a) P0/P2→Bus ($\overline{RD}/\overline{WR}$-Data) b) $\overline{RD}/\overline{WR}$ inactive c) XRAM is used	a) P0/P2→Bus ($\overline{RD}/\overline{WR}$-Data) b) $\overline{RD}/\overline{WR}$ active c) XRAM is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used
	MOVX @ Ri	XPAGE < XRAMCAN addr. page range	a) P0→Bus P2→I/O b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used	a) P0→Bus P2→I/O b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used	a) P0→Bus P2→I/O b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used
		XPAGE ≥ XRAMCAN addr. page range	a) P0→Bus ($\overline{RD}/\overline{WR}$-Data) P2→I/O b) $\overline{RD}/\overline{WR}$ inactive c) XRAM is used	a) P0→Bus ($\overline{RD}/\overline{WR}$-Data only) P2→I/O b) $\overline{RD}/\overline{WR}$ active c) XRAM is used	a) P0→Bus P2→I/O b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used
$\overline{EA}$ = 1	MOVX @DPTR	DPTR < XRAM/CAN address range	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used
		DPTR ≥ XRAMCAN address range	a) P0/P2→I/0 b) $\overline{RD}/\overline{WR}$ inactive c) XRAM is used	a) P0/P2→Bus ($\overline{RD}/\overline{WR}$-Data) b) $\overline{RD}/\overline{WR}$ active c) XRAM is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used
	MOVX @ Ri	XPAGE < XRAMCAN addr. page range	a) P0→Bus P2→I/O b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used	a) P0→Bus P2→I/O b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used	a) P0→Bus P2→I/O b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used
		XPAGE ≥ XRAMCAN addr. page range	a) P2→I/O P0/P2→I/O b) $\overline{RD}/\overline{WR}$ inactive c) XRAM is used	a) P0→Bus ($\overline{RD}/\overline{WR}$-Data) P2→I/O b) $\overline{RD}/\overline{WR}$ active c) XRAM is used	a) P0→Bus P2→I/O b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used

modes compatible to 8051/C501 family

Timer / Counter 2 with Compare/Capture/Reload

The timer 2 of the C515C provides additional compare/capture/reload features, which allow the selection of the following operating modes:

- Compare: up to 4 PWM signals with 16-bit/600 ns resolution
- Capture: up to 4 high speed capture inputs with 600 ns resolution
- Reload: modulation of timer 2 cycle time

The block diagram in **Figure 12** shows the general configuration of timer 2 with the additional compare/capture/reload registers. The I/O pins which can used for timer 2 control are located as multifunctional port functions at port 1.

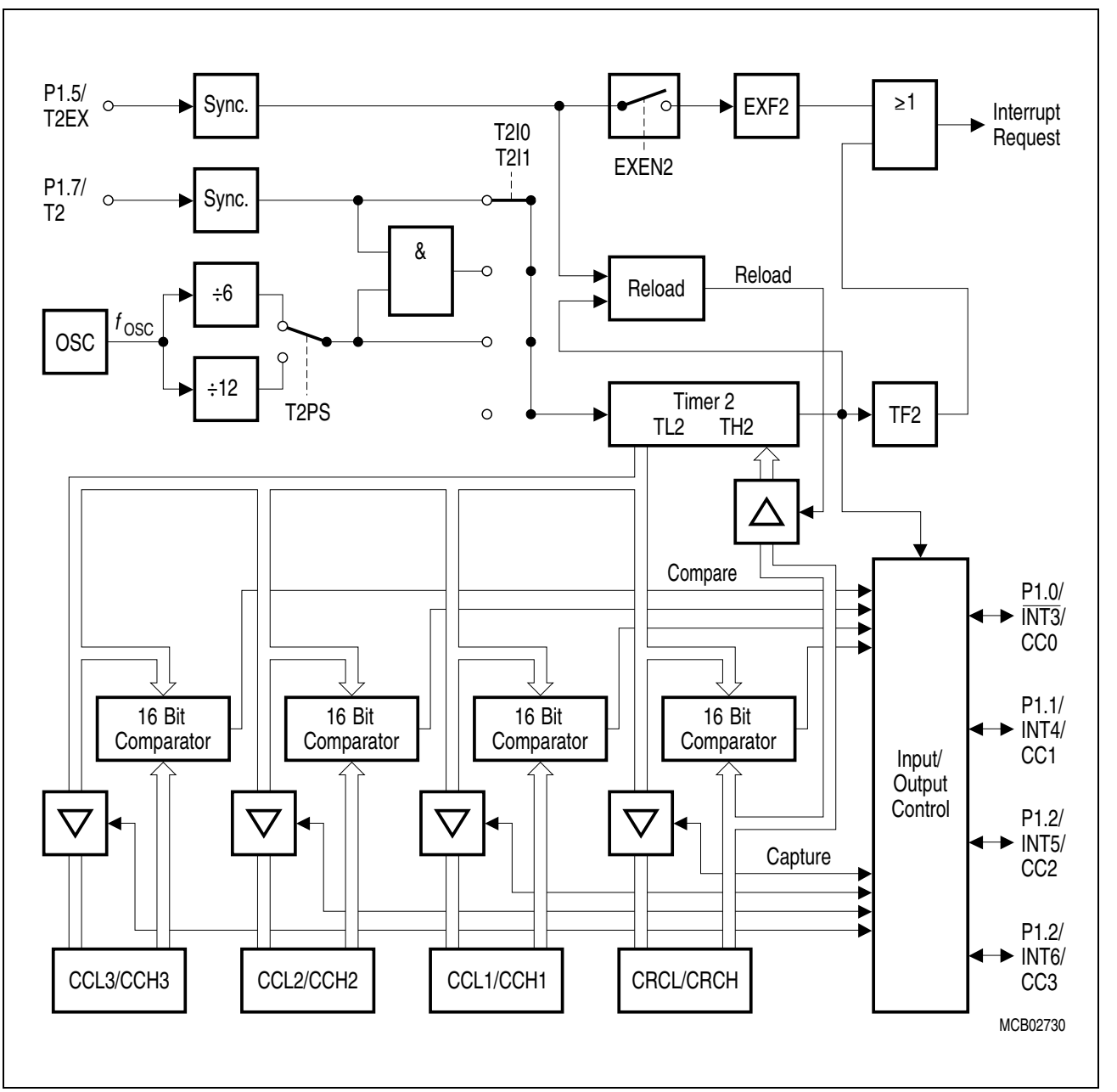


Figure 12 Timer 2 Block Diagram

Timer 2 Operating Modes

The timer 2, which is a 16-bit-wide register, can operate as timer, event counter, or gated timer. A roll-over of the count value in TL2/TH2 from all 1's to all 0's sets the timer overflow flag TF2 in SFR IRCON, which can generate an interrupt. The bits in register T2CON are used to control the timer 2 operation.

Timer Mode: In timer function, the count rate is derived from the oscillator frequency. A prescaler offers the possibility of selecting a count rate of 1/6 or 1/12 of the oscillator frequency.

Gated Timer Mode: In gated timer function, the external input pin T2 (P1.7) functions as a gate to the input of timer 2. If T2 is high, the internal clock input is gated to the timer. T2 = 0 stops the counting procedure. This facilitates pulse width measurements. The external gate signal is sampled once every machine cycle.

Event Counter Mode: In the event counter function. the timer 2 is incremented in response to a 1-to-0 transition at its corresponding external input pin T2 (P1.7). In this function, the external input is sampled every machine cycle. Since it takes two machine cycles (12 oscillator periods) to recognize a 1-to-0 transition, the maximum count rate is 1/12 of the oscillator frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it must be held for at least one full machine cycle.

Reload of Timer 2: Two reload modes are selectable:
In mode 0, when timer 2 rolls over from all 1's to all 0's, it not only sets TF2 but also causes the timer 2 registers to be loaded with the 16-bit value in the CRC register, which is preset by software.

In mode 1, a 16-bit reload from the CRC register is caused by a negative transition at the corresponding input pin P1.5/T2EX. This transition will also set flag EXF2 if bit EXEN2 in SFR IEN1 has been set.

Serial Interface (USART)

The serial port is full duplex and can operate in four modes (one synchronous mode, three asynchronous modes) as illustrated in **Table 8**.

Table 8 USART Operating Modes

Mode	SCON		Description
	SM0	SM1	
0	0	0	**Shift register mode, fixed baud rate** Serial data enters and exits through R×D; T×D outputs the shift clock; 8-bit are transmitted/received (LSB first)
1	0	1	**8-bit UART, variable baud rate** 10 bits are transmitted (through T×D) or received (at R×D)
2	1	0	**9-bit UART, fixed baud rate** 11 bits are transmitted (through T×D) or received (at R×D)
3	1	1	**9-bit UART, variable baud rate** Like mode 2

For clarification some terms regarding the difference between “baud rate clock” and “baud rate” should be mentioned. In the **asynchronous modes** the serial interfaces require a clock rate which is 16 times the baud rate for internal synchronization. Therefore, the baud rate generators/timers have to provide a “baud rate clock” (output signal in **Figure 15** to the serial interface which - there divided by 16 - results in the actual “baud rate”. Further, the abbreviation f_{OSC} refers to the oscillator frequency (crystal or external clock operation).

The variable baud rates for modes 1 and 3 of the serial interface can be derived either from timer 1 or from a dedicated baud rate generator (see **Figure 15**).

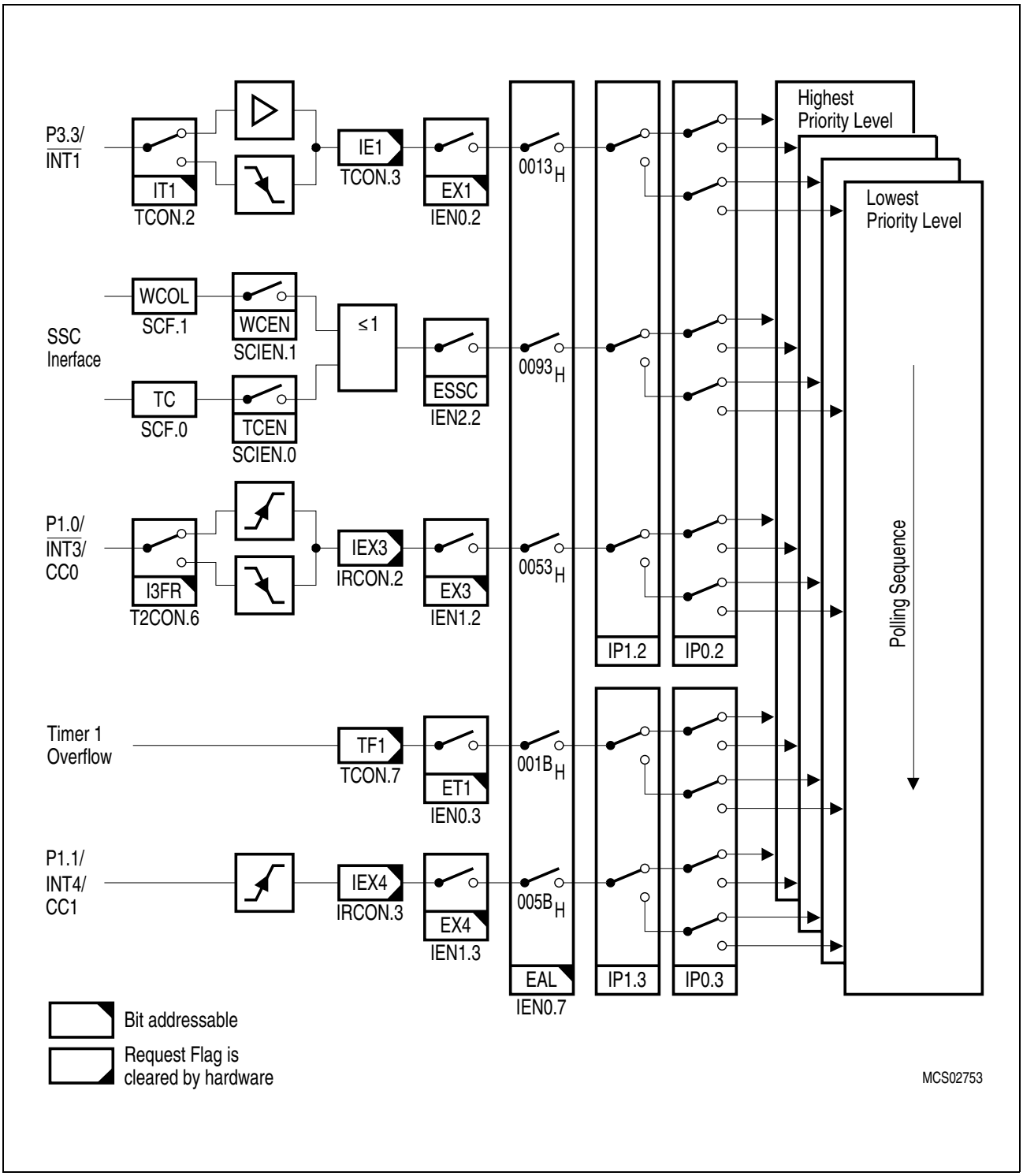


Figure 21 Interrupt Request Sources (Part 2)

Fail Save Mechanisms

The C515C offers two on-chip peripherals which monitor the program flow and ensure an automatic “fail-safe” reaction for cases where the controller’s hardware fails or the software hangs up:

- A programmable watchdog timer (WDT) with variable time-out period from 512 microseconds up to approx. 1.1 seconds at 6 MHz.
- An oscillator watchdog (OWD) which monitors the on-chip oscillator and forces the microcontroller into reset state in case the on-chip oscillator fails; it also provides the clock for a fast internal reset after power-on.

Programmable Watchdog Timer

The watchdog timer in the C515C is a 15-bit timer, which is incremented by a count rate of $f_{OSC}/12$ up to $f_{OSC}/192$. For programming of the watchdog timer overflow rate, the upper 7 bit of the watchdog timer can be written. **Figure 23** shows the block diagram of the watchdog timer unit.

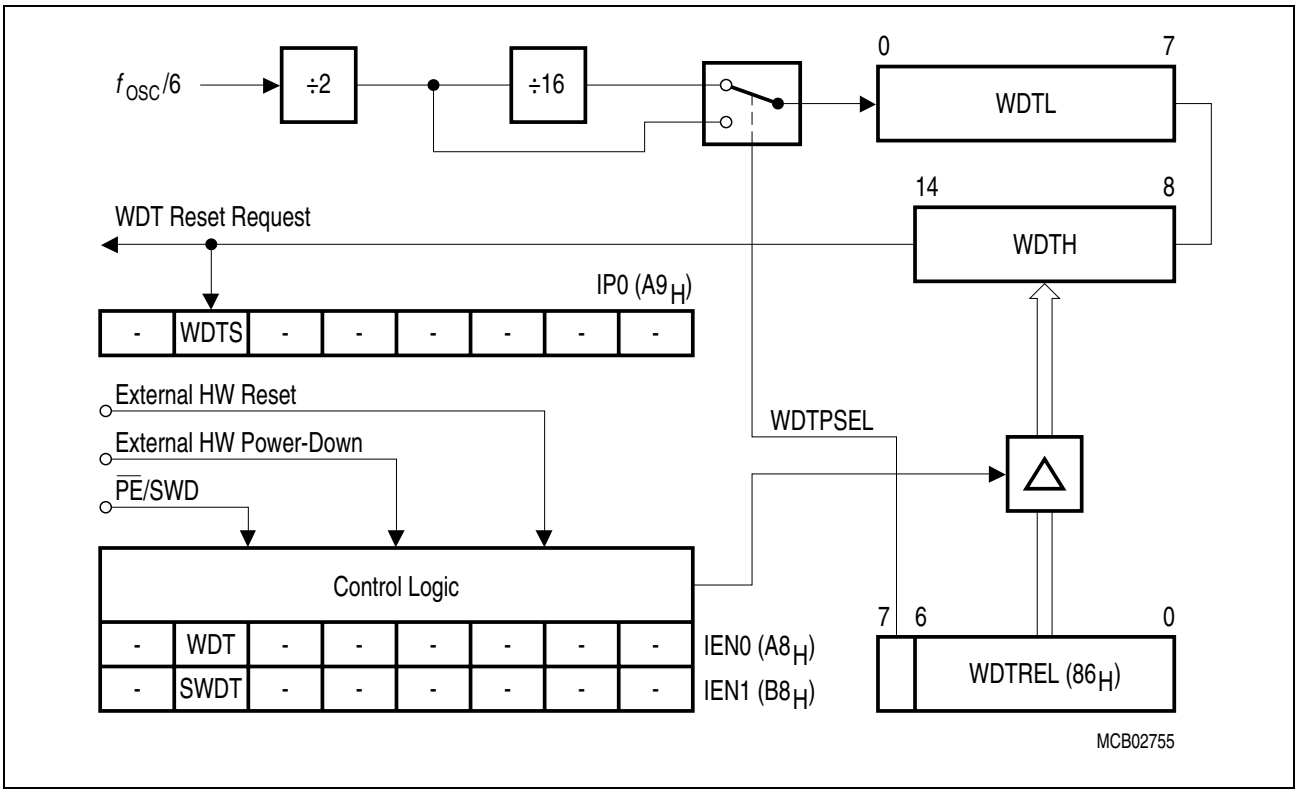


Figure 23 Block Diagram of the Programmable Watchdog Timer

The watchdog timer can be started by software (bit SWDT) or by hardware through pin $\overline{PE}$/SWD, but it cannot be stopped during active mode of the C515C. If the software fails to refresh the running watchdog timer an internal reset will be initiated on watchdog timer overflow. For refreshing of the watchdog timer the content of the SFR WDTREL is transferred to the upper 7-bit of the watchdog timer. The refresh sequence consists of

two consecutive instructions which set the bits WDT and SWDT each. The reset cause (external reset or reset caused by the watchdog) can be examined by software (flag WDTS). It must be noted, however, that the watchdog timer is halted during the idle mode and power down mode of the processor.

Oscillator Watchdog

The oscillator watchdog unit serves for four functions:

- **Monitoring of the on-chip oscillator's function**
  The watchdog supervises the on-chip oscillator's frequency; if it is lower than the frequency of the auxiliary RC oscillator in the watchdog unit, the internal clock is supplied by the RC oscillator and the device is brought into reset; if the failure condition disappears (i.e. the on-chip oscillator has a higher frequency than the RC oscillator), the part executes a final reset phase of typ. 1 ms in order to allow the oscillator to stabilize; then the oscillator watchdog reset is released and the part starts program execution again.
- **Fast internal reset after power-on**
  The oscillator watchdog unit provides a clock supply for the reset before the on-chip oscillator has started. The oscillator watchdog unit also works identically to the monitoring function.
- **Restart from the hardware power down mode**
  If the hardware power down mode is terminated the oscillator watchdog has to control the correct start-up of the on-chip oscillator and to restart the program. The oscillator watchdog function is only part of the complete hardware power down sequence; however, the watchdog works identically to the monitoring function.
- **Control of external wake-up from software power-down mode**
  When the software power-down mode is left by a low level at the P3.2/$\overline{\text{INT0}}$ pin, the oscillator watchdog unit assures that the microcontroller resumes operation (execution of the power-down wake-up interrupt) with the nominal clock rate. In the power-down mode the RC oscillator and the on-chip oscillator are stopped. Both oscillators are started again when power-down mode is released. When the on-chip oscillator has a higher frequency than the RC oscillator, the microcontroller starts operation after a final delay of typ. 1 ms in order to allow the on-chip oscillator to stabilize.

Table 11 Power Saving Modes Overview

Mode	Entering (2-Instruction Example)	Leaving by	Remarks
Idle mode	ORL PCON, #01_H ORL PCON, #20_H	Occurrence of an interrupt from a peripheral unit	CPU clock is stopped; CPU maintains their data; peripheral units are active (if enabled) and provided with clock
		Hardware Reset	
Software Power-Down Mode	ORL PCON, #02_H ORL PCON, #40_H	Hardware Reset	Oscillator is stopped; contents of on-chip RAM and SFR's are maintained;
		Short low pulse at pin P3.2/$\overline{INT0}$ (or P4.7/$\overline{RXDC}$, C515C-8E only)	
Hardware Power-Down Mode	$\overline{HWPD}$ = low	$\overline{HWPD}$ = high	C515C is put into its reset state and the oscillator is stopped; ports become floating outputs
Slow Down Mode	ORL PCON, #10_H	ANL PCON, #$0EF_H$ or Hardware Reset	Oscillator frequency is reduced to 1/32 of its nominal frequency

C515C-8E Pin Configuration in Programming Mode

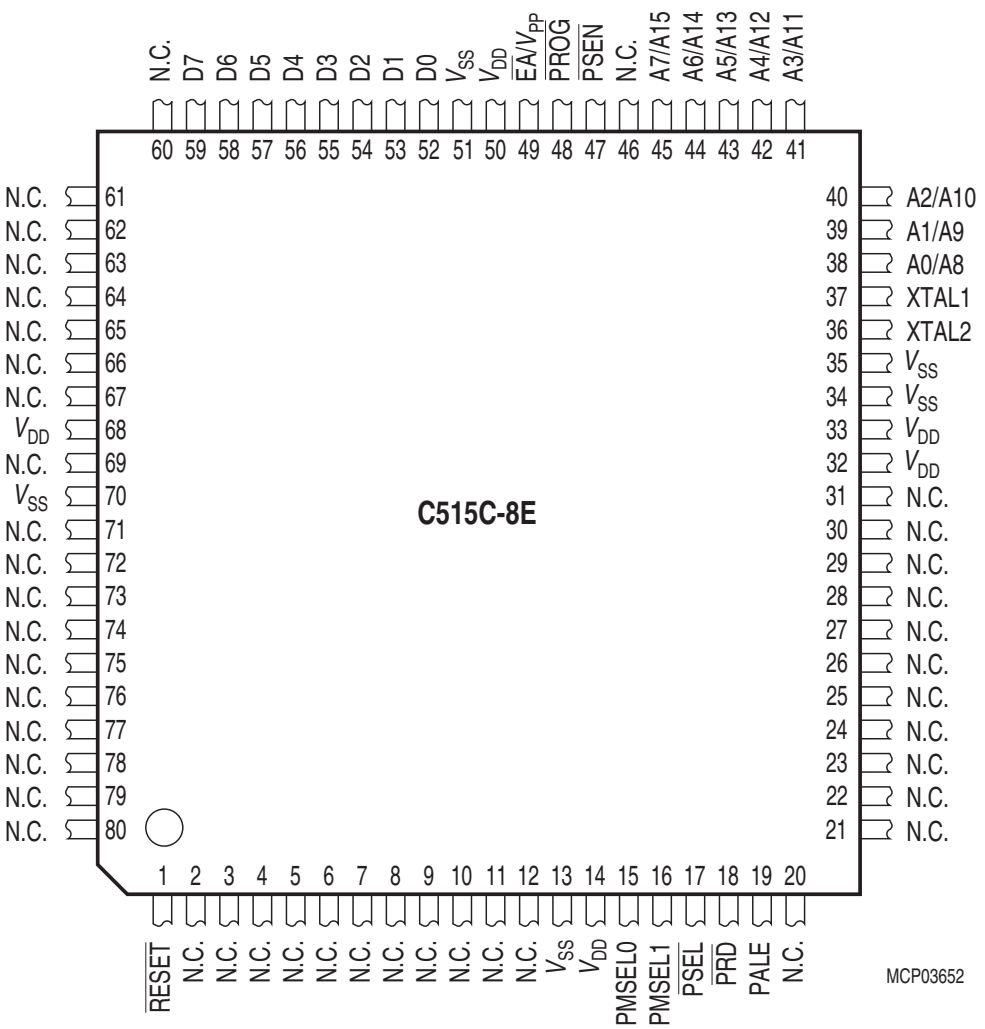


Figure 26 **P-MQFP-80-1 Pin Configuration of the C515C-8E in Programming Mode** (top view)

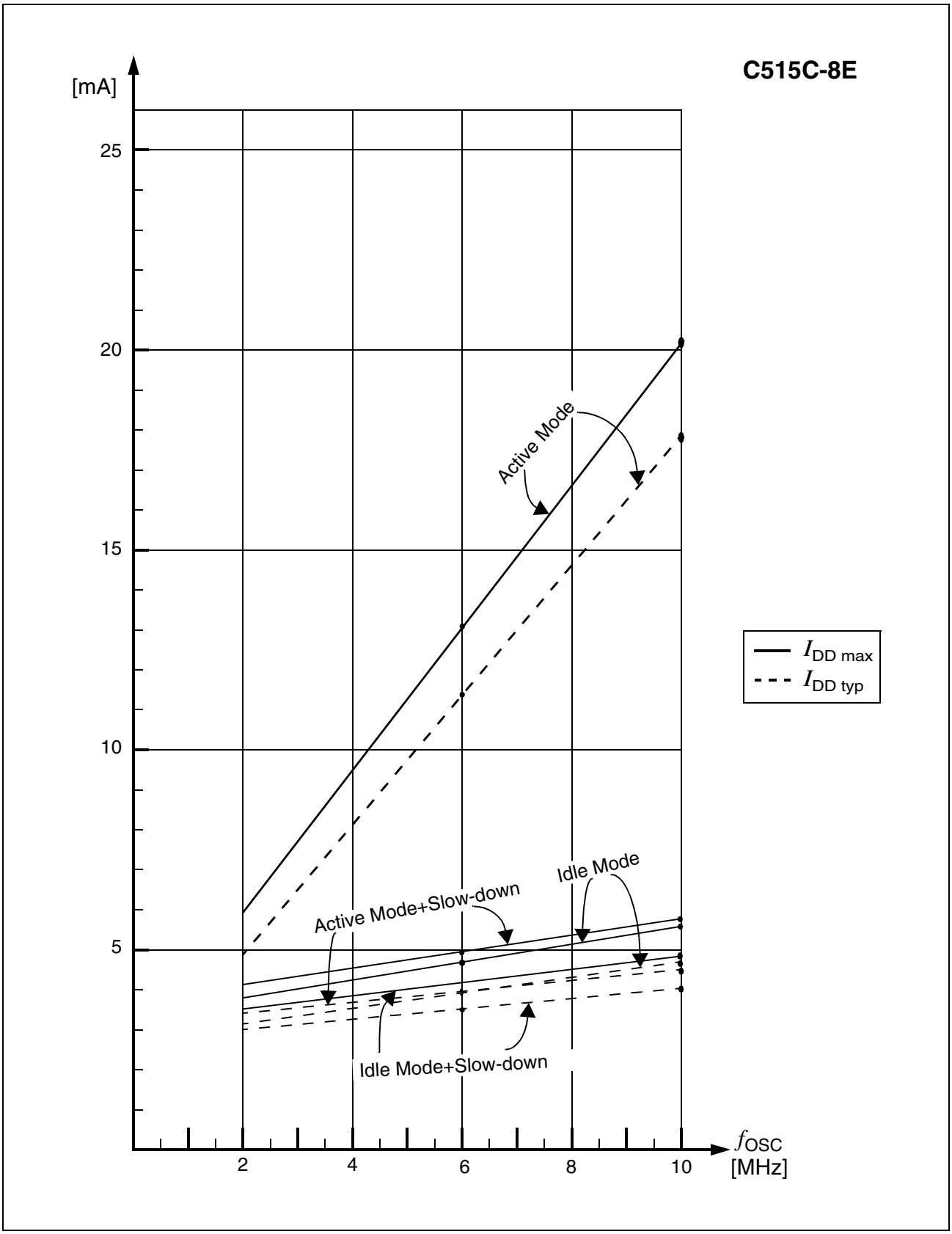


Figure 29 I_{DD} Diagrams of C515C-8E

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		10-MHz Clock Duty Cycle 0.4 to 0.6		Variable Clock 1/CLP= 2 MHz to 10 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	230	–	3 CLP - 70	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	230	–	3 CLP - 70	–	ns
Address hold after ALE	t_{LLAX2}	48	–	CLP - 15	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	150	–	2 CLP + TCL_{Hmin} - 90	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	80	–	CLP - 20	ns
ALE to valid data in	t_{LLDV}	–	267	–	4 CLP - 133	ns
Address to valid data in	t_{AVDV}	–	285	–	4 CLP + TCL_{Hmin} - 155	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	90	190	CLP + TCL_{Lmin} - 50	CLP + TCL_{Lmin} + 50	ns
Address valid to $\overline{WR}$	t_{AVWL}	103	–	2 CLP - 97	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	15	65	TCL_{Hmin} - 25	TCL_{Hmin} + 25	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	5	–	TCL_{Lmin} - 35	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	218	–	3 CLP + TCL_{Lmin} - 122	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	13	–	TCL_{Hmin} - 27	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

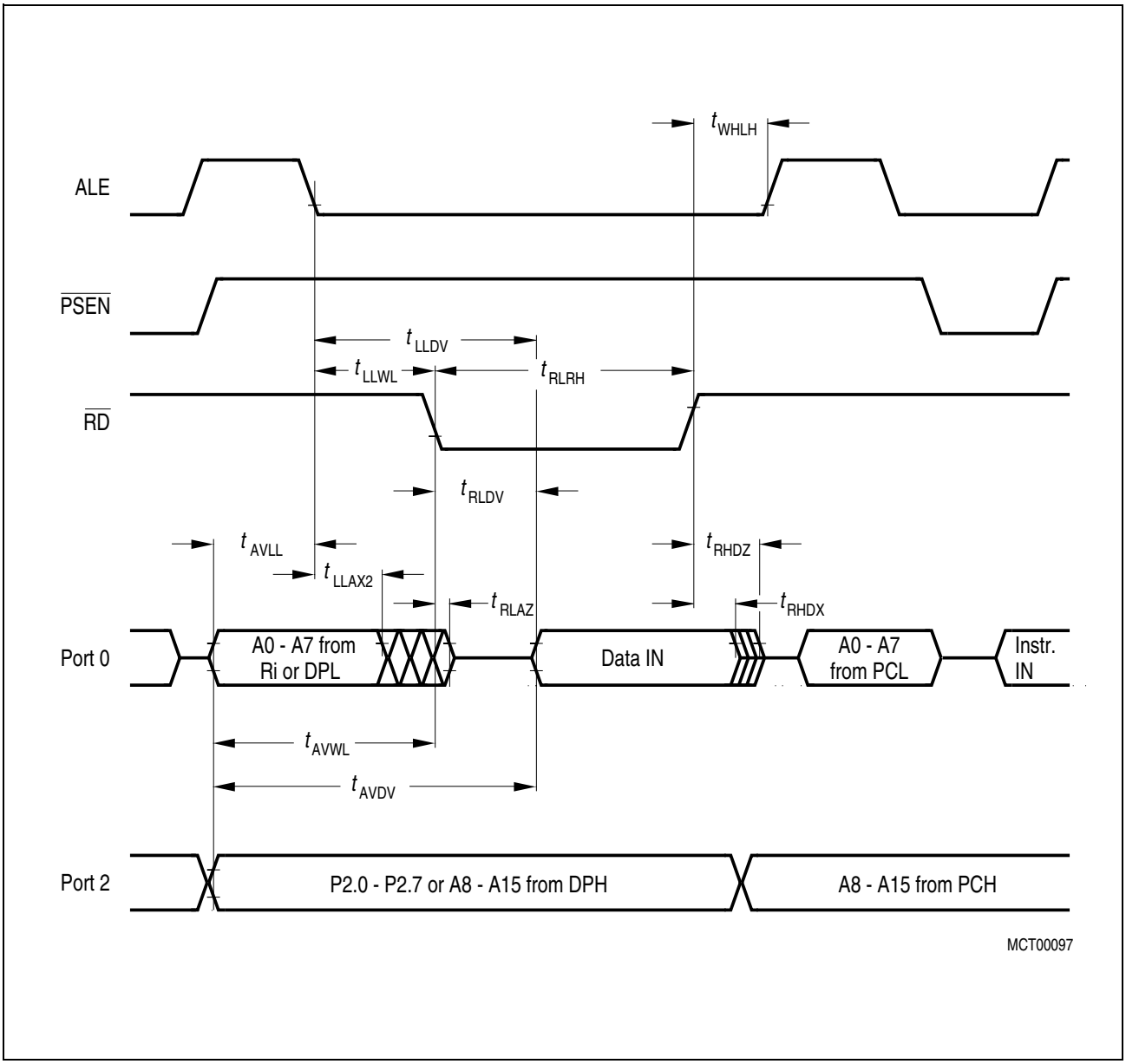


Figure 31 Data Memory Read Cycle

ROM/OTP Verification Characteristics for C515C-8R / C515C-8E

ROM Verification Mode 1 (C515C-8R)

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Address to valid data	t_{AVQV}	–	5 CLP	ns

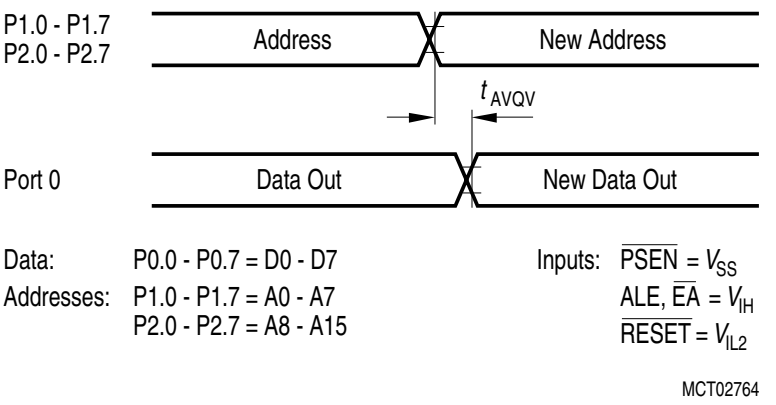
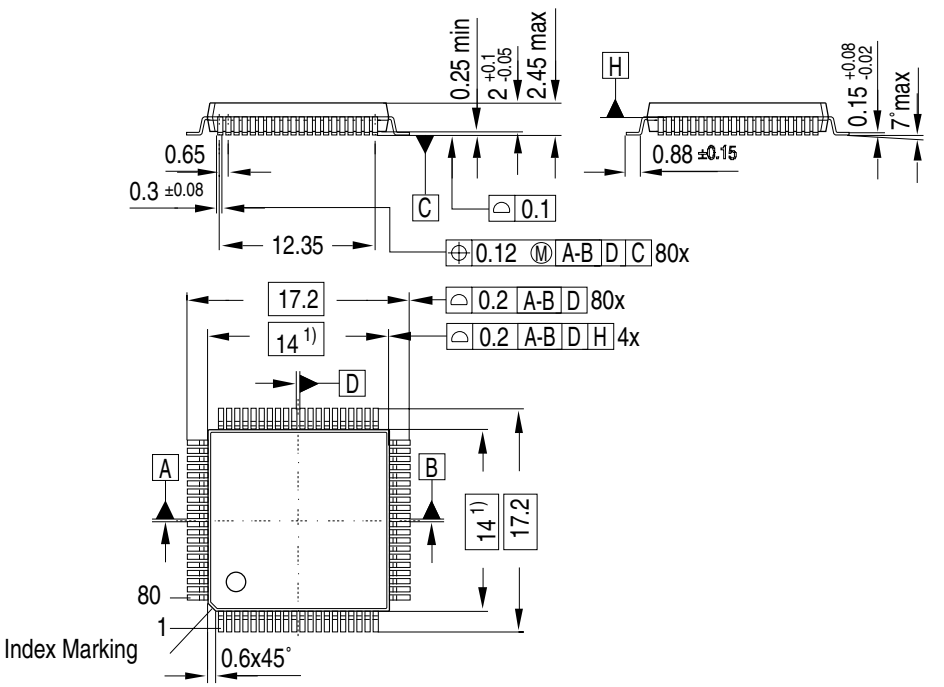


Figure 39 ROM Verification Mode 1

Package Outlines

P-MQFP-80-1
(Plastic Metric Quad Flat Package)



1) Does not include plastic or metal protrusions of 0.25 max per side

GPM05249

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: http://www.infineon.com/products.

SMD = Surface Mounted Device

Dimensions in mm