What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	27
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 10x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l062k8t6

2.1   Device overview

Table 1. Ultra-low-power STM32L062x8 device features and peripheral counts

Peripheral		STM32L062K8	STM32L062T8
Flash (Kbytes)		64	
Data EEPROM (Kbytes)		2	
RAM (Kbytes)		8	
AES		1	
Timers	General-purpose	3	
	Basic	1	
	LPTIMER	1	
RTC/SYSTICK/IWDG/WWDG		1/1/1/1	
Communication interfaces	SPI/I2S	3(2)[1]/0	
	I^{2}C	1	2
	USART	2	
	LPUART	0	1
	USB/(VDD_USB)	1/(0)	
GPIOs		27[2]	29
Clocks: HSE/LSE/HSI/MSI/LSI		0/1/1/1/1	
12-bit synchronized ADC Number of channels		1 10	
12-bit DAC Number of channels		1 1	
Comparators		2	
Capacitive sensing channels		14	
Max. CPU frequency		32 MHz	
Operating voltage		1.8 V to 3.6 V (down to 1.65 V at power-down) with BOR option 1.65 V to 3.6 V without BOR option	
Operating temperatures		Ambient temperature: –40 to +125 °C Junction temperature: –40 to +130 °C	
Packages		UFQFPN32, LQFP32	WLCSP36

1. 2 SPI interfaces are USARTs operating in SPI master mode.

2. LQFP32 has two GPIOs, less than UFQFPN32.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

Table 6. Temperature sensor calibration values

Calibration value name	Description	Memory address
TSENSE_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3 V	0x1FF8 007A - 0x1FF8 007B
TSENSE_CAL2	TS ADC raw data acquired at temperature of 130 °C V_{DDA}= 3 V	0x1FF8 007E - 0x1FF8 007F

3.12.1 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and Comparators. V_{REFINT} is internally connected to the ADC_IN17 input channel. It enables accurate monitoring of the V_{DD} value (when no external voltage, V_{REF+}, is available for ADC). The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 7. Internal voltage reference measured values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 25 °C V_{DDA} = 3 V	0x1FF8 0078 - 0x1FF8 0079

3.13 Digital-to-analog converter (DAC)

One 12-bit buffered DAC can be used to convert digital signal into analog voltage signal output. An optional amplifier can be used to reduce the output signal impedance.

This digital Interface supports the following features:

- One data holding register
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- DMA capability (including the underrun interrupt)
- External triggers for conversion
- Input reference voltage V_{REF+}

Four DAC trigger inputs are used in the STM32L062x8. The DAC channel is triggered through the timer update outputs that are also connected to different DMA channels.

3.18.2 Low-power Timer (LPTIM)

The low-power timer has an independent clock and is running also in Stop mode if it is clocked by LSE, LSI or an external clock. It is able to wakeup the devices from Stop mode.

This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous / one shot mode
- Selectable software / hardware input trigger
- Selectable clock source
    - Internal clock source: LSE, LSI, HSI or APB clock
    - External clock source over LPTIM input (working even with no internal clock source running, used by the Pulse Counter Application)
- Programmable digital glitch filter
- Encoder mode

3.18.3 Basic timer (TIM6)

This timer can be used as a generic 16-bit timebase. It is mainly used for DAC trigger generation.

3.18.4 SysTick timer

This timer is dedicated to the OS, but could also be used as a standard downcounter. It is based on a 24-bit downcounter with autoreload capability and a programmable clock source. It features a maskable system interrupt generation when the counter reaches '0'.

3.18.5 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 37 kHz internal RC and, as it operates independently of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. The counter can be frozen in debug mode.

3.18.6 Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.19 Communication interfaces

3.19.1 I^{2}C bus

Up to two I^{2}C interfaces (I2C1, I2C2) can operate in multimaster or slave modes.

Each I^{2}C interface can support Standard mode (Sm, up to 100 kbit/s), Fast mode (Fm, up to 400 kbit/s) and Fast Mode Plus (Fm+, up to 1 Mbit/s) with 20 mA output drive on some I/Os.

7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask) are also supported as well as programmable analog and digital noise filters.

Table 10. Comparison of I2C analog and digital filters

	Analog filter	**Digital filter**
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

In addition, I2C1 provides hardware support for SMBus 2.0 and PMBus 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. I2C1 also has a clock domain independent from the CPU clock, allowing the I2C1 to wake up the MCU from Stop mode on address match.

Each I2C interface can be served by the DMA controller.

Refer to *Table 11* for an overview of I2C interface features.

Table 11. STM32L062x8 I^{2}C implementation

I2C features[1]	I2C1	I2C2
7-bit addressing mode	X	X
10-bit addressing mode	X	X
Standard mode (up to 100 kbit/s)	X	X
Fast mode (up to 400 kbit/s)	X	X
Fast Mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X	X[2]
Independent clock	X	-
SMBus	X	-
Wakeup from STOP	X	-

1. X = supported.

2. See *Table 15: STM32L062x8 pin definitions on page 39* for the list of I/Os that feature Fast Mode Plus capability

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low energy consumption. Higher speed clock can be used to reach higher baudrates.

LPUART interface can be served by the DMA controller.

3.19.4 Serial peripheral interface (SPI)/Inter-integrated sound (I2S)

One SPI is able to communicate at up to 16 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

The USARTs with synchronous capability can also be used as SPI master.

The SPI can be served by the DMA controller.

Refer to *Table 13* for a summary pf SPI features.

Table 13. SPI/I2S implementation

SPI features[1]	SPI1
Hardware CRC calculation	X
I2S mode	-
TI mode	X

1. X = supported.

3.19.5 Universal serial bus (USB)

The STM32L062x8 embed a full-speed USB device peripheral compliant with the USB specification version 2.0. The internal USB PHY supports USB FS signaling, embedded DP pull-up and also battery charging detection according to Battery Charging Specification Revision 1.2. The USB interface implements a full-speed (12 Mbit/s) function interface with added support for USB 2.0 Link Power Management. It has software-configurable endpoint setting with packet memory up to 1 KB and suspend/resume support. It requires a precise 48 MHz clock which can be generated by the internal 48 MHz oscillator in automatic trimming mode. The synchronization for this oscillator can be taken from the USB data stream itself (SOF signalization) which allows crystal-less operation.

3.20 Clock recovery system (CRS)

The STM32L062x8 embed a special block which allows automatic trimming of the internal 48 MHz oscillator to guarantee its optimal accuracy over the whole device operational range. This automatic trimming is based on the external synchronization signal, which could be either derived from USB SOF signalization, from LSE oscillator, from an external signal on CRS_SYNC pin or generated by user software. For faster lock-in during startup it is also possible to combine automatic trimming with manual trimming action.

3.21 Cyclic redundancy check (CRC) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at linktime and stored at a given memory location.

3.22 Serial wire debug port (SW-DP)

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

Table 15. STM32L062x8 pin definitions (continued)

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP32	UFQFPN32	WLCSP36						
-	32	B5	PB8	I/O	FTf	-	TSC_SYNC, I2C1_SCL	-
32	-	D6	VSS	S		-	-	-
1	1	A5	VDD	S		-	-	-

1.   PA4 offers a reduced touch sensing sensitivity. It is thus recommended to use it as sampling capacitor I/O.

6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 18: Voltage characteristics*, *Table 19: Current characteristics*, and *Table 20: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard. Extended mission profiles are available on demand.

Table 18. Voltage characteristics

Symbol	Definition	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA}, V_{DD})[1]	–0.3	4.0	V
V_{IN}[2]	Input voltage on FT and FTf pins	V_{SS} –0.3	V_{DD}+4.0	
	Input voltage on TC pins	V_{SS} –0.3	4.0	
	Input voltage on BOOT0	V_{SS}	V_{DD} +4.0	
	Input voltage on any other pin	V_{SS} –0.3	4.0	
$|\Delta V_{DD}|$	Variations between different V_{DDx} power pins	-	50	mV
$|V_{DDA}$-$V_{DDx}|$	Variations between any V_{DDx} and V_{DDA} power pins[3]	-	300	
$|\Delta V_{SS}|$	Variations between all different ground pins	-	50	
V_{REF+} –V_{DDA}	Allowed voltage difference for V_{REF+} > V_{DDA}	-	0.4	V
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.11*		

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

2. V_{IN} maximum must always be respected. Refer to *Table 19* for maximum allowed injected current values.

3. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and device operation.

6.3.2 Embedded reset and power control block characteristics

The parameters given in the following table are derived from the tests performed under the ambient temperature condition summarized in *Table 21*.

Table 22. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}[1]	V_{DD} rise time rate	BOR detector enabled	0	-	∞	µs/V
		BOR detector disabled	0	-	1000	
	V_{DD} fall time rate	BOR detector enabled	20	-	∞	
		BOR detector disabled	0	-	1000	
$T_{RSTTEMPO}$[1]	Reset temporization	V_{DD} rising, BOR enabled	-	2	3.3	ms
		V_{DD} rising, BOR disabled[2]	0.4	0.7	1.6	
$V_{POR/PDR}$	Power-on/power down reset threshold	Falling edge	1	1.5	1.65	V
		Rising edge	1.3	1.5	1.65	
V_{BOR0}	Brown-out reset threshold 0	Falling edge	1.67	1.7	1.74	
		Rising edge	1.69	1.76	1.8	
V_{BOR1}	Brown-out reset threshold 1	Falling edge	1.87	1.93	1.97	
		Rising edge	1.96	2.03	2.07	
V_{BOR2}	Brown-out reset threshold 2	Falling edge	2.22	2.30	2.35	
		Rising edge	2.31	2.41	2.44	
V_{BOR3}	Brown-out reset threshold 3	Falling edge	2.45	2.55	2.6	
		Rising edge	2.54	2.66	2.7	
V_{BOR4}	Brown-out reset threshold 4	Falling edge	2.68	2.8	2.85	
		Rising edge	2.78	2.9	2.95	
V_{PVD0}	Programmable voltage detector threshold 0	Falling edge	1.8	1.85	1.88	
		Rising edge	1.88	1.94	1.99	
V_{PVD1}	PVD threshold 1	Falling edge	1.98	2.04	2.09	
		Rising edge	2.08	2.14	2.18	
V_{PVD2}	PVD threshold 2	Falling edge	2.20	2.24	2.28	
		Rising edge	2.28	2.34	2.38	
V_{PVD3}	PVD threshold 3	Falling edge	2.39	2.44	2.48	
		Rising edge	2.47	2.54	2.58	
V_{PVD4}	PVD threshold 4	Falling edge	2.57	2.64	2.69	
		Rising edge	2.68	2.74	2.79	
V_{PVD5}	PVD threshold 5	Falling edge	2.77	2.83	2.88	
		Rising edge	2.87	2.94	2.99	

Table 33. Peripheral current consumption in Run or Sleep mode[1] (continued)

Peripheral		Typical consumption, V_{DD} = 3.0 V, T_A = 25 °C				Unit
		Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	Low-power sleep and run	
AHB	CRC	1.5	1	1	1	μA/MHz (f_{HCLK})
	FLASH	0[3]	0[3]	0[3]	0[3]	
	DMA1	10	8	6.5	8.5	
	RNG	5.5	1	0.5	0.5	
	TSC	3	2.5	2	3	
All enabled		283	225	222.5	212.5	μA/MHz (f_{HCLK})
PWR		2.5	2	2	1	μA/MHz (f_{HCLK})

1. Data based on differential I_{DD} measurement between all peripherals OFF an one peripheral with clock enabled, in the following conditions: f_{HCLK} = 32 MHz (range 1), f_{HCLK} = 16 MHz (range 2), f_{HCLK} = 4 MHz (range 3), f_{HCLK} = 64kHz (Low-power run/sleep), f_{APB1} = f_{HCLK}, f_{APB2} = f_{HCLK}, default prescaler value for each peripheral. The CPU is in Sleep mode in both cases. No I/O pins toggling. Not tested in production.

2. HSI oscillator is OFF for this measure.

3. Current consumption is negligible and close to 0 μA.

Table 34. Peripheral current consumption in Stop and Standby mode[1]

Symbol	Peripheral	Typical consumption, T_A = 25 °C		Unit
		V_{DD}=1.8 V	V_{DD}=3.0 V	
$I_{DD(PVD / BOR)}$	-	0.7	1.2	μA
I_{REFINT}	-	-	1.4	
-	LSE Low drive[2]	0,1	0,1	
-	LPTIM1, Input 100 Hz	0,01	0,01	
-	LPTIM1, Input 1 MHz	6	6	
-	LPUART1	0,2	0,2	
-	RTC	0,3	0,48	

1. LPTIM peripheral cannot operate in Standby mode.

2. LSE Low drive consumption is the difference between an external clock on OSC32_IN and a quartz between OSC32_IN and OSC32_OUT.-

6.3.6 External clock source characteristics

Low-speed external user clock generated from an external source
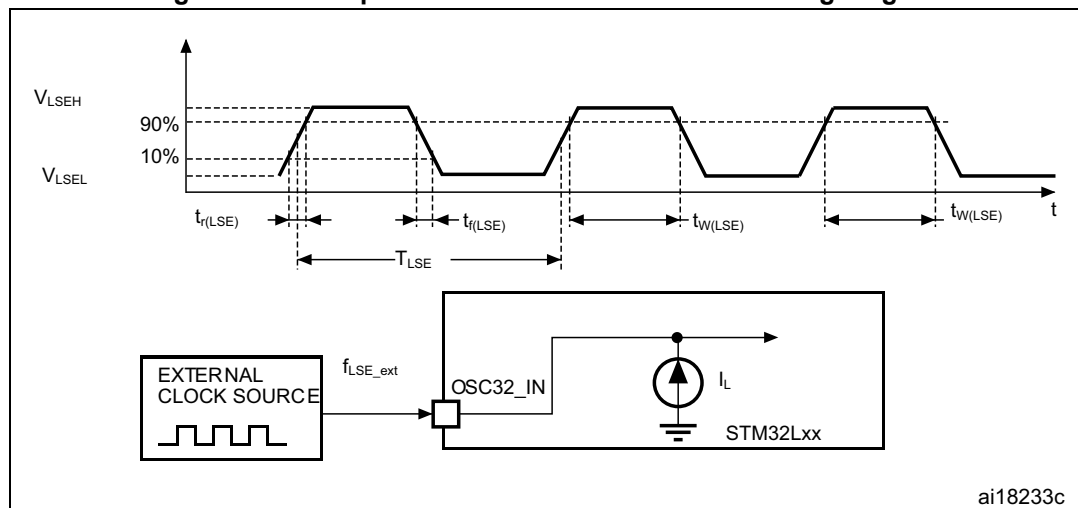
The characteristics given in the following table result from tests performed using a low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 21*.

Table 36. Low-speed external user clock characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency		1	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage	-	V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time		465	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time		-	-	10	
$C_{IN(LSE)}$	OSC32_IN input capacitance	-	-	0.6	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design, not tested in production

Figure 16. Low-speed external clock source AC timing diagram

6.3.7 Internal clock source characteristics

The parameters given in *Table 38* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 21*.

High-speed internal 16 MHz (HSI16) RC oscillator

Table 38. 16 MHz HSI16 oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI16}	Frequency	V_{DD} = 3.0 V	-	16	-	MHz
$TRIM^{(1)(2)}$	HSI16 user-trimmed resolution	Trimming code is not a multiple of 16	-	± 0.4	0.7	%
		Trimming code is a multiple of 16	-	-	± 1.5	%
$ACC_{HSI16}^{(2)}$	Accuracy of the factory-calibrated HSI16 oscillator	V_{DDA} = 3.0 V, T_A = 25 °C	-1[3]	-	1[3]	%
		V_{DDA} = 3.0 V, T_A = 0 to 55 °C	-1.5	-	1.5	%
		V_{DDA} = 3.0 V, T_A = -10 to 70 °C	-2	-	2	%
		V_{DDA} = 3.0 V, T_A = -10 to 85 °C	-2.5	-	2	%
		V_{DDA} = 3.0 V, T_A = -10 to 105 °C	-4	-	2	%
		V_{DDA} = 1.65 V to 3.6 V T_A = − 40 to 125 °C	-5.45	-	3.25	%
$t_{SU(HSI16)}^{(2)}$	HSI16 oscillator startup time	-	-	3.7	6	µs
$I_{DD(HSI16)}^{(2)}$	HSI16 oscillator power consumption	-	-	100	140	µA

1. The trimming step differs depending on the trimming code. It is usually negative on the codes which are multiples of 16 (0x00, 0x10, 0x20, 0x30...0xE0).

2. Guaranteed by characterization results.

3. Guaranteed by test in production.

Figure 18. HSI16 minimum and maximum value versus temperature
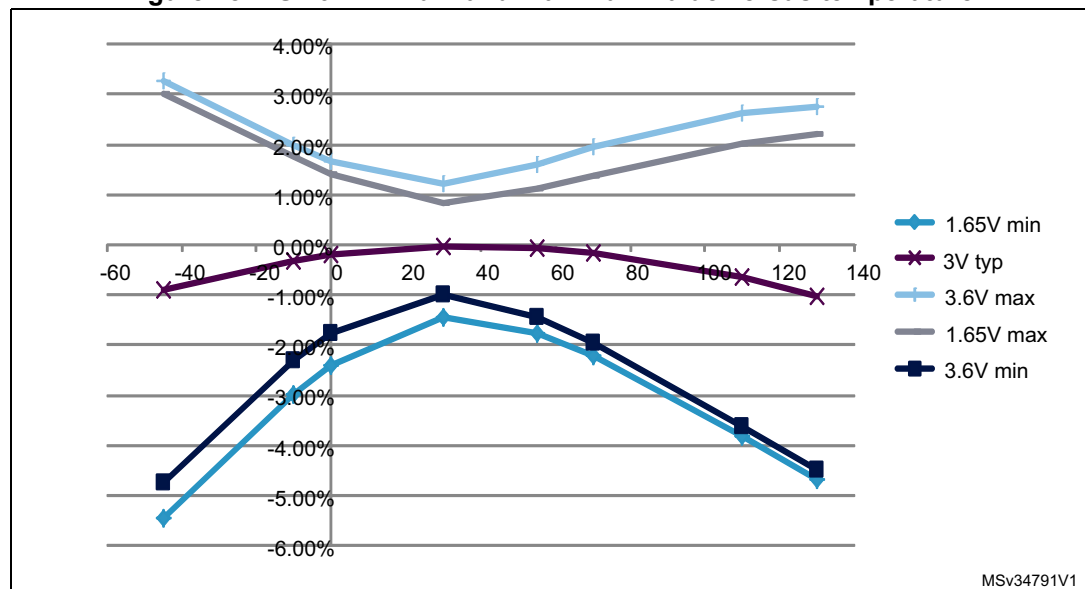
6.3.9 Memory characteristics

RAM memory

Table 43. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VRM	Data retention mode[1]	STOP mode (or RESET)	1.65	-	-	V

1. Minimum supply voltage without losing data stored in RAM (in Stop mode or under Reset) or in hardware registers (only in Stop mode).

Flash memory and data EEPROM

Table 44. Flash memory and data EEPROM characteristics

Symbol	Parameter	Conditions	Min	Typ	Max[1]	Unit
V_{DD}	Operating voltage Read / Write / Erase	-	1.65	-	3.6	V
t_{prog}	Programming time for word or half-page	Erasing	-	3.28	3.94	ms
		Programming	-	3.28	3.94	
I_{DD}	Average current during the whole programming / erase operation	T_A = 25 °C, V_{DD} = 3.6 V	-	500	700	µA
	Maximum current (peak) during the whole programming / erase operation		-	1.5	2.5	mA

1. Guaranteed by design.

Table 45. Flash memory and data EEPROM endurance and retention

Symbol	Parameter	Conditions	Value Min[1]	Unit
N_{CYC}[2]	Cycling (erase / write) Program memory	T_A = -40°C to 105 °C	10	kcycles
	Cycling (erase / write) EEPROM data memory		100	
	Cycling (erase / write) Program memory	T_A = -40°C to 125 °C	0.2	
	Cycling (erase / write) EEPROM data memory		2	

6.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset occurrence oscillator frequency deviation).

The test results are given in the *Table 50*.

Table 50. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0	-0	NA	mA
	Injected current on PA0, PA4, PA5, PA11, PA12, PC15, PH0 and PH1	-5	0	
	Injected current on any other FT, FTf pins	-5 [(1)]	NA	
	Injected current on any other pins	-5 [(1)]	+5	

1. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.
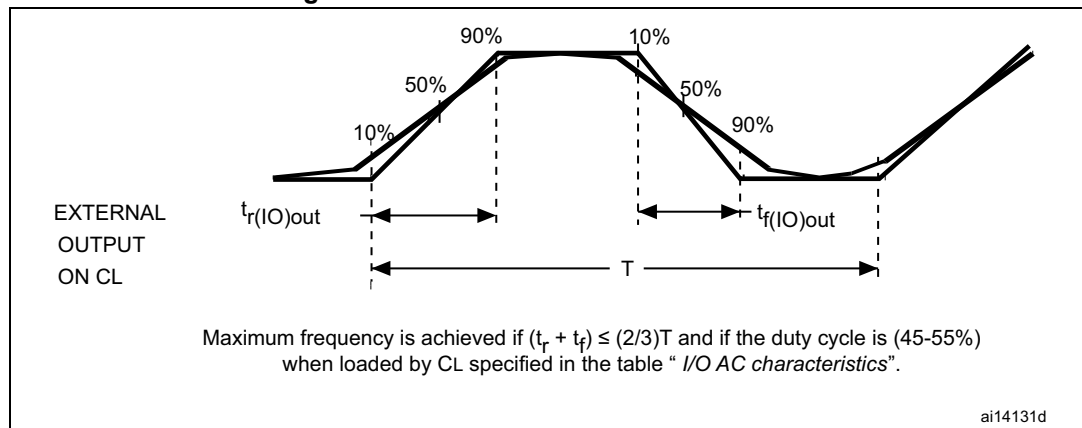
Output voltage levels

Unless otherwise specified, the parameters given in *Table 52* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 21*. All I/Os are CMOS and TTL compliant.

Table 52. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}[1]	Output low level voltage for an I/O pin	CMOS port[2], I_{IO} = +8 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	V
V_{OH}[3]	Output high level voltage for an I/O pin		V_{DD}-0.4	-	
V_{OL}[1]	Output low level voltage for an I/O pin	TTL port[2], I_{IO} =+ 8 mA 2.7 V ≤V_{DD} ≤ 3.6 V	-	0.4	
V_{OH}[3][4]	Output high level voltage for an I/O pin	TTL port[2], I_{IO} = -6 mA 2.7 V ≤V_{DD} ≤ 3.6 V	2.4	-	
V_{OL}[1][4]	Output low level voltage for an I/O pin	I_{IO} = +15 mA 2.7 V ≤V_{DD} ≤ 3.6 V	-	1.3	
V_{OH}[3][4]	Output high level voltage for an I/O pin	I_{IO} = -15 mA 2.7 V ≤V_{DD} ≤ 3.6 V	V_{DD}-1.3	-	
V_{OL}[1][4]	Output low level voltage for an I/O pin	I_{IO} = +4 mA 1.65 V ≤V_{DD} < 3.6 V	-	0.45	
V_{OH}[3][4]	Output high level voltage for an I/O pin	I_{IO} = -4 mA 1.65 V ≤V_{DD} ≤ 3.6 V	V_{DD}-0.45	-	
V_{OLFM+}[1][4]	Output low level voltage for an FTf I/O pin in Fm+ mode	I_{IO} = 20 mA 2.7 V ≤V_{DD} ≤ 3.6 V	-	0.4	
		I_{IO} = 10 mA 1.65 V ≤V_{DD} ≤ 3.6 V	-	0.4	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 19*. The sum of the currents sunk by all the I/Os (I/O ports and control pins) must always be respected and must not exceed $\Sigma I_{IO(PIN)}$.

2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.

3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 19*. The sum of the currents sourced by all the I/Os (I/O ports and control pins) must always be respected and must not exceed $\Sigma I_{IO(PIN)}$.

4. Guaranteed by characterization results.

Figure 21. I/O AC characteristics definition

Maximum frequency is achieved if $(t_r + t_f) \leq (2/3)T$ and if the duty cycle is (45-55%) when loaded by CL specified in the table " *I/O AC characteristics*".

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6.3.14 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} , except when it is internally driven low (see *Table 54*).

Unless otherwise specified, the parameters given in *Table 54* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 21*.

Table 54. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$[1]	NRST input low level voltage	-	V_{SS}	-	0.8	
$V_{IH(NRST)}$[1]	NRST input high level voltage	-	1.4	-	V_{DD}	
$V_{OL(NRST)}$[1]	NRST output low level voltage	I_{OL} = 2 mA 2.7 V < V_{DD} < 3.6 V	-	-	0.4	V
		I_{OL} = 1.5 mA 1.65 V < V_{DD} < 2.7 V	-	-		
$V_{hys(NRST)}$[1]	NRST Schmitt trigger voltage hysteresis	-	-	10%V_{DD}[2]	-	mV
R_{PU}	Weak pull-up equivalent resistor[3]	V_{IN} = V_{SS}	30	45	60	kΩ
$V_{F(NRST)}$[1]	NRST input filtered pulse	-	-	-	50	ns
$V_{NF(NRST)}$[1]	NRST input not filtered pulse	-	350	-	-	ns

1. Guaranteed by design.

2. 200 mV minimum value

3. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is around 10%.

Table 58. DAC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes till DAC_OUT reaches final value ±1LSB	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ	-	7	12	µs
Update rate	Max frequency for a correct DAC_OUT change (95% of final value) with 1 LSB variation in the input code	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ	-	-	1	Msps
t_{WAKEUP}	Wakeup time from off state (setting the ENx bit in the DAC Control register)[9]	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ	-	9	15	µs
PSRR+	V_{DDA} supply rejection ratio (static DC measurement)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ	-	-60	-35	dB

1. Guaranteed by characterization results.
2. Guaranteed by design, not tested in production.
3. Connected between DAC_OUT and V_{SSA}.
4. Difference between two consecutive codes - 1 LSB.
5. Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095.
6. Difference between the value measured at Code (0x800) and the ideal value = $V_{REF+}/2$.
7. Difference between the value measured at Code (0x001) and the ideal value.
8. Difference between ideal slope of the transfer function and measured slope computed from code 0x000 and 0xFFF when buffer is OFF, and from code giving 0.2 V and (V_{DDA} – 0.2) V when buffer is ON.
9. In buffered mode, the output can overshoot above the final value for low input code (starting from min value).

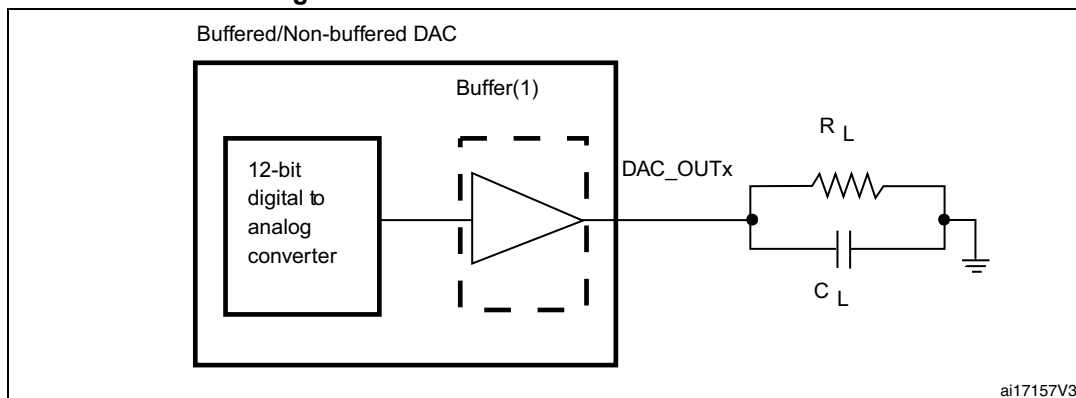**Figure 27. 12-bit buffered/non-buffered DAC**

Table 62. Comparator 2 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max[1]	Unit
V_{DDA}	Analog supply voltage	-	1.65	-	3.6	V
V_{IN}	Comparator 2 input voltage range	-	0	-	V_{DDA}	V
t_{START}	Comparator startup time	Fast mode	-	15	20	µs
		Slow mode	-	20	25	
$t_{d\ slow}$	Propagation delay[2] in slow mode	$1.65\ V \leq V_{DDA} \leq 2.7\ V$	-	1.8	3.5	
		$2.7\ V \leq V_{DDA} \leq 3.6\ V$	-	2.5	6	
$t_{d\ fast}$	Propagation delay[2] in fast mode	$1.65\ V \leq V_{DDA} \leq 2.7\ V$	-	0.8	2	
		$2.7\ V \leq V_{DDA} \leq 3.6\ V$	-	1.2	4	
V_{offset}	Comparator offset error		-	±4	±20	mV
dThreshold/ dt	Threshold voltage temperature coefficient	$V_{DDA} = 3.3V$, $T_A = 0$ to $50\ °C$, V- = V_{REFINT}, 3/4 V_{REFINT}, 1/2 V_{REFINT}, 1/4 V_{REFINT}.	-	15	30	ppm /°C
I_{COMP2}	Current consumption[3]	Fast mode	-	3.5	5	µA
		Slow mode	-	0.5	2	

1. Guaranteed by characterization results.

2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.

3. Comparator consumption only. Internal reference voltage (required for comparator operation) is not included.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status *are available at* www.st.com. ECOPACK® is an ST trademark.

7.1 Standard WLCSP36 package information

Figure 32. Standard WLCSP36 - 2.61 x 2.88 mm, 0.4 mm pitch wafer level chip scale package outline
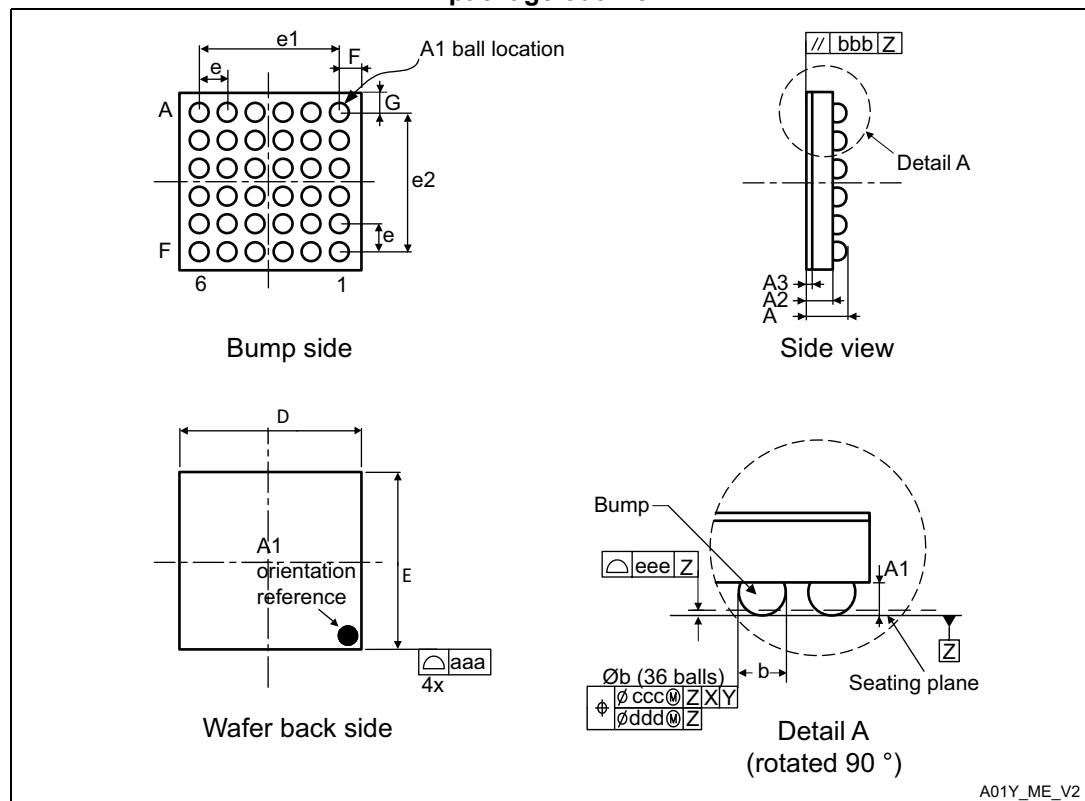
1. Drawing is not to scale.
2. b dimensions is measured at the maximum bump diameter parallel to primary datum Z

Table 72. Standard WLCSP36 - 2.61 x 2.88 mm, 0.4 mm pitch wafer level chip scale mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	0.59	-	-	0.023
A1	-	0.18	-	-	0.007	-
A2	-	0.38	-	-	0.015	-
A3	-	0.025[2]	-	-	0.001	-
b	0.22	0.25	0.28	0.009	0.010	0.011
D	2.59	2.61	2.63	0.102	0.103	0.104
E	2.86	2.88	2.90	0.112	0.113	0.114
e	-	0.40	-	-	0.016	-
e1	-	2.00	-	-	0.079	-
e2	-	2.00	-	-	0.079	-
F	-	0.305[3]	-	-	0.012	-
G	-	0.440[3]	-	-	0.017	-
aaa	-	-	0.100	-	-	0.004
bbb	-	-	0.100	-	-	0.004
ccc	-	-	0.100	-	-	0.004
ddd	-	-	0.050	-	-	0.002
eee	-	-	0.050	-	-	0.002

1. Values in inches are converted from mm and rounded to the 3rd decimal place.

2. Nominal dimension rounded to the 3rd decimal place results from process capability.

3. Calculated dimensions are rounded to the 3rd decimal place.

Figure 33. Standard WLCSP36 - 2.61 x 2.88 mm, 0.4 mm pitch wafer level chip scale recommended footprint