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Details

Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	I ² C, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3.8V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st72f321bj6t6tr

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3 REGISTER & MEMORY MAP

As shown in Figure 5, the MCU is capable of addressing 64K bytes of memories and I/O registers.

The available memory locations consist of 128 bytes of register locations, up to 2Kbytes of RAM and up to 60Kbytes of user program memory. The RAM space includes up to 256 bytes for the stack from 0100h to 01FFh.

The highest address bytes contain the user reset and interrupt vectors.

IMPORTANT: Memory locations marked as "Reserved" must never be accessed. Accessing a reseved area can have unpredictable effects on the device.

Related Documentation

AN 985: Executing Code in ST7 RAM

Figure 5. Memory Map





ST72321BRx, ST72321BARx ST72321BJx, ST72321BKx

Address	Block	Register Label	Register Name	Reset Status	Remarks
002Ah	WATCHDOG	WDGCR	Watchdog Control Register	7Fh	R/W
002Bh		SICSR	System Integrity Control/Status Register	000x 000x b	R/W
002Ch 002Dh	MCC	MCCSR MCCBCR	Main Clock Control / Status Register Main Clock Controller: Beep Control Register	00h 00h	R/W R/W
002Eh to 0030h			Reserved Area (3 Bytes)		
0031h 0032h 0033h 0034h 0035h 0036h 0037h 0038h 0039h 003Ah 003Bh 003Ch 003Ch 003Eh 003Fh	TIMER A	TACR2 TACR1 TACSR TAIC1HR TAIC1LR TAOC1HR TAOC1LR TAOC1LR TACHR TACLR TACLR TAACLR TAACLR TAIC2LR TAIC2LR TAOC2LR	Timer A Control Register 2 Timer A Control Register 1 Timer A Control/Status Register Timer A Input Capture 1 High Register Timer A Input Capture 1 Low Register Timer A Output Compare 1 High Register Timer A Output Compare 1 Low Register Timer A Counter High Register Timer A Counter High Register Timer A Alternate Counter High Register Timer A Alternate Counter Low Register Timer A Input Capture 2 High Register Timer A Input Capture 2 Low Register Timer A Output Compare 2 High Register Timer A Output Compare 2 Low Register	00h 00h xxxx x0xx b xxh 80h 00h FFh FCh FCh FCh xxh xxh 80h 00h	R/W R/W Read Only Read Only R/W R/W Read Only Read Only
0040h		l	Reserved Area (1 Byte)		
0041h 0042h 0043h 0044h 0045h 0045h 0046h 0047h 0048h 0049h 004Ah 004Bh 004Ch 004Ch 004Eh 004Fh	TIMER B	TBCR2 TBCR1 TBCSR TBIC1HR TBIC1LR TBOC1HR TBOC1LR TBCHR TBCHR TBCLR TBACHR TBACLR TBIC2HR TBIC2LR TBIC2LR TBOC2LR	CR2Timer B Control Register 2CR1Timer B Control Register 1CSRTimer B Control/Status RegisterIC1HRTimer B Input Capture 1 High RegisterIC1LRTimer B Input Capture 1 Low RegisterOC1HRTimer B Output Compare 1 High RegisterOC1LRTimer B Output Compare 1 Low RegisterOC1LRTimer B Counter High RegisterCHRTimer B Counter Low RegisterCLRTimer B Alternate Counter High RegisterACHRTimer B Alternate Counter Low RegisterIC2HRTimer B Input Capture 2 High RegisterIC2LRTimer B Output Compare 2 High RegisterOC2LRTimer B Output Compare 2 Low Register		R/W R/W Read Only Read Only R/W R/W Read Only Read Only
0050h 0051h 0052h 0053h 0054h 0055h 0056h 0057h	TBOC2LR Timer B Output Compare 2 Low Register SCISR SCI Status Register SCIDR SCI Data Register SCIBRR SCI Baud Rate Register SCICR1 SCI Control Register 1 SCICR2 SCI Control Register 2 SCIERPR SCI Extended Receive Prescaler Register Reserved area SCI Extended Transmit Prescaler Register		C0h xxh 00h x000 0000b 00h 00h 00h	Read Only R/W R/W R/W R/W R/W	

INTERRUPTS (Cont'd)

Instruction	New Description	Function/Example	11	н	10	Ν	Z	С
HALT	Entering Halt mode		1		0			
IRET	Interrupt routine return	Pop CC, A, X, PC	11	Н	10	Ν	Z	С
JRM	Jump if I1:0=11 (level 3)	l1:0=11 ?						
JRNM	Jump if I1:0<>11	11:0<>11 ?						
POP CC	Pop CC from the Stack	Mem => CC	1	Н	10	Ν	Z	С
RIM	Enable interrupt (level 0 set)	Load 10 in I1:0 of CC	1		0			
SIM	Disable interrupt (level 3 set)	Load 11 in I1:0 of CC	1		1			
TRAP	Software trap	Software NMI	1		1			
WFI	Wait for interrupt		1		0			

Table 7. Dedicated Interrupt Instruction Set

Note: During the execution of an interrupt routine, the HALT, POPCC, RIM, SIM and WFI instructions change the current software priority up to the next IRET instruction or one of the previously mentioned instructions.



POWER SAVING MODES (Cont'd)

8.3 WAIT MODE

WAIT mode places the MCU in a low power consumption mode by stopping the CPU.

This power saving mode is selected by calling the 'WFI' instruction.

All peripherals remain active. During WAIT mode, the I[1:0] bits of the CC register are forced to '10', to enable all interrupts. All other registers and memory remain unchanged. The MCU remains in WAIT mode until an interrupt or RESET occurs, whereupon the Program Counter branches to the starting address of the interrupt or Reset service routine.

The MCU will remain in WAIT mode until a Reset or an Interrupt occurs, causing it to wake up.

Refer to Figure 26.



Note:

1. Before servicing an interrupt, the CC register is pushed on the stack. The I[1:0] bits of the CC register are set to the current software priority level of the interrupt routine and recovered when the CC register is popped.





I/O PORTS (Cont'd)

Table 13. I/O Port Register Map and Reset Values

Address (Hex.)	Register Label	7	6	5	4	3	2	1	0
Rese of all I/O p	t Value ort registers	0	0	0	0	0	0	0	0
0000h	PADR								
0001h	PADDR	MSB							LSB
0002h	PAOR								
0003h	PBDR								
0004h	PBDDR	MSB							LSB
0005h	PBOR								
0006h	PCDR								
0007h	PCDDR	MSB							LSB
0008h	PCOR								
0009h	PDDR								
000Ah	PDDDR	MSB							LSB
000Bh	PDOR								
000Ch	PEDR								
000Dh	PEDDR	MSB							LSB
000Eh	PEOR								
000Fh	PFDR								
0010h	PFDDR	MSB							LSB
0011h	PFOR								

Related Documentation

AN 970: SPI Communication between ST7 and EEPROM

AN1045: S/W implementation of I2C bus master AN1048: Software LCD driver

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MAIN CLOCK CONTROLLER WITH REAL TIME CLOCK (Cont'd)

10.2.5 Low Power Modes

Mode	Description
WAIT	No effect on MCC/RTC peripheral. MCC/RTC interrupt cause the device to exit from WAIT mode.
ACTIVE- HALT	No effect on MCC/RTC counter (OIE bit is set), the registers are frozen. MCC/RTC interrupt cause the device to exit from ACTIVE-HALT mode.
HALT	MCC/RTC counter and registers are frozen. MCC/RTC operation resumes when the MCU is woken up by an interrupt with "exit from HALT" capability.

10.2.6 Interrupts

The MCC/RTC interrupt event generates an interrupt if the OIE bit of the MCCSR register is set and the interrupt mask in the CC register is not active (RIM instruction).

Interrupt Event	Event Flag	Enable Control Bit	Exit from Wait	Exit from Halt
Time base overflow event	OIF	OIE	Yes	No ¹⁾

Note:

The MCC/RTC interrupt wakes up the MCU from ACTIVE-HALT mode, not from HALT mode.

10.2.7 Register Description MCC CONTROL/STATUS REGISTER (MCCSR)

Read/Write

Reset Value: 0000 0000 (00h)

7							0
мсо	CP1	CP0	SMS	TB1	TB0	OIE	OIF

Bit 7 = **MCO** *Main clock out selection*

This bit enables the MCO alternate function on the PF0 I/O port. It is set and cleared by software.

0: MCO alternate function disabled (I/O pin free for general-purpose I/O)

1: MCO alternate function enabled (f_{CPU} on I/O port)

Note: To reduce power consumption, the MCO function is not active in ACTIVE-HALT mode.

Bit 6:5 = CP[1:0] CPU clock prescaler

These bits select the CPU clock prescaler which is applied in the different slow modes. Their action is conditioned by the setting of the SMS bit. These two bits are set and cleared by software

f _{CPU} in SLOW mode	CP1	CP0
f _{OSC2} / 2	0	0
f _{OSC2} / 4	0	1
f _{OSC2} / 8	1	0
f _{OSC2} / 16	1	1

Bit 4 = **SMS** *Slow mode select*

This bit is set and cleared by software.

0: Normal mode. f_{CPU} = f_{OSC2}

1: Slow mode. f_{CPU} is given by CP1, CP0 See Section 8.2 SLOW MODE and Section 10.2 MAIN CLOCK CONTROLLER WITH REAL TIME CLOCK AND BEEPER (MCC/RTC) for more details.

Bit 3:2 = TB[1:0] Time base control

These bits select the programmable divider time base. They are set and cleared by software.

Counter	Time	Base	TB1	TRO
Prescaler	f _{OSC2} =4MHz	f _{OSC2} =8MHz	101	100
16000	4ms	2ms	0	0
32000	8ms	4ms	0	1
80000	20ms	10ms	1	0
200000	50ms	25ms	1	1

A modification of the time base is taken into account at the end of the current period (previously set) to avoid an unwanted time shift. This allows to use this time base as a real time clock.

Bit 1 = **OIE** Oscillator interrupt enable

This bit set and cleared by software.

0: Oscillator interrupt disabled

1: Oscillator interrupt enabled

This interrupt can be used to exit from ACTIVE-HALT mode.

When this bit is set, calling the ST7 software HALT instruction enters the ACTIVE-HALT power saving mode.



ON-CHIP PERIPHERALS (Cont'd)

INPUT CAPTURE CONTROL / STATUS REGISTER (ARTICCSR)

Read/Write

Reset Value: 0000 0000 (00h)

7							0
0	0	CS2	CS1	CIE2	CIE1	CF2	CF1

Bit 7:6 = Reserved, always read as 0.

Bit 5:4 = **CS[2:1]** Capture Sensitivity

These bits are set and cleared by software. They determine the trigger event polarity on the corresponding input capture channel.

0: Falling edge triggers capture on channel x.

1: Rising edge triggers capture on channel x.

Bit 3:2 = **CIE[2:1]** *Capture Interrupt Enable* These bits are set and cleared by software. They enable or disable the Input capture channel interrupts independently.

0: Input capture channel x interrupt disabled.

1: Input capture channel x interrupt enabled.

Bit 1:0 = CF[2:1] Capture Flag

These bits are set by hardware and cleared by software reading the corresponding ARTICRx register. Each CFx bit indicates that an input capture x has occurred.

0: No input capture on channel x.

1: An input capture has occurred on channel x.

INPUT CAPTURE REGISTERS (ARTICRx)

Read only

Reset Value: 0000 0000 (00h)

7							0
IC7	IC6	IC5	IC4	IC3	IC2	IC1	IC0

Bit 7:0 = IC[7:0] Input Capture Data

These read only bits are set and cleared by hardware. An ARTICRx register contains the 8-bit auto-reload counter value transferred by the input capture channel x event.

16-BIT TIMER (Cont'd)

Figure 43. Timer Block Diagram



16-BIT TIMER (Cont'd)

10.4.3.6 Pulse Width Modulation Mode

Pulse Width Modulation (PWM) mode enables the generation of a signal with a frequency and pulse length determined by the value of the OC1R and OC2R registers.

Pulse Width Modulation mode uses the complete Output Compare 1 function plus the OC2R register, and so this functionality can not be used when PWM mode is activated.

In PWM mode, double buffering is implemented on the output compare registers. Any new values written in the OC1R and OC2R registers are taken into account only at the end of the PWM period (OC2) to avoid spikes on the PWM output pin (OCMP1).

Procedure

To use Pulse Width Modulation mode:

- 1. Load the OC2R register with the value corresponding to the period of the signal using the formula in the opposite column.
- 2. Load the OC1R register with the value corresponding to the period of the pulse if (OLVL1 = 0 and OLVL2 = 1) using the formula in the opposite column.
- Select the following in the CR1 register:
 - Using the OLVL1 bit, select the level to be applied to the OCMP1 pin after a successful comparison with the OC1R register.
 - Using the OLVL2 bit, select the level to be applied to the OCMP1 pin after a successful comparison with the OC2R register.
- 4. Select the following in the CR2 register:
 - Set OC1E bit: the OCMP1 pin is then dedicated to the output compare 1 function.
 - Set the PWM bit.
 - Select the timer clock (CC[1:0]) (see Table 1).



If OLVL1 = 1 and OLVL2 = 0 the length of the positive pulse is the difference between the OC2R and OC1R registers.

If OLVL1 = OLVL2 a continuous signal will be seen on the OCMP1 pin.

The OC*i*R register value required for a specific timing application can be calculated using the following formula:

Where:

t = Signal or pulse period (in seconds)

f_{CPU} = CPU clock frequency (in hertz)

PRESC = Timer prescaler factor (2, 4 or 8 depending on CC[1:0] bits, see Table 1)

If the timer clock is an external clock the formula is:

Where:

t

Signal or pulse period (in seconds)

f_{EXT} = External timer clock frequency (in hertz)

The Output Compare 2 event causes the counter to be initialized to FFFCh (See Figure 11)

Notes:

- 1. After a write instruction to the OC*i*HR register, the output compare function is inhibited until the OC*i*LR register is also written.
- 2. The OCF1 and OCF2 bits cannot be set by hardware in PWM mode therefore the Output Compare interrupt is inhibited.
- 3. The ICF1 bit is set by hardware when the counter reaches the OC2R value and can produce a timer interrupt if the ICIE bit is set and the I bit is cleared.
- 4. In PWM mode the ICAP1 pin can not be used to perform input capture because it is disconnected to the timer. The ICAP2 pin can be used to perform input capture (ICF2 can be set and IC2R can be loaded) but the user must take care that the counter is reset each period and ICF1 can also generates interrupt if ICIE is set.
- 5. When the Pulse Width Modulation (PWM) and One Pulse mode (OPM) bits are both set, the PWM mode is the only active one.

16-BIT TIMER (Cont'd)

10.4.7 Register Description

Each Timer is associated with three control and status registers, and with six pairs of data registers (16-bit values) relating to the two input captures, the two output compares, the counter and the alternate counter.

CONTROL REGISTER 1 (CR1)

Read/Write

Reset Value: 0000 0000 (00h)

7							0
ICIE	OCIE	TOIE	FOLV2	FOLV1	OLVL2	IEDG1	OLVL1

Bit 7 = **ICIE** *Input Capture Interrupt Enable.* 0: Interrupt is inhibited.

1: A timer interrupt is generated whenever the ICF1 or ICF2 bit of the SR register is set.

Bit 6 = **OCIE** *Output Compare Interrupt Enable.* 0: Interrupt is inhibited.

1: A timer interrupt is generated whenever the OCF1 or OCF2 bit of the SR register is set.

Bit 5 = **TOIE** *Timer Overflow Interrupt Enable.* 0: Interrupt is inhibited.

1: A timer interrupt is enabled whenever the TOF bit of the SR register is set.

Bit 4 = FOLV2 Forced Output Compare 2.

- This bit is set and cleared by software.
- 0: No effect on the OCMP2 pin.
- 1: Forces the OLVL2 bit to be copied to the OCMP2 pin, if the OC2E bit is set and even if there is no successful comparison.

Bit 3 = FOLV1 Forced Output Compare 1.

- This bit is set and cleared by software.
- 0: No effect on the OCMP1 pin.
- 1: Forces OLVL1 to be copied to the OCMP1 pin, if the OC1E bit is set and even if there is no successful comparison.

Bit 2 = OLVL2 Output Level 2.

This bit is copied to the OCMP2 pin whenever a successful comparison occurs with the OC2R register and OCxE is set in the CR2 register. This value is copied to the OCMP1 pin in One Pulse mode and Pulse Width Modulation mode.

Bit 1 = IEDG1 Input Edge 1.

This bit determines which type of level transition on the ICAP1 pin will trigger the capture.0: A falling edge triggers the capture.1: A rising edge triggers the capture.

Bit 0 = OLVL1 Output Level 1.

The OLVL1 bit is copied to the OCMP1 pin whenever a successful comparison occurs with the OC1R register and the OC1E bit is set in the CR2 register.



SERIAL PERIPHERAL INTERFACE (Cont'd)

- SS: Slave select:

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This input signal acts as a 'chip select' to let the SPI master communicate with slaves individually and to avoid contention on the data lines. Slave SS inputs can be driven by standard I/O ports on the master MCU.

10.5.3.1 Functional Description

A basic example of interconnections between a single master and a single slave is illustrated in Figure 55.

The MOSI pins are connected together and the MISO pins are connected together. In this way data is transferred serially between master and slave (most significant bit first).

The communication is always initiated by the master. When the master device transmits data to a slave device via MOSI pin, the slave device responds by sending data to the master device via the MISO pin. This implies full duplex communication with both data out and data in synchronized with the same clock signal (which is provided by the master device via the SCK pin).

To use a single data line, the MISO and MOSI pins must be connected at each node (in this case only simplex communication is possible).

Four possible data/clock timing relationships may be chosen (see Figure 58) but master and slave must be programmed with the same timing mode.



Figure 55. Single Master/ Single Slave Application

SERIAL PERIPHERAL INTERFACE (Cont'd)

10.5.6 Low Power Modes

Mode	Description
WAIT	No effect on SPI. SPI interrupt events cause the device to exit from WAIT mode.
HALT	SPI registers are frozen. In HALT mode, the SPI is inactive. SPI oper- ation resumes when the MCU is woken up by an interrupt with "exit from HALT mode" ca- pability. The data received is subsequently read from the SPIDR register when the soft- ware is running (interrupt vector fetching). If several data are received before the wake- up event, then an overrun error is generated. This error can be detected after the fetch of the interrupt routine that woke up the device.

10.5.6.1 Using the SPI to wakeup the MCU from Halt mode

In slave configuration, the SPI is able to wakeup the ST7 device from HALT mode through a SPIF interrupt. The data received is subsequently read from the SPIDR register when the software is running (interrupt vector fetch). If multiple data transfers have been performed before software clears the SPIF bit, then the OVR bit is set by hardware. **Note:** When waking up from Halt mode, if the SPI remains in Slave mode, it is recommended to perform an extra communications cycle to bring the SPI from Halt mode state to normal state. If the SPI exits from Slave mode, it returns to normal state immediately.

Caution: The SPI can wake up the ST7 from Halt mode only if the Slave Select signal (external SS pin or the SSI bit in the SPICSR register) is low when the ST7 enters Halt mode. So if Slave selection is configured as external (see Section 10.5.3.2), make sure the master drives a low level on the SS pin when the slave enters Halt mode.

10.5.7 Interrupts

Interrupt Event	Event Flag	Enable Control Bit	Exit from Wait	Exit from Halt
SPI End of Transfer Event	SPIF		Yes	Yes
Master Mode Fault Event	MODF	SPIE	Yes	No
Overrun Error	OVR		Yes	No

Note: The SPI interrupt events are connected to the same interrupt vector (see Interrupts chapter). They generate an interrupt if the corresponding Enable Control Bit is set and the interrupt mask in

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SERIAL COMMUNICATIONS INTERFACE (Cont'd)

10.6.4.2 Transmitter

The transmitter can send data words of either 8 or 9 bits depending on the M bit status. When the M bit is set, word length is 9 bits and the 9th bit (the MSB) has to be stored in the T8 bit in the SCICR1 register.

Character Transmission

During an SCI transmission, data shifts out least significant bit first on the TDO pin. In this mode, the SCIDR register consists of a buffer (TDR) between the internal bus and the transmit shift register (see Figure 1.).

Procedure

- Select the M bit to define the word length.
- Select the desired baud rate using the SCIBRR and the SCIETPR registers.
- Set the TE bit to assign the TDO pin to the alternate function and to send a idle frame as first transmission.
- Access the SCISR register and write the data to send in the SCIDR register (this sequence clears the TDRE bit). Repeat this sequence for each data to be transmitted.

Clearing the TDRE bit is always performed by the following software sequence:

- 1. An access to the SCISR register
- 2. A write to the SCIDR register

The TDRE bit is set by hardware and it indicates:

- The TDR register is empty.
- The data transfer is beginning.
- The next data can be written in the SCIDR register without overwriting the previous data.

This flag generates an interrupt if the TIE bit is set and the I bit is cleared in the CCR register.

When a transmission is taking place, a write instruction to the SCIDR register stores the data in the TDR register and which is copied in the shift register at the end of the current transmission.

When no transmission is taking place, a write instruction to the SCIDR register places the data directly in the shift register, the data transmission starts, and the TDRE bit is immediately set. When a frame transmission is complete (after the stop bit) the TC bit is set and an interrupt is generated if the TCIE is set and the I bit is cleared in the CCR register.

Clearing the TC bit is performed by the following software sequence:

1. An access to the SCISR register

2. A write to the SCIDR register

Note: The TDRE and TC bits are cleared by the same software sequence.

Break Characters

Setting the SBK bit loads the shift register with a break character. The break frame length depends on the M bit (see Figure 2.).

As long as the SBK bit is set, the SCI send break frames to the TDO pin. After clearing this bit by software the SCI insert a logic 1 bit at the end of the last break frame to guarantee the recognition of the start bit of the next frame.

Idle Characters

Setting the TE bit drives the SCI to send an idle frame before the first data frame.

Clearing and then setting the TE bit during a transmission sends an idle frame after the current word.

Note: Resetting and setting the TE bit causes the data in the TDR register to be lost. Therefore the best time to toggle the TE bit is when the TDRE bit is set, that is, before writing the next byte in the SCIDR.



SERIAL COMMUNICATIONS INTERFACE (Cont'd)

10.6.7 Register Description

STATUS REGISTER (SCISR)

Read Only

Reset Value: 1100 0000 (C0h)

7							0
TDRE	тс	RDRF	IDLE	OR	NF	FE	PE

Bit 7 = **TDRE** *Transmit data register empty.*

This bit is set by hardware when the content of the TDR register has been transferred into the shift register. An interrupt is generated if the TIE bit = 1 in the SCICR2 register. It is cleared by a software sequence (an access to the SCISR register followed by a write to the SCIDR register).

0: Data is not transferred to the shift register 1: Data is transferred to the shift register

Note: Data is not transferred to the shift register unless the TDRE bit is cleared.

Bit 6 = **TC** *Transmission complete.*

This bit is set by hardware when transmission of a frame containing Data is complete. An interrupt is generated if TCIE = 1 in the SCICR2 register. It is cleared by a software sequence (an access to the SCISR register followed by a write to the SCIDR register).

0: Transmission is not complete

1: Transmission is complete

Note: TC is not set after the transmission of a Preamble or a Break.

Bit 5 = **RDRF** Received data ready flag.

This bit is set by hardware when the content of the RDR register has been transferred to the SCIDR register. An interrupt is generated if RIE = 1 in the SCICR2 register. It is cleared by a software sequence (an access to the SCISR register followed by a read to the SCIDR register).

0: Data is not received

1: Received data is ready to be read

Bit 4 = **IDLE** *Idle line detect.*

This bit is set by hardware when a Idle Line is detected. An interrupt is generated if the ILIE = 1 in the SCICR2 register. It is cleared by a software sequence (an access to the SCISR register followed by a read to the SCIDR register). 0: No Idle Line is detected

1: Idle Line is detected

1. Idle Lille is delected

Note: The IDLE bit is not set again until the RDRF bit has been set itself (that is, a new idle line occurs).

Bit 3 = **OR** Overrun error.

This bit is set by hardware when the word currently being received in the shift register is ready to be transferred into the RDR register while RDRF = 1. An interrupt is generated if RIE = 1 in the SCICR2 register. It is cleared by a software sequence (an access to the SCISR register followed by a read to the SCIDR register).

0: No Overrun error

1: Overrun error is detected

Note: When this bit is set RDR register content is not lost but the shift register is overwritten.

Bit 2 = NF Noise flag.

This bit is set by hardware when noise is detected on a received frame. It is cleared by a software sequence (an access to the SCISR register followed by a read to the SCIDR register). 0: No noise is detected

1: Noise is detected

Note: This bit does not generate interrupt as it ap-

pears at the same time as the RDRF bit which itself generates an interrupt.

Bit 1 = **FE** Framing error.

This bit is set by hardware when a de-synchronization, excessive noise or a break character is detected. It is cleared by a software sequence (an access to the SCISR register followed by a read to the SCIDR register).

0: No Framing error is detected

1: Framing error or break character is detected

Note: This bit does not generate interrupt as it appears at the same time as the RDRF bit which itself generates an interrupt. If the word currently being transferred causes both frame error and overrun error, it will be transferred and only the OR bit will be set.

Bit 0 = **PE** Parity error.

This bit is set by hardware when a parity error occurs in receiver mode. It is cleared by a software sequence (a read to the status register followed by an access to the SCIDR data register). An interrupt is generated if PIE = 1 in the SCICR1 register. 0: No parity error

1: Parity error

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I²C BUS INTERFACE (Cont'd)

Figure 67. Transfer Sequencing



EV1: EVF=1, ADSL=1, cleared by reading SR1 register.

EV2: EVF=1, BTF=1, cleared by reading SR1 register followed by reading DR register.

EV3: EVF=1, BTF=1, cleared by reading SR1 register followed by writing DR register.

EV3-1: EVF=1, AF=1, BTF=1; AF is cleared by reading SR1 register. BTF is cleared by releasing the

lines (STOP=1, STOP=0) or by writing DR register (DR=FFh). Note: If lines are released by

STOP=1, STOP=0, the subsequent EV4 is not seen.

EV4: EVF=1, STOPF=1, cleared by reading SR2 register.

EV5: EVF=1, SB=1, cleared by reading SR1 register followed by writing DR register.

EV6: EVF=1, cleared by reading SR1 register followed by writing CR register (for example PE=1).

EV7: EVF=1, BTF=1, cleared by reading SR1 register followed by reading DR register.

EV8: EVF=1, BTF=1, cleared by reading SR1 register followed by writing DR register.

EV9: EVF=1, ADD10=1, cleared by reading SR1 register followed by writing DR register.

12 ELECTRICAL CHARACTERISTICS

12.1 PARAMETER CONDITIONS

Unless otherwise specified, all voltages are referred to $\mathrm{V}_{\mathrm{SS}}.$

12.1.1 Minimum and Maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A=25^{\circ}C$ and $T_A=T_Amax$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean $\pm 3\Sigma$).

12.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A=25^{\circ}$ C, $V_{DD}=5$ V.They are given only as design guidelines and are not tested.

12.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

12.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in Figure 70.

Figure 70. Pin loading conditions



12.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in Figure 71.

Figure 71. Pin input voltage





CLOCK AND TIMING CHARACTERISTICS (Cont'd)

fore	Typical Ceramic Resonators ¹⁾		
Supplier	(MHz)	Reference ²⁾	Recommended OSCRANGE Option bit configuration
	2	CSTCC2M00G56A-R0	MP Mode ³⁾
ata	4	CSTCR4M00G55B-R0	MS Mode
Mui	8	CSTCE8M00G55A-R0	HS Mode
	16	CSTCE16M0G53A-R0	HS Mode

Notes:

1. Resonator characteristics given by the ceramic resonator manufacturer.

SMD = [-R0: Plastic tape package (Ø =180mm), -B0: Bulk] LEAD = [-A0: Flat pack package (Radial taping Ho= 18mm), -B0: Bulk]

3. LP mode is not recommended for 2 MHz resonator because the peak to peak amplitude is too small (>0.8V) For more information on these resonators, please consult www.murata.com



12.10 TIMER PERIPHERAL CHARACTERISTICS

Subject to general operating conditions for $V_{\text{DD}},\,f_{\text{OSC}},$ and T_{A} unless otherwise specified.

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output...).

12.10.1 8-Bit PWM-ART Auto-Reload Timer

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
t	PW/M resolution time		1			t _{CPU}
^r res(PWM)		f _{CPU} =8MHz	125			ns
f _{EXT}	ART external clock frequency		0		f _{CPU} /2	MH-7
f _{PWM}	PWM repetition rate		0		f _{CPU} /2	
Res _{PWM}	PWM resolution				8	bit
V _{OS}	PWM/DAC output step voltage	V _{DD} =5V, Res=8-bits		20		mV

12.10.2 16-Bit Timer

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
t _{w(ICAP)in}	Input capture pulse time		1			t _{CPU}
t _{res(PWM)} P	PW/M resolution time		2			t _{CPU}
		f _{CPU} =8MHz	250			ns
f _{EXT}	Timer external clock frequency		0		f _{CPU} /4	MHz
f _{PWM}	PWM repetition rate		0		f _{CPU} /4	MHz
Res _{PWM}	PWM resolution				16	bit

COMMUNICATION INTERFACE CHARACTERISTICS (Cont'd)

The following table gives the values to be written in the I2CCCR register to obtain the required I^2C SCL line frequency.

Table 28. SCL Frequency Table

				I2CCCI	R Value			
f _{SCL}		f _{CPU} =	4 MHz.			f _{CPU} =	8 MHz.	
(kHz)	V _{DD} =	V _{DD} = 4.1 V		V _{DD} = 5 V		: 4.1 V	V _{DD} = 5 V	
	R_P=3.3k Ω	R_P=4.7k Ω	R_P=3.3k Ω	R_P=4.7k Ω	$R_P=3.3k\Omega$	$R_P=4.7k\Omega$	$R_P=3.3k\Omega$	R_P=4.7k Ω
400	NA	NA	NA	NA	83h	83	83h	83h
300	NA	NA	NA	NA	85h	85h	85h	85h
200	83h	83h	83h	83h	8Ah	89h	8Ah	8Ah
100	10h	10h	10h	10h	24h	23h	24h	23h
50	24h	24h	24h	24h	4Ch	4Ch	4Ch	4Ch
20	5Fh	5Fh	5Fh	5Fh	FFh	FFh	FFh	FFh

Legend:

 R_P = External pull-up resistance f_{SCL} = I²C speed NA = Not achievable

Note:

– For speeds around 200 kHz, achieved speed can have $\pm 5\%$ tolerance

- For other speed ranges, achieved speed can have ±2% tolerance

The above variations depend on the accuracy of the external components used.

16 REVISION HISTORY

Table 32. Revision History

Date	Revision	Description of Changes
		Added "32-Pin LQFP Package Pinout" on page 10
		Removed CSS feature in "SYSTEM INTEGRITY MANAGEMENT (SI)" on page 29.
21-Mar-2006	2	Updated "DEVICE ORDERING INFORMATION AND TRANSFER OF CUSTOMER CODE"
		on page 177
		Updated "KNOWN LIMITATIONS" on page 186
10-Apr-2006	3	Removed blank pages
		In Table 2 added note for I/O Port E2 (PE2) output mode "pull-up always activated"
		Deleted the sentence in Section 4.3.1 'Readout protection is not supported if LVD is enabled'
		In Section 10.4 16-bit timer, replaced text in note 3 with "In both internal and external clock modes, OCFi and OCMPi are set while the counter value equals the OCiR register value (see Figure 50 for an example with fCPU/2 and Figure 51 for an example with fCPU/4). This behavior is the same in OPM or PWM mode."
10-Apr-2007	4	Removed Compare Register i Latch signal from Figure 51.
· • · · p· _ • • ·		Removed EMC protective circuitry in Figure 87 on page 159 (device works correctly without these components)
		Changed Footnote 4 in Section 12.11.1
		Added 'TIMD set simultaneously with OC interrupt' in Section 15.1.2
		Added 'Pull-up always active on PE2' in Section 15.1.8
		Deleted limitations 'Halt ActiveHalt Power consumption' 'I2C interrupt exit from Halt/Active- Halt' and Safe connection of OSC1/OSC2 pins' in Section 15
13-Oct-2008	5	Title of the document changed Modified "Starting the Conversion" on page 129 Modified t _{RET} and N _{RW} values in "FLASH Memory" on page 151 Modified "Absolute Maximum Ratings (Electrical Sensitivity)" on page 154 Values in inches rounded to 4 decimal digits (instead of 3) in "PACKAGE MECHANICAL DA- TA" on page 170 Modified "PACKAGE CHARACTERISTICS" on page 170 (Section 13.3)
		Modified "TIMD set simultaneously with OC interrupt" on page 185 Modified Section 14.2 DEVICE ORDERING INFORMATION AND TRANSFER OF CUS- TOMER CODE on page 176 (Figure 102 and option list)

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