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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	11
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	16-VQFN Exposed Pad
Supplier Device Package	16-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f610-e-ml

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

PIC16F610/16HV610 16-Pin Diagram (QFN)



TABLE 3:	PIC16F610/16HV610	16-PIN SUMMARY

I/O	Pin	Comparators	Timers	ers Interrupts Pull-ups		Basic
RA0	12	C1IN+	-	IOC	Y	ICSPDAT
RA1	11	C12IN0-		IOC	Y	ICSPCLK
RA2	10	C1OUT	TOCKI	INT/IOC	Y	—
RA3 ⁽¹⁾	3	—	_	IOC	Y(2)	MCLR/VPP
RA4	2	—	T1G	IOC	Y	OSC2/CLKOUT
RA5	1	—	T1CKI	IOC	Y	OSC1/CLKIN
RC0	9	C2IN+	—	—	—	—
RC1	8	C12IN1-		—		—
RC2	7	C12IN2-	—	—	_	—
RC3	6	C12IN3-		—	—	_
RC4	5	C2OUT	_	—	—	—
RC5	4	—		—	_	_
—	16	—	_	—	_	Vdd
—	13					Vss

Note 1: Input only.

2: Only when pin is configured for external MCLR.

2.2.2.1 STATUS Register

The STATUS register, shown in Register 2-1, contains:

- the arithmetic status of the ALU
- · the Reset status

-n = Value at POR

• the bank select bits for data memory (RAM)

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the TO and PD bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, CLRF STATUS, will clear the upper three bits and set the Z bit. This leaves the STATUS register as `000u uluu' (where u = unchanged).

It is recommended, therefore, that only BCF, BSF, SWAPF and MOVWF instructions are used to alter the STATUS register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits, see the **Section 13.0 "Instruction Set Summary"**.

- Note 1: Bits IRP and RP1 of the STATUS register are not used by the PIC16F610/616/16HV610/616 and should be maintained as clear. Use of these bits is not recommended, since this may affect upward compatibility with future products.
 - 2: The <u>C</u> and <u>DC</u> bits operate as a Borrow and Digit Borrow out bit, respectively, in subtraction. See the SUBLW and SUBWF instructions for examples.

x = Bit is unknown

REGISTER 2-1: STATUS: STATUS REGISTER

'1' = Bit is set

Reserved	Reserved	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x		
IRP	RP1	RP0	TO	PD	Z	DC	С		
bit 7 k									
Legend:									
R = Readable bit W = Writable bit				U = Unimplemented bit, read as '0'					

'0' = Bit is cleared

bit 7	IRP: This bit is reserved and should be maintained as '0'
bit 6	RP1: This bit is reserved and should be maintained as '0'
bit 5	RP0: Register Bank Select bit (used for direct addressing) 1 = Bank 1 (80h – FFh) 0 = Bank 0 (00h – 7Fh)
bit 4	TO: Time-out bit
	 1 = After power-up, CLRWDT instruction or SLEEP instruction 0 = A WDT time-out occurred
bit 3	PD: Power-down bit 1 = After power-up or by the CLRWDT instruction 0 = By execution of the SLEEP instruction
bit 2	Z: Zero bit 1 = The result of an arithmetic or logic operation is zero 0 = The result of an arithmetic or logic operation is not zero
bit 1	DC: Digit Carry/Borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions), For Borrow, the polarity is reversed. 1 = A carry-out from the 4th low-order bit of the result occurred 0 = No carry-out from the 4th low-order bit of the result
bit 0	C : Carry/Borrow bit ⁽¹⁾ (ADDWF, ADDLW, SUBLW, SUBWF instructions) 1 = A carry-out from the Most Significant bit of the result occurred 0 = No carry-out from the Most Significant bit of the result occurred
Note 1:	For Borrow, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high-order or low-order bit of the source register.

2.2.2.6 PCON Register

The Power Control (PCON) register (see Table 12-2) contains flag bits to differentiate between a:

- Power-on Reset (POR)
- Brown-out Reset (BOR)
- Watchdog Timer Reset (WDT)
- External MCLR Reset

The PCON register also controls the software enable of the $\overline{\text{BOR}}.$

The PCON register bits are shown in Register 2-6.

REGISTER 2-6: PCON: POWER CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0 ⁽¹⁾
—	—	—	—	—	—	POR	BOR
bit 7							bit 0

Legend:											
R = Readable bit		W = Writable bit	U = Unimplemented bit,	read as '0'							
-n = Value at POR		'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown							
bit 7-2	Unimplemented: Read as '0'										
bit 1	POR: Pov	wer-on Reset Status bit									
	1 = No Po	= No Power-on Reset occurred									
	0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)										
bit 0 BOR: Brown-out Reset Status bit											
	1 = No Br	1 = No Brown-out Reset occurred									

0 = A Brown-out Reset occurred (must be set in software after a Brown-out Reset occurs)

Note 1: Reads as '0' if Brown-out Reset is disabled.







6.2.1 INTERNAL CLOCK SOURCE

When the internal clock source is selected the TMR1H:TMR1L register pair will increment on multiples of TCY as determined by the Timer1 prescaler.

6.2.2 EXTERNAL CLOCK SOURCE

When the external clock source is selected, the Timer1 module may work as a timer or a counter.

When counting, Timer1 is incremented on the rising edge of the external clock input T1CKI. In addition, the Counter mode clock can be synchronized to the microcontroller system clock or run asynchronously.

If an external clock oscillator is needed (and the microcontroller is using the INTOSC without CLKOUT), Timer1 can use the LP oscillator as a clock source.

Note:	In Counter mode, a falling edge must be
	registered by the counter prior to the first
	incrementing rising edge.

6.3 Timer1 Prescaler

Timer1 has four prescaler options allowing 1, 2, 4 or 8 divisions of the clock input. The T1CKPS bits of the T1CON register control the prescale counter. The prescale counter is not directly readable or writable; however, the prescaler counter is cleared upon a write to TMR1H or TMR1L.

6.4 Timer1 Oscillator

A low-power 32.768 kHz crystal oscillator is built-in between pins OSC1 (input) and OSC2 (output). The oscillator is enabled by setting the T1OSCEN control bit of the T1CON register. The oscillator will continue to run during Sleep.

The Timer1 oscillator is shared with the system LP oscillator. Thus, Timer1 can use this mode only when the primary system clock is derived from the internal oscillator or when the oscillator is in the LP Oscillator mode. The user must provide a software time delay to ensure proper oscillator start-up.

TRISA5 and TRISA4 bits are set when the Timer1 oscillator is enabled. RA5 and RA4 bits read as '0' and TRISA5 and TRISA4 bits read as '1'.

Note: The oscillator requires a start-up and stabilization time before use. Thus, T1OSCEN should be set and a suitable delay observed prior to enabling Timer1.

6.5 Timer1 Operation in Asynchronous Counter Mode

If control bit T1SYNC of the T1CON register is set, the external clock input is not synchronized. The timer continues to increment asynchronous to the internal phase clocks. The timer will continue to run during Sleep and can generate an interrupt on overflow, which will wake-up the processor. However, special precautions in software are needed to read/write the timer (see Section 6.5.1 "Reading and Writing Timer1 in Asynchronous Counter Mode").

- Note: When switching from synchronous to asynchronous operation, it is possible to skip an increment. When switching from asynchronous to synchronous operation, it is possible to produce an additional increment.
- Note: In asynchronous counter mode or when using the internal oscillator and T1ACS=1, Timer1 can not be used as a time base for the capture or compare modes of the ECCP module (for PIC16F616/HV616 only).

6.5.1 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L while the timer is running from an external asynchronous clock will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself, poses certain problems, since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers, while the register is incrementing. This may produce an unpredictable value in the TMR1H:TMR1L register pair.

6.6 Timer1 Gate

Timer1 gate source is software configurable to be the T1G pin or the output of Comparator C2. This allows the device to directly time external events using T1G or analog events using Comparator C2. See the CM2CON1 register (Register 8-3) for selecting the Timer1 gate source. This feature can simplify the software for a Delta-Sigma A/D converter and many

other applications. For more information on Delta-Sigma A/D converters, see the Microchip web site (www.microchip.com).

Note:	TMR1GE bit of the T1CON register must
	be set to use either $\overline{T1G}$ or C2OUT as the
	Timer1 gate source. See the CM2CON1
	register (Register 8-3) for more informa-
	tion on selecting the Timer1 gate source.

Timer1 gate can be inverted using the T1GINV bit of the T1CON register, whether it originates from the T1G pin or Comparator C2 output. This configures Timer1 to measure either the active-high or active-low time between events.

6.7 Timer1 Interrupt

The Timer1 register pair (TMR1H:TMR1L) increments to FFFFh and rolls over to 0000h. When Timer1 rolls over, the Timer1 interrupt flag bit of the PIR1 register is set. To enable the interrupt on rollover, you must set these bits:

- TMR1IE bit of the PIE1 register
- PEIE bit of the INTCON register
- GIE bit of the INTCON register
- T1SYNC bit of the T1CON register
- TMR1CS bit of the T1CON register
- T1OSCEN bit of the T1CON register (can be set)

The interrupt is cleared by clearing the TMR1IF bit in the Interrupt Service Routine.

Note: The TMR1H:TTMR1L register pair and the TMR1IF bit should be cleared before enabling interrupts.

6.8 Timer1 Operation During Sleep

Timer1 can only operate during Sleep when setup in Asynchronous Counter mode. In this mode, an external crystal or clock source can be used to increment the counter. To set up the timer to wake the device:

- TMR1ON bit of the T1CON register must be set
- TMR1IE bit of the PIE1 register must be set
- PEIE bit of the INTCON register must be set

The device will wake-up on an overflow and execute the next instruction. If the GIE bit of the INTCON register is set, the device will call the Interrupt Service Routine (0004h).

6.9 ECCP Capture/Compare Time Base (PIC16F616/16HV616 Only)

The ECCP module uses the TMR1H:TMR1L register pair as the time base when operating in Capture or Compare mode.

In Capture mode, the value in the TMR1H:TMR1L register pair is copied into the CCPR1H:CCPR1L register pair on a configured event.

In Compare mode, an event is triggered when the value CCPR1H:CCPR1L register pair matches the value in the TMR1H:TMR1L register pair. This event can be a Special Event Trigger.

For more information, see Section 10.0 "Enhanced Capture/Compare/PWM (With Auto-Shutdown and Dead Band) Module (PIC16F616/16HV616 Only)".

6.10 ECCP Special Event Trigger (PIC16F616/16HV616 Only)

When the ECCP is configured to trigger a special event, the trigger will clear the TMR1H:TMR1L register pair. This special event does not cause a Timer1 interrupt. The ECCP module may still be configured to generate a ECCP interrupt.

In this mode of operation, the CCPR1H:CCPR1L register pair effectively becomes the period register for Timer1.

Timer1 should be synchronized to the FOSC to utilize the Special Event Trigger. Asynchronous operation of Timer1 can cause a Special Event Trigger to be missed.

In the event that a write to TMR1H or TMR1L coincides with a Special Event Trigger from the ECCP, the write will take precedence.

For more information, see **Section 10.2.4** "**Special Event Trigger**".

6.11 Comparator Synchronization

The same clock used to increment Timer1 can also be used to synchronize the comparator output. This feature is enabled in the Comparator module.

When using the comparator for Timer1 gate, the comparator output should be synchronized to Timer1. This ensures Timer1 does not miss an increment if the comparator changes.

For more information, see Section 8.8.2 "Synchronizing Comparator C2 Output to Timer1".

8.5 Operation During Sleep

The comparator, if enabled before entering Sleep mode, remains active during Sleep. The additional current consumed by the comparator is shown separately in **Section 15.0** "**Electrical Specifications**". If the comparator is not used to wake the device, power consumption can be minimized while in Sleep mode by turning off the comparator. Each comparator is turned off by clearing the CxON bit of the CMxCON0 register.

A change to the comparator output can wake-up the device from Sleep. To enable the comparator to wake the device from Sleep, the CxIE bit of the PIE1 register and the PEIE bit of the INTCON register must be set. The instruction following the Sleep instruction always executes following a wake from Sleep. If the GIE bit of the INTCON register is also set, the device will then execute the interrupt service routine.

8.6 Effects of a Reset

A device Reset forces the CMxCON0 and CM2CON1 registers to their Reset states. This forces both comparators and the voltage references to their OFF states.

9.0 ANALOG-TO-DIGITAL CONVERTER (ADC) MODULE (PIC16F616/16HV616 ONLY)

The Analog-to-Digital Converter (ADC) allows conversion of an analog input signal to a 10-bit binary representation of that signal. This device uses analog inputs, which are multiplexed into a single sample and hold circuit. The output of the sample and hold is connected to the input of the converter. The converter generates a 10-bit binary result via successive approximation and stores the conversion result into the ADC result registers (ADRESL and ADRESH).

The ADC voltage reference is software selectable to either VDD or a voltage applied to the external reference pins.

The ADC can generate an interrupt upon completion of a conversion. This interrupt can be used to wake-up the device from Sleep.

Figure 9-1 shows the block diagram of the ADC.

FIGURE 9-1: ADC BLOCK DIAGRAM



Note: The ADRESL and ADRESH registers are read-only.

NOTES:

12.2 Calibration Bits

The 8 MHz internal oscillator is factory calibrated. These calibration values are stored in fuses located in the Calibration Word (2008h). The Calibration Word is not erased when using the specified bulk erase sequence in the *Memory Programming Specification* (DS41284) and thus, does not require reprogramming.

12.3 Reset

The PIC16F610/616/16HV610/616 differentiates between various kinds of Reset:

- a) Power-on Reset (POR)
- b) WDT Reset during normal operation
- c) WDT Reset during Sleep
- d) MCLR Reset during normal operation
- e) MCLR Reset during Sleep
- f) Brown-out Reset (BOR)

Some registers are not affected in any Reset condition; their status is unknown on POR and unchanged in any other Reset. Most other registers are reset to a "Reset state" on:

- Power-on Reset
- MCLR Reset
- MCLR Reset during Sleep
- WDT Reset
- Brown-out Reset (BOR)

WDT wake-up does not cause register resets in the same manner as a WDT Reset since wake-up is viewed as the resumption of normal operation. TO and \overline{PD} bits are set or cleared differently in different Reset situations, as indicated in Table 12-2. Software can use these bits to determine the nature of the Reset. See Table 12-4 for a full description of Reset states of all registers.

A simplified block diagram of the On-Chip Reset Circuit is shown in Figure 12-1.

The MCLR Reset path has a noise filter to detect and ignore small pulses. See **Section 15.0** "**Electrical Specifications**" for pulse-width specifications.

FIGURE 12-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



12.3.5 TIME-OUT SEQUENCE

On power-up, the time-out sequence is as follows:

- PWRT time-out is invoked after POR has expired.
- OST is activated after the PWRT time-out has expired.

The total time-out will vary based on oscillator configuration and PWRTE bit status. For example, in EC mode with PWRTE bit erased (PWRT disabled), there will be no time-out at all. Figure 12-4, Figure 12-5 and Figure 12-6 depict time-out sequences.

Since the time-outs occur from the POR pulse, if $\overline{\text{MCLR}}$ is kept low long enough, the time-outs will expire. Then, bringing $\overline{\text{MCLR}}$ high will begin execution immediately (see Figure 12-5). This is useful for testing purposes or to synchronize more than one PIC16F610/616/ 16HV610/616 device operating in parallel.

Table 12-5 shows the Reset conditions for some special registers, while Table 12-4 shows the Reset conditions for all the registers.

12.3.6 POWER CONTROL (PCON) REGISTER

The Power Control register PCON (address 8Eh) has two Status bits to indicate what type of Reset occurred last.

Bit 0 is \overrightarrow{BOR} (Brown-out). \overrightarrow{BOR} is unknown on Poweron Reset. It must then be set by the user and checked on subsequent Resets to see if $\overrightarrow{BOR} = 0$, indicating that a Brown-out has occurred. The \overrightarrow{BOR} Status bit is a "don't care" and is not necessarily predictable if the brown-out circuit is disabled (BOREN<1:0> = 00 in the Configuration Word register).

Bit 1 is POR (Power-on Reset). It is a '0' on Power-on Reset and unaffected otherwise. The user must write a '1' to this bit following a Power-on Reset. On a subsequent Reset, if POR is '0', it will indicate that a Power-on Reset has occurred (i.e., VDD may have gone too low).

For more information, see **Section 12.3.4** "**Brown-out Reset (BOR)**".

Oppillator Configuration	Powe	er-up	Brown-o	Wake-up from	
Oscillator Configuration	PWRTE = 0	PWRTE = 1	PWRTE = 0	PWRTE = 1	Sleep
XT, HS, LP	TPWRT + 1024 • Tosc	1024 • Tosc	TPWRT + 1024 • Tosc	1024 • Tosc	1024 • Tosc
RC, EC, INTOSC	TPWRT	—	TPWRT	_	—

TABLE 12-1: TIME-OUT IN VARIOUS SITUATIONS

TABLE 12-2: STATUS/PCON BITS AND THEIR SIGNIFICANCE

POR	BOR	то	PD	Condition
0	х	1	1	Power-on Reset
u	0	1	1	Brown-out Reset
u	u	0	u	WDT Reset
u	u	0	0	WDT Wake-up
u	u	u	u	MCLR Reset during normal operation
u	u	1	0	MCLR Reset during Sleep

Legend: u = unchanged, x = unknown

TABLE 12-3: SUMMARY OF REGISTERS ASSOCIATED WITH BROWN-OUT RESET

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets ⁽¹⁾
PCON			_	_			POR	BOR	dd	uu
STATUS	IRP	RP1	RP0	TO	PD	Z	DC	С	0001 1xxx	000q quuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition. Shaded cells are not used by BOR.

Note 1: Other (non Power-up) Resets include MCLR Reset and Watchdog Timer Reset during normal operation.

FIGURE 12-9:	WAKE-UP FROM S	SLEEP THRO	UGH INTER	RUPT		
, Q1 Q2 OSC1/¯/¯_ CLKOUT ⁽⁴⁾ , INT pin	Q3 Q4 ; Q1 Q2 Q3 Q4 ; Q 		Q1 Q2 Q3 Q4 	(01 02 03 04; /~_~/	Q1 Q2 Q3 Q4;(Q1 Q2 Q3 Q4 \/\/\/\
INTF flag (INTCON reg.)			Interrupt Laten	_{Cy} (3)		
GIE bit (INTCON reg.)	P	rocessor in Sleep				
Instruction Flow PC X F	PC / PC+1 /	PC + 2	X PC + 2	PC+2 X	0004h X	0005h
Instruction { Inst(PC	i) = Sleep Inst(PC + 1)		Inst(PC + 2)		Inst(0004h)	Inst(0005h)
Instruction { Inst(PC – 1) Sleep		Inst(PC + 1)	Dummy Cycle	Dummy Cycle	Inst(0004h)
Note 1: XT, HS of 2: Tost = 1 3: GIE = 1	or LP Oscillator mode assumed 1024 Tosc (drawing not to scale ' assumed. In this case after w	d. e). This delay does rake-up, the process	not apply to EC, II sor jumps to 0004	NTOSC and RC Os n. If GIE = '0', exec	scillator modes. ution will continue	in-line.

4: CLKOUT is not available in XT, HS, LP or EC Oscillator modes, but shown here for timing reference.

12.8 Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out using $\mathsf{ICSP}^{\mathsf{TM}}$ for verification purposes.

Note:	The entire Flash program m	nemory will be					
	erased when the code protection is turned						
	off. See the Memory	Programming					
	Specification (DS41284)	for more					
	information.						

12.9 ID Locations

Four memory locations (2000h-2003h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are not accessible during normal execution but are readable and writable during Program/Verify mode. Only the Least Significant 7 bits of the ID locations are used.

Mnemonic,		Description		14-Bit Opcode				Status	
Оре	erands	Description		MSb			LSb	Affected	Notes
BYTE-ORIENTED FILE REGISTER OPERATIONS									
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C, DC, Z	1, 2
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	1, 2
CLRF	f	Clear f	1	00	0001	lfff	ffff	Z	2
CLRW	_	Clear W	1	00	0001	0xxx	xxxx	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	1, 2
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	1, 2
DECFSZ	f, d	Decrement f, Skip if 0	1 (2)	00	1011	dfff	ffff		1, 2, 3
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	1, 2
INCFSZ	f, d	Increment f, Skip if 0	1 (2)	00	1111	dfff	ffff		1, 2, 3
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	1, 2
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	1, 2
MOVWF	f	Move W to f	1	00	0000	lfff	ffff		
NOP	-	No Operation	1	00	0000	0xx0	0000		
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	С	1, 2
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	С	1, 2
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C, DC, Z	1, 2
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff		1, 2
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	1, 2
		BIT-ORIENTED FILE REGIST			IS			1	
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		1.2
BSF	f. b	Bit Set f	1	01	01bb	bfff	ffff		1.2
BTFSC	f. b	Bit Test f. Skip if Clear	1 (2)	01	10bb	bfff	ffff		3
BTFSS	f. b	Bit Test f. Skip if Set	1 (2)	01	11bb	bfff	ffff		3
	-, -	LITERAL AND CONTROL	OPERAT	IONS					-
ADDI W	k	Add literal and W	1	11	111x	kkkk	kkkk	C. DC. 7	
ANDIW	k	AND literal with W	1	11	1001	kkkk	kkkk	7	
CALL	k	Call Subroutine	2	10	0kkk	kkkk	kkkk	-	
CIRWDT	· _	Clear Watchdog Timer	1	00	0000	0110	0100	TO PD	
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk		
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLW	k	Move literal to W	1	11	00xx	kkkk	kkkk	_	
RETFIE	_	Return from interrupt	2	00	0000	0000	1001		
RETLW	k	Return with literal in W	2	11	01xx	kkkk	kkkk		
RETURN	_	Return from Subroutine	2	00	0000	0000	1000		
SLEEP	_	Go into Standby mode	1	00	0000	0110	0011	TO, PD	
SUBLW	k	Subtract W from literal	1	11	110x	kkkk	kkkk	C, DC. Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z	

TABLE 13-2: PIC16F610/616/16HV610/616 INSTRUCTION SET

Note 1: When an I/O register is modified as a function of itself (e.g., MOVF PORTA, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 module.

3: If the Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

14.2 MPLAB C Compilers for Various Device Families

The MPLAB C Compiler code development systems are complete ANSI C compilers for Microchip's PIC18, PIC24 and PIC32 families of microcontrollers and the dsPIC30 and dsPIC33 families of digital signal controllers. These compilers provide powerful integration capabilities, superior code optimization and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

14.3 HI-TECH C for Various Device Families

The HI-TECH C Compiler code development systems are complete ANSI C compilers for Microchip's PIC family of microcontrollers and the dsPIC family of digital signal controllers. These compilers provide powerful integration capabilities, omniscient code generation and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

The compilers include a macro assembler, linker, preprocessor, and one-step driver, and can run on multiple platforms.

14.4 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel[®] standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

14.5 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler and the MPLAB C18 C Compiler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

14.6 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC devices. MPLAB C Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- · Support for fixed-point and floating-point data
- Command line interface
- · Rich directive set
- Flexible macro language
- MPLAB IDE compatibility

14.11 PICkit 2 Development Programmer/Debugger and PICkit 2 Debug Express

The PICkit[™] 2 Development Programmer/Debugger is a low-cost development tool with an easy to use interface for programming and debugging Microchip's Flash families of microcontrollers. The full featured Windows® programming interface supports baseline (PIC10F, PIC12F5xx, PIC16F5xx), midrange (PIC12F6xx, PIC16F), PIC18F, PIC24, dsPIC30, dsPIC33, and PIC32 families of 8-bit, 16-bit, and 32-bit microcontrollers, and many Microchip Serial EEPROM products. With Microchip's powerful MPLAB Integrated Development Environment (IDE) the PICkit[™] 2 enables in-circuit debugging on most PIC[®] microcontrollers. In-Circuit-Debugging runs, halts and single steps the program while the PIC microcontroller is embedded in the application. When halted at a breakpoint, the file registers can be examined and modified.

The PICkit 2 Debug Express include the PICkit 2, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

14.12 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an MMC card for file storage and data applications.

14.13 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM[™] and dsPICDEM[™] demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ[®] security ICs, CAN, IrDA[®], PowerSmart battery management, SEEVAL[®] evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

15.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings^(†)

Ambient temperature under bias	40° to +125°C					
Storage temperature	65°C to +150°C					
Voltage on VDD with respect to Vss	0.3V to +6.5V					
Voltage on MCLR with respect to Vss	0.3V to +13.5V					
Voltage on all other pins with respect to Vss	0.3V to (VDD + 0.3V)					
Total power dissipation ⁽¹⁾						
Maximum current out of Vss pin	95 mA					
Maximum current into Vod pin	95 mA					
Input clamp current, Iık (Vı < 0 or Vı > VDD)	± 20 mA					
Output clamp current, Ioк (Vo < 0 or Vo >VDD)	± 20 mA					
Maximum output current sunk by any I/O pin	25 mA					
Maximum output current sourced by any I/O pin25 mA						
Maximum current sunk by PORTA and PORTC (combined)	90 mA					
Maximum current sourced PORTA and PORTC (combined)	90 mA					
Note 1: Power dissipation is calculated as follows: PDIS = VDD x {IDD $-\sum$ IOH} + \sum {(VI IOL).	о – Vон) х Iон} + ∑(Vol х					

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

TABLE 15-2: OSCILLATOR PARAMETERS

Standard Operating Conditions (unless otherwise stated)Operating Temperature $-40^{\circ}C \le TA \le +125^{\circ}C$								
Param No.	Sym	Characteristic	Freq. Tolerance	Min	Тур†	Max	Units	Conditions
OS06	TWARM	Internal Oscillator Switch when running ⁽³⁾	—			2	Tosc	Slowest clock
OS07	INTosc	Internal Calibrated	±1%	3.96	4.0	4.04	MHz	$VDD = 3.5V, T_A = 25^{\circ}C$
	INTOSC Frequency ⁽²⁾ (4MHz)		±2%	3.92	4.0	4.08	MHz	$2.5V \le VDD \le 5.5V$, 0°C $\le TA \le +85$ °C
			±5%	3.80	4.0	4.2	MHz	$2.0V \le VDD \le 5.5V$, -40°C \le TA \le +85°C (Ind.), -40°C \le TA \le +125°C (Ext.)
OS08	INTosc	Internal Calibrated	±1%	7.92	8.0	8.08	MHz	$VDD = 3.5V, T_A = 25^{\circ}C$
		INTOSC Frequency ⁽²⁾ (8MHz)	±2%	7.84	8.0	8.16	MHz	$2.5V \le VDD \le 5.5V$, $0^{\circ}C \le TA \le +85^{\circ}C$
			±5%	7.60	8.0	8.40	MHz	$2.0V \le VDD \le 5.5V$, -40°C \le TA \le +85°C (Ind.), -40°C \le TA \le +125°C (Ext.)
OS10*	TIOSC ST	INTOSC Oscillator Wake-	_	5.5	12	24	μS	$VDD = 2.0V, -40^{\circ}C \text{ to } +85^{\circ}C$
		up from Sleep	—	3.5	7	14	μs	VDD = 3.0V, -40°C to +85°C
		Stan-up nine	—	3	6	11	μs	VDD = 5.0V, -40°C to +85°C

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TcY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to the OSC1 pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

2: To ensure these oscillator frequency tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 µF and 0.01 µF values in parallel are recommended.

3: By design.

TABLE 15-4:RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER
AND BROWN-OUT RESET PARAMETERS

Standard Operating Conditions (unless otherwise stated)Operating Temperature $-40^{\circ}C \le TA \le +125^{\circ}C$							
Param No.	Sym	Characteristic	Min	Тур†	Max	Units	Conditions
30	TMCL	MCLR Pulse Width (low)	2 5			μs μs	VDD = 5V, -40°C to +85°C VDD = 5V, -40°C to +125°C
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	10 10	20 20	30 35	ms ms	VDD = 5V, -40°C to +85°C VDD = 5V, -40°C to +125°C
32	Tost	Oscillation Start-up Timer Period ^(1, 2)	_	1024		Tosc	(NOTE 3)
33*	TPWRT	Power-up Timer Period	40	65	140	ms	
34*	Tioz	I/O High-impedance from MCLR Low or Watchdog Timer Reset	_	_	2.0	μs	
35*	VBOR	Brown-out Reset Voltage	2.0	2.15	2.3	V	(NOTE 4)
36*	VHYST	Brown-out Reset Hysteresis		100	_	mV	
37*	TBOR	Brown-out Reset Minimum Detection Period	100			μS	$VDD \leq VBOR$

Legend: TBD = To Be Determined

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- 2: By design.
- 3: Period of the slower clock.
- **4:** To ensure these voltage tolerances, VDD and VSS must be capacitivey decoupled as close to the device as possible. 0.1 μF and 0.01 μF values in parallel are recommended.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to the OSC1 pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

15.13 High Temperature Operation

This section outlines the specifications for <u>the</u> <u>PIC16F616 device operating in a temperature range</u> <u>between -40°C and 150°C.⁽⁴⁾</u> The specifications between -40°C and 150°C⁽⁴⁾ are identical to those shown in DS41302 and DS80329.

Note 1:	Writes	are	<u>not</u>	allowed	for	Flash
	Program	n Mer	nory a	above 125°	°C.	
э.		imina	cnoci	fications or	o inci	boacod

- All AC timing specifications are increased by 30%. This derating factor will include parameters such as TPWRT.
- **3:** The temperature range indicator in the part number is "H" for -40°C to 150°C.⁽⁴⁾

Example: PIC16F616T-H/ST indicates the device is shipped in a tAPE and reel configuration, in the TSSOP package, and is rated for operation from -40°C to 150°C.⁽⁴⁾

4: AEC-Q100 reliability testing for devices intended to operate at 150°C is 1,000 hours. Any design in which the total operating time from 125°C to 150°C will be greater than 1,000 hours is not warranted without prior written approval from Microchip Technology Inc.

TABLE 15-13: ABSOLUTE MAXIMUM RATINGS

Parameter	Source/Sink	Value	Units
Max. Current: VDD	Source	20	mA
Max. Current: Vss	Sink	50	mA
Max. Current: PIN	Source	5	mA
Max. Current: PIN	Sink	10	mA
Pin Current: at Voн	Source	3	mA
Pin Current: at VoL	Sink	8.5	mA
Port Current: A and C	Source	20	mA
Port Current: A and C	Sink	50	mA
Maximum Junction Temperature		155	°C

Note: Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

APPENDIX B: MIGRATING FROM OTHER PIC[®] DEVICES

This discusses some of the issues in migrating from other $\text{PIC}^{\textcircled{0}}$ devices to the <code>PIC16F6XX</code> Family of devices.

B.1 PIC16F676 to PIC16F610/616/16HV610/616

TABLE B-1: FEATURE COMPARISON

Feature	PIC16F676	PIC16F610/16HV610	PIC16F616/16HV616
Max Operating Speed	20 MHz	20 MHz	20 MHz
Max Program Memory (Words)	1024	1024	2048
SRAM (bytes)	64	64	128
A/D Resolution	10-bit	None	10-bit
Timers (8/16-bit)	1/1	1/1	2/1
Oscillator Modes	8	8	8
Brown-out Reset	Y	Y	Y
Internal Pull-ups	RA0/1/2/4/5	RA0/1/2/4/5, MCLR	RA0/1/2/4/5, MCLR
Interrupt-on-change	RA0/1/2/3/4/5	RA0/1/2/3/4/5	RA0/1/2/3/4/5
Comparator	1	2	2
ECCP	N	Ν	Y
INTOSC Frequencies	4 MHz	4/8 MHz	4/8 MHz
Internal Shunt Regulator	N	Y (PIC16HV610)	Y (PIC16HV616)

Note: This device has been designed to perform to the parameters of its data sheet. It has been tested to an electrical specification designed to determine its conformance with these parameters. Due to process differences in the manufacture of this device, this device may have different performance characteristics than its earlier version. These differences may cause this device to perform differently in your application than the earlier version of this device.